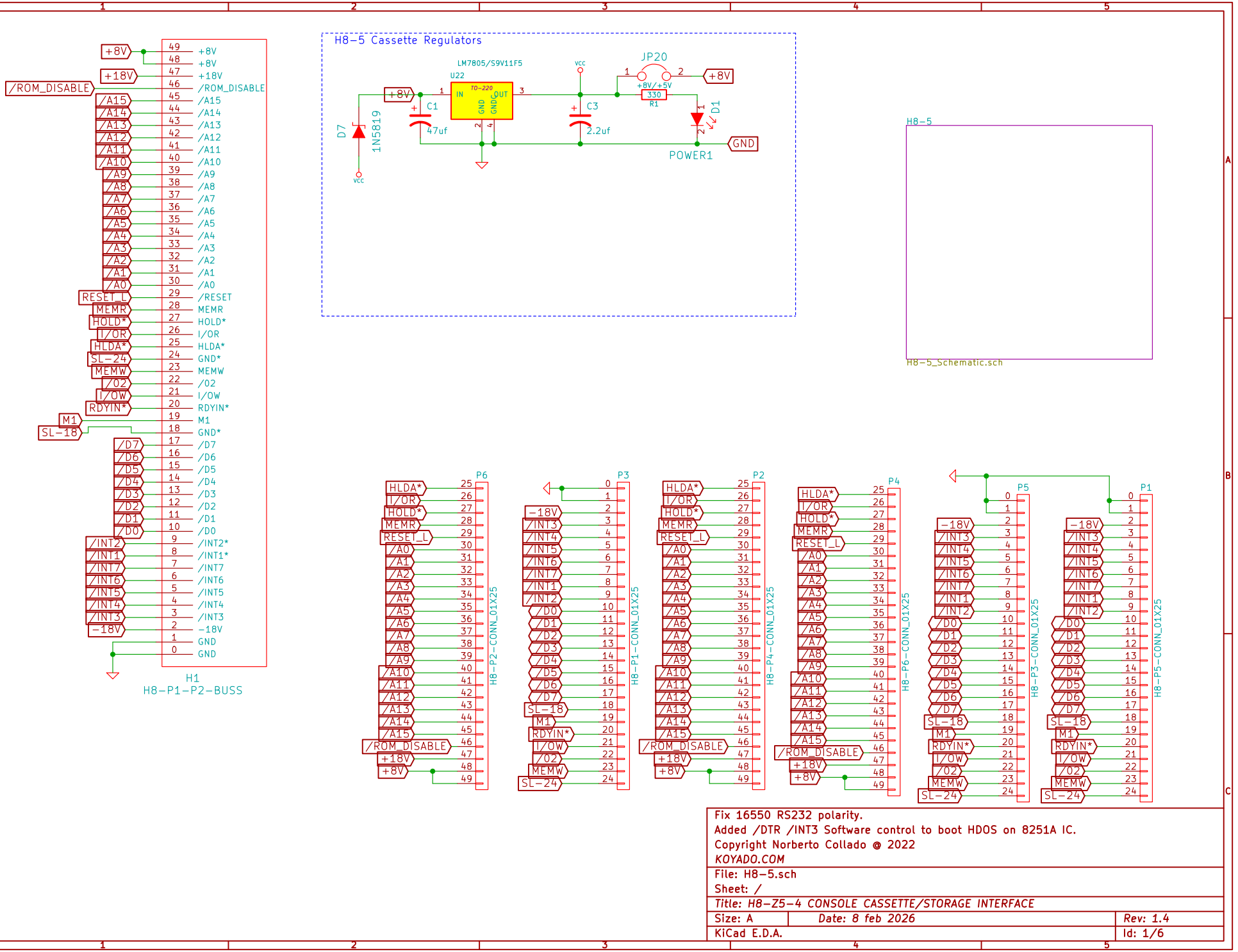
H8-5 Cassette Regulators
LM7805/S9V11F5
U22
TO-220
IN
GND
GNDO
OUT
VCC
JP20
+8V/+5V
330
R1
C1
47uf
C3
2.2uf
D7
1N5819
D1
POWER1
GND
+8V
+18V
H8-5
H8-5_Schematic.sch
/ROM_DISABLE
/A15
/A14
/A13
/A12
/A11
/A10
/A9
/A8
/A7
/A6
/A5
/A4
/A3
/A2
/A1
/A0
RESET_L
MEMR
HOLD*
I/OR
HLDA*
SL-24
MEMW
/O2
I/OW
RDYIN*
M1
SL-18
/D7
/D6
/D5
/D4
/D3
/D2
/D1
/D0
/INT2
/INT1
/INT7
/INT6
/INT5
/INT4
/INT3
-18V
GND
H1
H8-P1-P2-BUSS
P6
P3
P2
P4
P5
P1
H8-P2-CONN_01X25
H8-P1-CONN_01X25
H8-P4-CONN_01X25
H8-P6-CONN_01X25
H8-P3-CONN_01X25
H8-P5-CONN_01X25
Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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File: H8-5.sch
Sheet: /
Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE
Size: A
Date: 8 feb 2026
Rev: 1.4
KiCad E.D.A.
Id: 1/6

H8-5 I/O DECODER

370Q/371Q (LOAD/DUMP)
CASSETTE ON H8-5

H8-BUS

SPARE

H19 CONSOLE - 372Q & 373Q

P82C51 CONSOLE BAUD RATE

/DTR is needed to control interrupts
for HDOS boot on 8251A IC.

BUFFER ENABLED L

BUFFER DIRECTION CONTROL

ENABLE BUFFER

Audio Input

Audio Input Decoder.sch

Audio Out

Audio Out Circuit.sch

CASSETTE RECORDER

CASSETTE_RECORDER_CONTROLLER.sch

EXT-SW
RELAY-PIN4
RELAY-PIN5
RELAY-PIN6
RELAY-PIN7
AUDIO-IN
CASSETTE_AUDIO_OUT-PIN10
P103
CASSETTE INTERFACE

COM PORT

82C50.sch

Receives Data from Cassette or RS-232 circuit

Receives Clock from Cassette or H8T Baud Rate

CASSETTE/DTR

Selects between cassette input or RS-232 input.
EXT-SW CLOSED = RS-232 MODE
EXT-SW OPEN = CASSETTE MODE (DEFAULT)

On power-on, Cassette mode is selected
by default if EXT-SW is open.

Pin 1	RI
Pin 2	TXD
Pin 3	RXD
Pin 4	DSR
Pin 5	GND
Pin 6	DTR
Pin 7	CTS
Pin 8	RTS
Pin 9	Power Input /DCD

RS232 Pinout
(9 Pin Female)

Pin 5 Pin 1
Pin 9 Pin 6

1200bps/9600bps

RS-232 TO H8T FORMAT

RS-232 INTERFACE DESIGNED BY DAVE T. RUNKLE

http://www.astrorat.com/heathkith8computer/rs232interfaceonh85.html

Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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File: H8-5_Schematic.sch
Sheet: /H8-5/
Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE

Size: C	Date: 8 feb 2026	Rev: 1.4
KiCad E.D.A.		Id: 2/6

AUDIO COAXIAL CABLE
AUDIO-IN
P17
TP3
JP15
AUDIO
R102 10K
R101 100
D101 1N4148
D102 1N4148
C101 .047uf
R103 1K
R106 100K
C102 4.7uf
R104 1K
R105 10K
R107 3.3K
R108 100K
U102A
LM2901N
SLICER
FB1
FB
C2 10uf
R109 1K
VCC
Note: If using 74LS123, then R = 7.5K + 680 ohms.
R111 10K
C103 .001uf
U101A 74123
FREQUENCY DOUBLER
2.8usec
R112 10K
C104 .001uf
U101B 74123
Note: If using 74LS123, then R = 7.5K + 680 ohms.
2.8usec
U108A 74LS00
VIRTUAL POTS
RV113 5K
RV4 5K
RV3 5K
R114 7.5K * 1%
C105 .1uf
U103B 74123
SPACE DETECTOR
2.8usec
TP1
AUDIO IN
TP1
312 µSEC
DATA LATCH
U104A 74LS74
U104B 74LS74
74LS08 U117C
/RxD
Receiver Data
I/O
D701
R708 330
R115 10K
C106 .001uf
U103A 74123
Note: If using 74LS123, then R = 7.5K + 680 ohms.
2.8usec
CONTROLLED DIVIDER
U105A 74LS74
U105B 74LS74
R116 3.3K
R117 10K
* C107- 230PF for 1200bps
* C107 - .001uF for 300bps
** 10pf cap (C24) - when C107 is 220pf.
PLL CLOCK SYNTHESIZER
1.2kHz
230pf
C107
JP14
VCO
10pf
C24
**10pf
U106 CD4046
R122 100K
R123 1K
C108 1uf
1v
19.2 KHz
U108B 74LS00
Receiver Clock
/RxC
Note: Use only CD4046.
Do not use 74HC4046 as it runs faster.
R121 1M
VIRTUAL POTS
RV119 200K
RV1 200K
RV2 200K
R118 47K
PLL ADJUST
H0
L0
L1
H1
L0-H0
L1-H1
JP10
JP12
U107 74LS93
4800Hz -300 BPS
19.2 KHz - 1200BPS
CALIBRATION JUMPERS
TL/TP1/TP2
JP1
TP1
TP2
TL
JP2
TP3
TP4
TP3/TP4
P8
TP2
U117A 74LS08
2400Hz
2.4KHZ
P18

Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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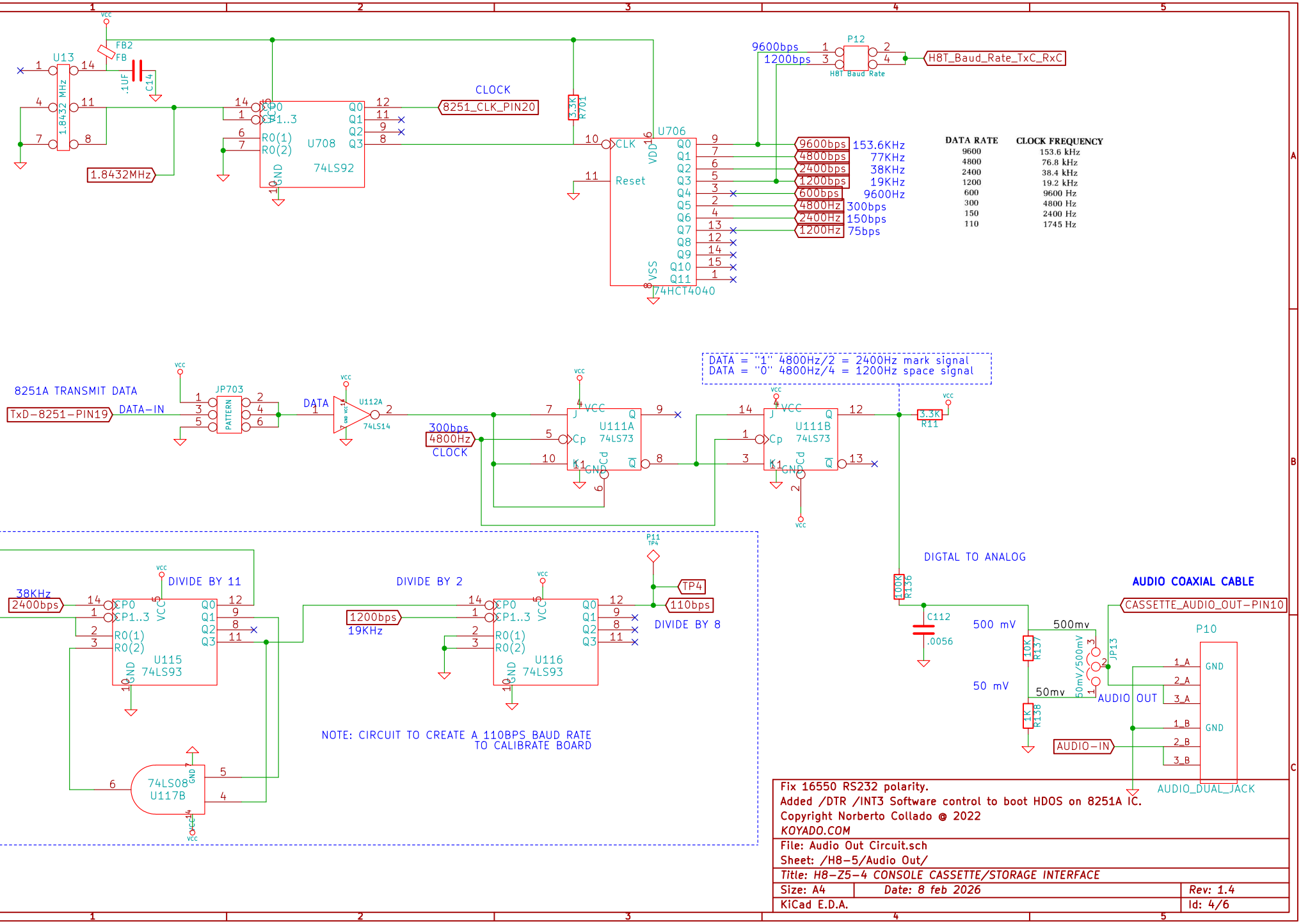
File: Audio Input Decoder.sch		
Sheet: /H8-5/Audio Input/		
Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE		
Size: B	Date: 8 feb 2026	Rev: 1.4
KiCad E.D.A.		Id: 3/6



Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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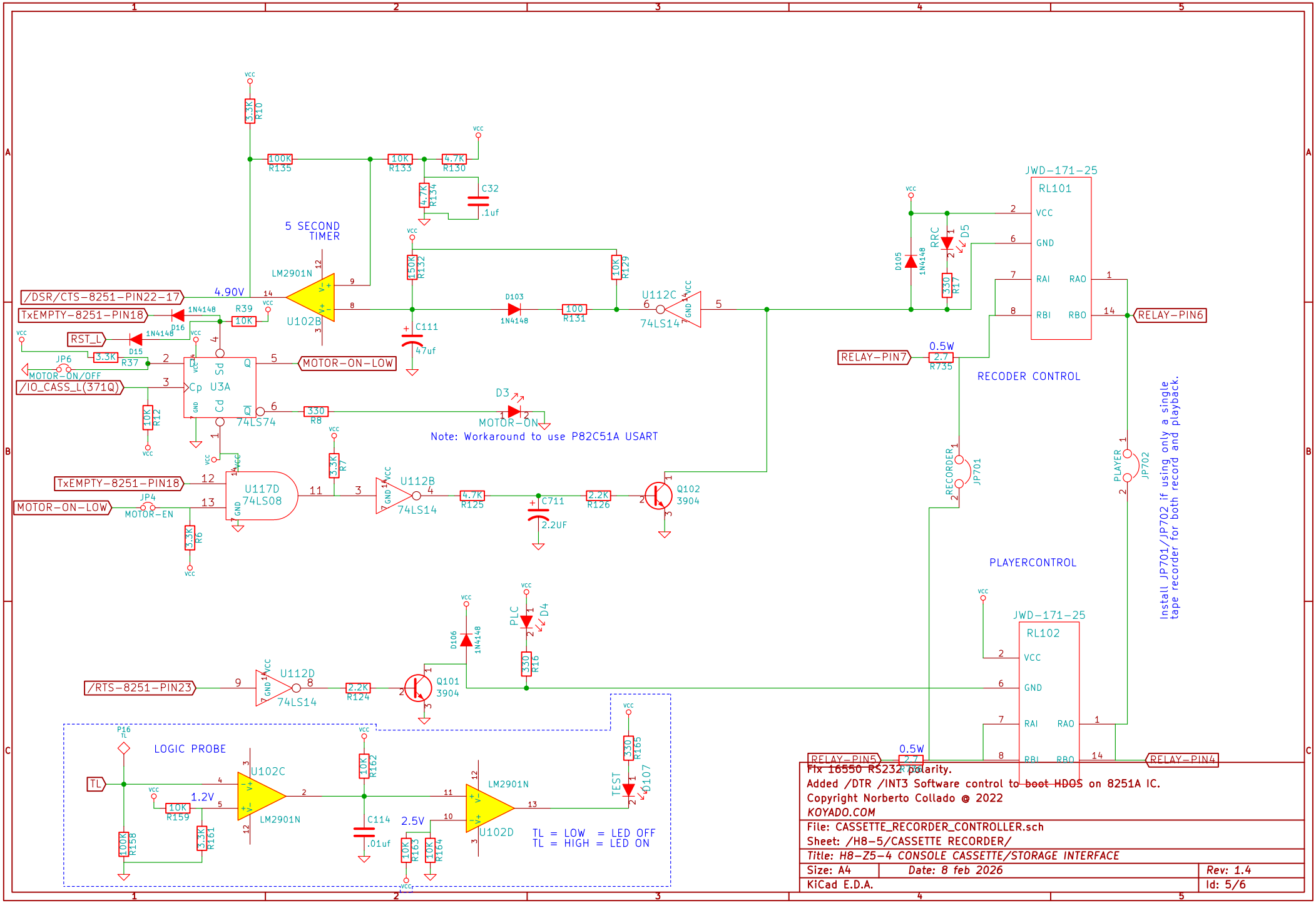
File: Audio Out Circuit.sch
Sheet: /H8-5/Audio Out/
Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE

Size: A4	Date: 8 feb 2026	Rev: 1.4
KiCad E.D.A.		Id: 4/6


5 SECOND TIMER
LM2901N
U102B
/DSR/CTS-8251-PIN22-17
TxEMPTY-8251-PIN18
RST_L
/IO_CASS_L(371Q)
MOTOR-ON/OFF
MOTOR-ON-LOW
U3A
74LS74
D3
MOTOR-ON
Note: Workaround to use P82C51A USART
U117D
74LS08
U112B
74LS14
Q102
3904
U112C
74LS14
U112D
74LS14
Q101
3904
/RTS-8251-PIN23
LOGIC PROBE
U102C
LM2901N
U102D
TL = LOW = LED OFF
TL = HIGH = LED ON
JWD-171-25
RL101
RL102
RECODER CONTROL
PLAYERCONTROL
RELAY-PIN6
RELAY-PIN7
RELAY-PIN5
RELAY-PIN4
Install JP701/JP702 if using only a single tape recorder for both record and playback.
Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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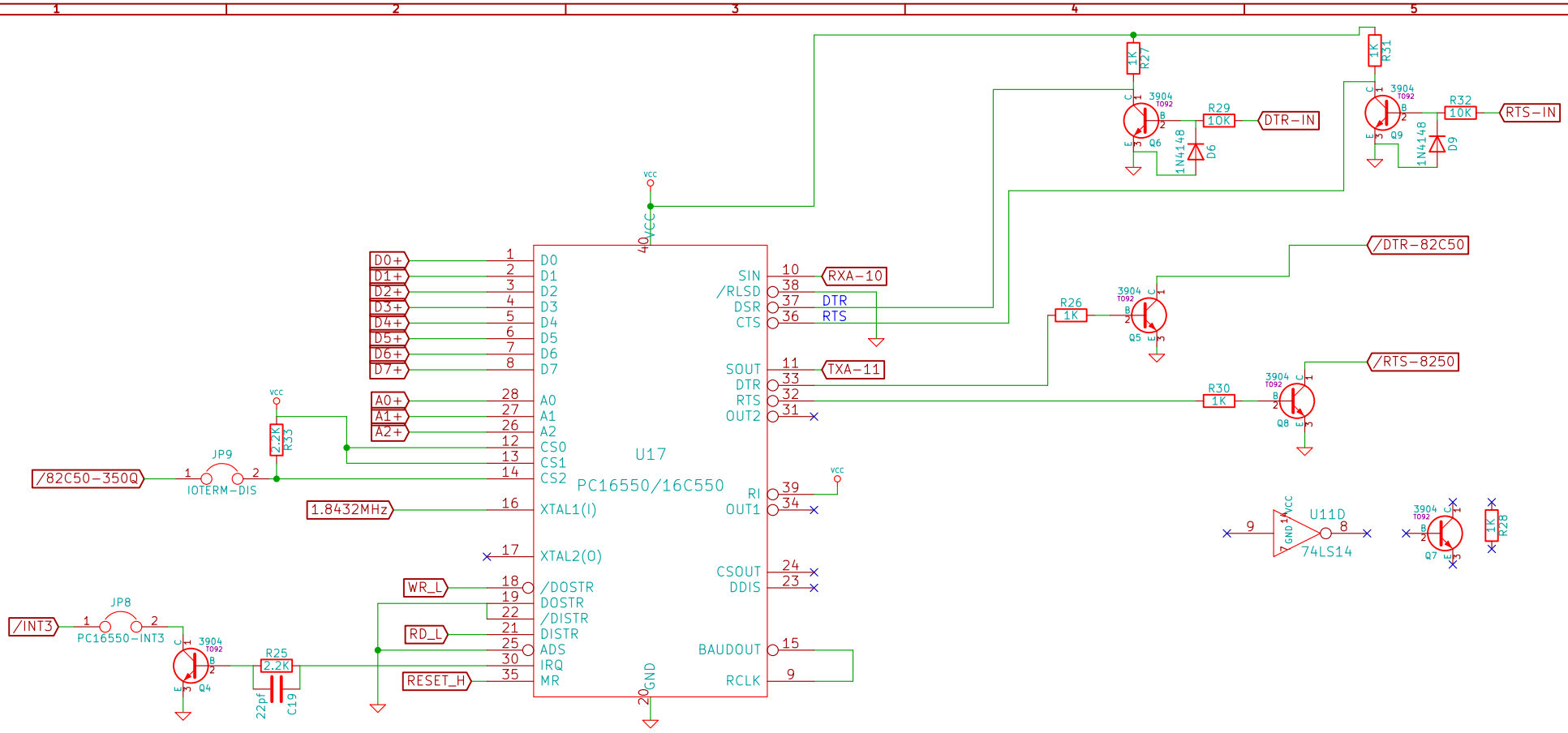
KOYADO.COM
File: CASSETTE_RECORDER_CONTROLLER.sch
Sheet: /H8-5/CASSETTE RECORDER/
Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE
Size: A4
Date: 8 feb 2026
Rev: 1.4
KiCad E.D.A.
Id: 5/6



Fix 16550 RS232 polarity.
Added /DTR /INT3 Software control to boot HDOS on 8251A IC.
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KOYADO.COM

File: 82C50.sch
Sheet: /H8-5/COM PORT/

Title: H8-Z5-4 CONSOLE CASSETTE/STORAGE INTERFACE

Size: A4	Date: 8 feb 2026	Rev: 1.4
KiCad E.D.A.		Id: 6/6