# DATA TECHNOLOGY CORPORATION MRX101D CONTROLLER SPECIFICATION FOR MEMOREX 101 DISK DRIVES

## January 13, 1981

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## 1.0 INTRODUCTION

The MRX101D Controller consists of a microprocessor-based controller with on-board data separator logic (for FDD), that is able to control a maximum of four disk drives. The controller has two disk drive interface ports. One port connects to the Memorex 101 type disk drives, and the other connects to floppy disk drives. The floppy drive I/O port works with industry standard single or dual head floppy disk drives. The floppy disk track formats are IBM 1D/2D compatible.

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Commands are issued to the controller over a bidirectional bus connected to the host computer. The data separator/"serdes" logic serializes bytes and converts to MFM data, and deserializes MFM data into 8-bit bytes for the double density floppy drives.

Due to the micro-programmed approach utilized in the controller, extensive diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media inperfections up to 4-bit burst errors on the Memorex 101 disk drives.

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# 2.0 MRX101D CONTROLLER

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# 2.1 Features of alleg neithologues and with the primary of the breaking and have

OVERLAPPED SEEK

In multiple drive configurations the host can issue seeks to different drives without waiting for the first drive to complete its seek.

SHOTOR BUTTONS

AUTOMATIC SEEK
A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.

FAULT DETECTION Two classes of faults are flagged to improve error handling:

- Controller faults
- Disk faults

AUTOMATIC HEAD and CYLINDER SWITCHING If, during a multi-block data transfer, the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.

DATA ERROR
DETECTION AND
CORRECTION

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If a data error is detected during a disk data transfer, the MRX101D will determine whether or not the error is correctable. If uncorrectable, the MRX101D will indicate this. If the error is correctable, either a pointer and mask can be requested by the host for applying the correction or the error can be automatically corrected by the MRX101D.

LOGICAL TO PHYSICAL UNIT CORRELATION Logical Unit Number (LUN's) are independent of physical port numbers. All accesses specify LUN's.

ON BOARD SECTOR BUFFER A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.

EFFICIENT HOST PROTOCOL

A bidirectional bus between the controller and host provides a simple, yet efficient communication path. In addition, a high level command set permits effective command initiation.

SECTOR INTERLEAVING

Sector interleaving is programmable up to 32 ways.

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**ODD PARITY** 

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The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.

NUMBER OF DRIVES

militare error bandanu

The controller will connect to a maximum of four (4) drives. The drives can be any combination of Memorex 101 and/or industry standard floppy disk drives.

BAD SECTOR/ WRITE-PROTECT SECTOR

A sector can be flagged as a bad sector or write-protected sector in the specified ID field. (Memorex 101 only)

TRACK FORMATS

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Memorex 101: NRZ

256 Bytes/Sector, 40 Sectors/Track

IBM 1D/2D: Track format for floppy disk drives can be selected under program control in real time. The track formats are:

1) Single-density, single-sided

2) Single-density, double-sided or silver all the side of the side

Double-density, single-sided and additional and a significant and

4) Double-density, double-sided

military than eath of button probatigmore have III Refer to Section 4.0 for details. I to recommend that

thing bad dilw materials in fall nottempore its and upor Kins

2.2 System Configuration

Refer to Figure 2-1. The controller and data separator comprise a single PCB. A maximum of (4) drives may be connected to the controller. The floppy control cable is connected to connector J9. The Memorex 101 control cable is connected to connected to either J2, J3, J4, or J5. Connector J6 is connected to the host interface board. All cables are the mass terminated type.

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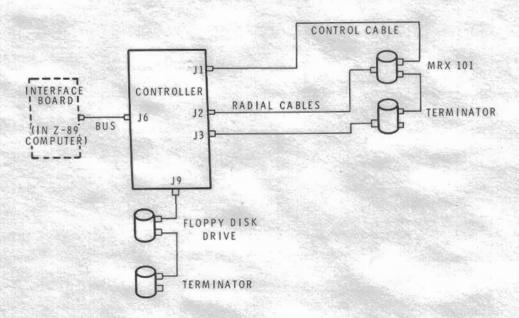


Figure 2-1

#### 2.3 Theory of Operation

SACTARIMES!

Disk commands are issued to the MRX101D via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (Command structure is described in Section 4.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

Memers 101 MRS

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send completion status to the host. (Further delineation of the completion status may be requested by issuing the appropriate sense commands.)

Odd parity is generated by the MRX101D for all information that it puts on the I/O bus. If enabled, the MRX101D flags all information that it receives with bad parity.

Saint to Figure 2.4. The controller and data superator of fifting the of age PCE of figure man, of (4) of

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#### 2.3.1 Electrical Interface

The electrical interface to the Memorex 101 drive will conform to the specification described in the Memorex 101 interface specification.

The electrical interface to the MRX101D Host Bus is described in the following sections.

Send status byte la-

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#### 3.0 MRX101D HOST BUS

The MRX101D Host Bus is a negative-logic, bidirectional, 8-bit data bus utilizing odd parity. The electrical interface consists of an open collector bus terminated on each end by a 220/300 ohm resistor network. The controller regulates transfers across the bus which eliminates data overruns that could occur during data transfers.

The term "asserted" means that the signal on the host bus is between 0 V and 0.8 V. The term "deasserted" means that the signal on the host bus is between 2.5 V and 3.5 V (negative or low true logic).

#### 3.1 Signal Definition See See Section 2017 (225) 201 (275) 1851 and 1857 2024

#### 3.1.1 Unidirectional Signals Driven By Controller

CONTRACTOR OF THE PARTY OF THE	
I/O	Input/Output. When asserted, the data on the bus is driven by the controller. When deasserted, the data on the bus is driven by the interface board. The interface board uses this line to enable its drivers onto the data bus.
C/D most sea	Command/Data. When asserted, the data transmitted across the bus are the command bytes. When deasserted, the data are the disk data bytes.
BUSY	This bit is asserted as a response to the SEL line from the interface board and to indicate that the host bus is currently in use.
MSG	Message. When asserted along with C/D and I/O, indicates that the command is completed. This bit is always followed with the assertion of REO.

controller waits 256 on for ALA return before their out

REQ

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**Request.** This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the H/A.

I/O	C/D	MSG	Meaning	
d	a	d	Get command from H/A	
d	d	d	Get data from H/A	
a	d	d	Send data to H/A	OF BIRTISM OF
a	a	d	Send status byte to H/A	
$\ldots a_{m}$	a	a a	Command done to H/A	She Not Cler Water

a=asserted, d=deasserted

#### 3.1.2 Unidirectional Signals Driven By Interface Board

ACK

Acknowledge This bit is asserted as a response to REQ from the controller. The timing requirements on this signal with respect to the data is described in REQuest section. ACK must be returned for each REQ assertion. Once REQ has been asserted, the

controller waits 256 µs for ACK return before timing out.

RST

Reset When asserted, this bit forces the controller to the beginning of its microcode.

Any error status request will result in invalid information after RST has been asserted.

All signals to the drives are deasserted. RST must be asserted for a minimum of 250 ns

and a maximum of 10 \mus.

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(183) in moltween out drive hoppilled avew hash tid and T. hetelog

SEL Select When asserted, it indicates the beginning of the command transaction. The H/A asserts SEL to gain the attention of the controller. The controller will return BUSY

This bir is asserted as a response to the ballbedrame that the first line is currently in some

within 1 µs.

#### 3.1.3 Bidirectional Data

DB (7-0,P) — Data lines 7 thru 0 represent the eight data bits. (DB0=1sb). Parity is represented by P. The controller utilizes odd parity (the number of asserted bits on the host bus is always odd).

#### 3.2 Theory of Operation

Whenever the interface board has a command for the controller, it performs a selection sequence to gain the attention of the controller. The sequence is as follows (refer to Figures 3-1, 3-2, and 3-3):

The interface board asserts SEL and DB0 (controller address bit) on the host bus. It then waits for the controller to respond with BUSY. Upon reception of BUSY, the interface board deasserts SEL. The controller now has control of the host bus.

After the controller asserts BUSY, it then asserts C/D to indicate command mode transfer, and deasserts I/O to indicate output and to fetch the command bytes from the interface board. The command bytes are transferred over the host bus with the REQ/ACK handshake protocol until all command bytes are transferred to the controller. (The command byte fetch mode ends after the last REQ pulse from the controller is deasserted.)

For data transfer, the controller deasserts the C/D line to indicate data mode. Depending on the command type (read/write disk) the I/O bit on the host bus is asserted or deasserted by the controller, and the data is transferred (a byte at a time) with the same REQ/ACK handshake protocol. After all the data bytes have been transferred, a completion status is placed on the data bus by the controller — C/D and I/O are asserted. REQ is asserted and the controller waits for ACK from the interface board. After the status byte transfer, the controller places zeros on the data bus and asserts C/D, I/O and MSG along with REQ to indicate to the host that the command is complete (this action can be used to generate an interrupt on the host system). After the interface board responds with ACK, the controller deasserts REQ, BUSY and all other lines. This completes the command execution and the controller is now ready to be selected for the next command.

#### **Timing Requirements for Controller Selection**

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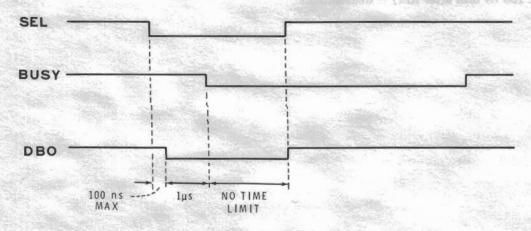
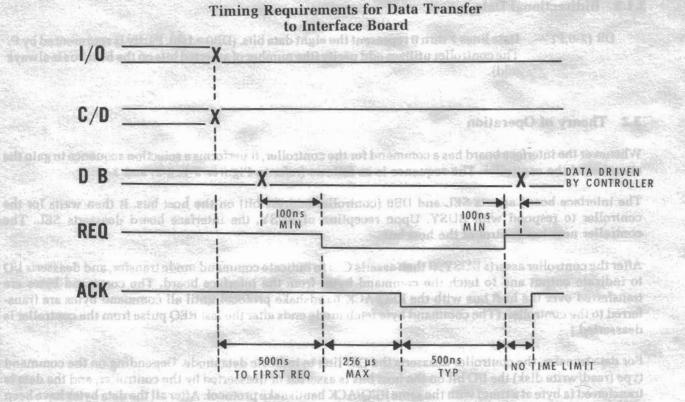


Figure 3-1

Note: SEL must be deasserted before the controller asserts REQ.

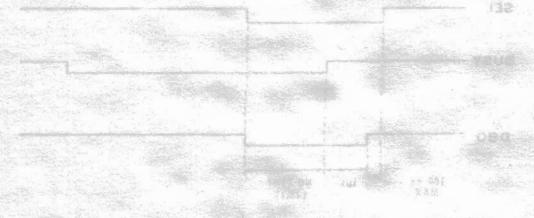


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Note 1: For Status Byte Transfer (I/O, C/D asserted and MSG deasserted); or Interrupt Byte Transfer (MSG, I/O, C/D asserted), REQ is asserted 500 ns (typical) after the assertion of any of the above bits.

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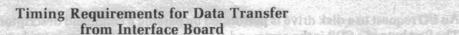
Data driven by the controller is stable 100 ns min at the interface board end before REQ is asserted, and 100 ns min after REQ is deasserted.



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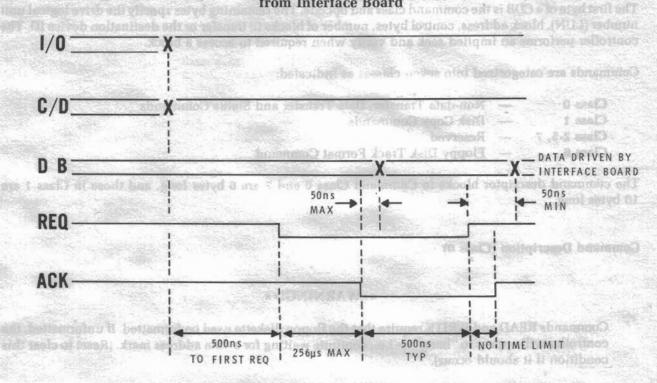


Figure 3-3

- Note 1: Data driven by the interface board is stable 50 ns max at the interface board end after ACK is asserted, and 50 ns min after REQ is deasserted.
  - 2: For command mode transfers, SEL must be deasserted before ACK is asserted. This sequence follows the selection protocol.

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#### 4.0 COMMANDS

An I/O request to a disk drive is performed by passing a command descriptor block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, number of blocks to transfer or the destination device ID. The controller performs an implied seek and verify when required to access a block.

Commands are categorized into seven classes as indicated:

Class 0 — Non-data Transfer, Data Transfer and Status Commands

Class 1 — Disk Copy Commands

Class 2-5, 7 — Reserved

Class 6 — Floppy Disk Track Format Command

The command descriptor blocks in Command Class 0 and 7 are 6 bytes long, and those in Class 1 are 10 bytes long.

#### Command Description (Class 0)

#### \*\*WARNING!\*\*

Commands READ and WRITE require that the floppy diskette used be formatted. If unformatted, the controller will appear to "hang" — i.e., continue waiting for a data address mark. (Reset to clear this condition if it should occur).

Opcode (Hex)	Description
00	Test drive ready. Selects the drive and verifies drive ready.
01	Recalibrate. Positions the R/W arm to Track 00, clears possible error status in the drive.
02	Request Syndrome. Returns the offset and syndrome for data field error correction. The two bytes are as follows:



The bit offset is relative from the first data bit, i.e., Bit 7 of Byte 0.

Request Sense. This command must be issued immediately after an error. It returns 4 bytes of drive and controller sense for the specified LUN. (See copy block for exception).

Format Drive. Formats all blocks with ID field according to interleave factor and data fields.

The data field contains E5 Hex.

05 Reserved.

06

Format Track. Formats the specified track with bad block flag cleared in all blocks of that track. Writes E5 Hex in the data fields.

Allege Commands

07	Format Bad Sector. Formats the specified sector ID with bad sector flag (Bit 7 in head byte) set.
08	Read. Reads the specified number of blocks starting from initial block address given in the CDB. (See Warning above!)
09	Write-protect the sector. Writes the specified sector ID field with write-protected flag. (Bit 6 in head byte) set. (See Warning above!)
0A	Write. Writes the specified number of blocks starting from initial block address given in the CDB.
ов	Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drive's capable of overlap seek.

### **Command Description (Class 1)**

Opcode (Hex)	Description	a de la companya de l
00	Copy Block. Co	pies the number of sectors from the source drive to the destination drive.

#### Command Description (Class 6)

Opcode	Description
(Hex)	

00

Define Floppy Disk Track Format. The Track format code in byte 5 of the CDB defines the track format for the LUN. The Track Format Codes are as follows:

Track Format Code (Hex)	Track Format Description
00	Single-density, single-sided. All tracks — FM recording, 128 bytes/sector, 26 sectors/track.
01	Single-density, double-sided. All tracks — FM recording, 128 bytes/sector, 26 sectors/track.
06	Double-density, single-sided. Side 0, cylinder 0 — FM recording. 128 bytes/sector, 26 sectors/track. All other tracks — MFM recording, 256 bytes/sector, 26 sectors/track.
07	Double-density, double-sided. Side 0, cylinder 0 — FM recording, 128 bytes/sector, 26 sectors/track. All other tracks — MFM recording, 256 bytes/sector, 26 sectors/track.

NOTE: If track format information for floppy is not specified after each reset or power-on, the default mode will be as follows:

Switch Setting	Mode with any side should be of
10 (dual-head FDD)	Single-density, single-sided (same as track format code 00)
11 (single-head FDD)	Single-density, single-sided (same as track format code 00)

limit, initializa seek, to apecified block and inmultimally returns complete on status balons that

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Refer to Appendix C, "Switch Set-up Instructions", to set up the switches.

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Comment Description (Class 1)

Charinand Description (Classic

Track Format Castle

#### 4.1 Command Format

#### 4.1.1 Class 0 Commands

Byte	7 6 5 4 3 2 1 0	
0	0 0 0 opcode	Description of
1	LUN logical adr2*	Copy Black, On
2	logical adr1*	
3	logical adr0*	
4	number of blocks	is sest.) philipin
5	control	AND PARTY.
	Control of the Contro	and the same of th

<sup>\*</sup> Refer to section 4.3 for Logical Address Computation LUN = Logical Unit Number for the drive — 0, 1, 2, or 3.

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LOGICAL ADR (0-2)

= Logical Sector Address of specified sector. LOGICAL ADR0 is the LSB. Sectors start at zero (cy1=head=sector=0). After the end of the track is reached, the next logical sector is located on the next track. If the end of the cylinder is reached, the next logical sector is located on the first track on the next cylinder.

NUMBER OF BLOCKS

= Contains the number of blocks (sectors) to transfer per command. Also indicates the Interleave factor for Format, Check Track commands only.

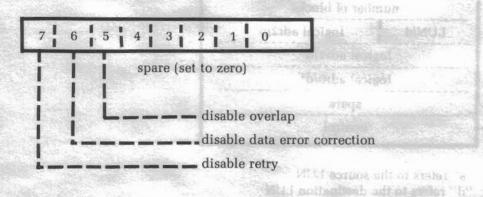
Congresseds in this group

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Track Fornest Cade"

us 6 Command

CONTROL BYTE is defined as follows:



#### Commands in this group

- a) NOP
- b) Format Drive
- c) Check Format
- d) Request Sense
- e) Request Syndrome
- f) Recalibrate
- g) Read Block(s)
- h) Write Protect Sector
- i) Write Block(s)
- i) Format Track
- k) Format Bad Sector
- l) Seek

#### 4.1.2 Class 1 Commands

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7	6	5	4	3	2	1	0
0	0	1		(	pcod	е	milyo d
last d	LUN/	S	Maria C	logic	al ad	r2/s*	l entrin
Ched		lo	gical	adr1	/s*		10000
		lo	gical	adr0	s*		Savetil
		nu	mber	of blo	ocks		
1	LUN/	d		logic	cal ad	r2/d*	3.1
		lo	gical	adr1	d*		
		lo	gical	adr0	d*		
4.00	717		sp	are			
			COI	ntrol		013001	
	     	0 0 LUN/	0 0 1  LUN/s  lo  nu  LUN/d	0 0 1  LUN/s  logical  logical  number  LUN/d  logical  logical  sp	0 0 1 logical adr1, logical adr0, number of blo logical adr1, logical adr1, logical adr1, logical adr1,	0 0 1 opcod  LUN/s logical ad  logical adr1/s*  logical adr0/s*  number of blocks  LUN/d logical adr1/d*  logical adr0/d*  spare	0 0 1 opcode  LUN/s logical adr2/s*  logical adr1/s*  logical adr0/s*  number of blocks  LUN/d logical adr2/d*  logical adr1/d*  logical adr0/d*  spare

<sup>&</sup>quot;s" refers to the source LUN

#### Commands in this group

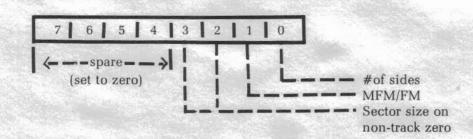
a) Copy Block

#### 4.1.3 Class 6 Commands



NOTE: See Class 6 Command Description for more information and default modes for floppy drives.

<sup>\*</sup>Track Format Code byte is defined as follows:



<sup>&</sup>quot;d" refers to the destination LUN

<sup>\*</sup>Refer to section 4.3 for Logical Address Computation

#### 4.2 Status Format

#### 4.2.1 Completion Status Byte



Bit 0 Parity error during transfer from host to controller.

Bit 1 Error occurred during command execution.

Bit 2-4 Spare (set to zero).

Bit 5-7 Logical unit number of the drive.

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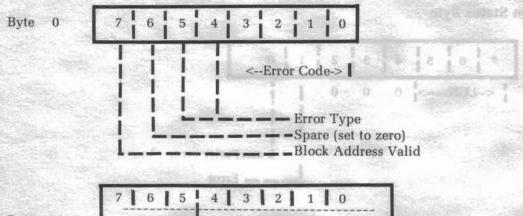
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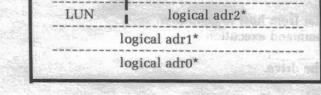
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#### 4.2.2 Drive and Controller Sense



Byte 1 2

3



\*Refer to section for Logical Address Computation

Block Address Valid — Indicates that the Logical Sector Address in bytes 1 thru 3 contain the block at which the error occurred.

WHITTH REPORT WHITE

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Error Type — Indicates the general type of error.

Error Code — The actual error interpretation.

LUN — The Logical Unit Number of the erring drive.

#### 4.3 Logical Address Computation

The Logical address is computed as follows:

Logical adr = (CYADR \* HDCYL + HDADR) \* SETRK + SEADR (see note)

Where: CYADR = cylinder address

HDADR = head address

SEADR = sector address

HDCYL = number of heads per cylinder SETRK = number of sectors per track

Bit 0 of Logical adr0 = the least significant bit.

Bit 4 of Logical adr2 = the most significant bit.

NOTE: SEADR = (SEADR - 1) for IBM track format.

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#### 4.4 ERROR CODE TABLE

#### Type 0 (Drive) Error Codes

- 0 No status
  1 No index signal
  2 No seek complete
  3 Write fault
- Write fault
  Drive not ready
  Drive not selected.
- 6 No Track 00

#### Type 1 (Controller) Error Codes

- 0 ID read error. ECC error in the ID field.
- 1 Uncorrectable data error during a read.
- 2 ID Address Mark not found.
- 3 Data Address Mark not found.
- 4 Record not found. Found correct cylinder and head but not sector.
- 5 Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
- 6 DMA Data time out error. No acknowledge within 256 μs.
- 7 Write protected.
- 8 Correctable data field error.
- 9 Bad block found.
- A Format Error. The controller detected that during the Check Track command, the format on the drive was not as expected.

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#### Type 2 (Command) Error Codes

- Invalid Command received from the host.
- 1 Illegal disk address. Address is beyond the maximum address.
- 2 Illegal function for the specified drive.
  - e.g. Check Track command does not apply for floppy disks with IBM track format.

#### 5.0 ELECTRICAL/MECHANICAL SPECIFICATION

#### **Physical Parameters**

Width	8.5 inches
Length	13.5 inches
Height	0.49 inches
Weight	1.12 lbs.

#### **Environmental Parameters**

Temp. (degree) F/C	Operating 32/0 to 131/55	Storage -40/-10 to 167/75
Relative Humidity (@ 40 degrees F, wet bulb temp no condensation)	10% to 95%	10% to 95%
Altitude	sea level to 10K feet	sea level to 15K feet

#### **Power Requirements**

Methe protected.

Correctable data field

Voltage @ current	+5 VDC @ 4.6A (max)
	-5 VDC @ 500 mA (max)
	+24 VDC @ 100 mA (max)

#### 6.0 DIAGNOSTIC PHILOSOPHY

The controller contains 8 diagnostic LED error indicators. Each time an error occurs the controller deposits a value in the LEDs and returns a failure status to the host adaptor. The LED value can be decoded, but the error it indicates will be available to the host software. The errors that are returned by the controller is very detailed. As a result preliminary fault isolation is made fairly easily, narrowing the failure to the particular interface portion of the controller.

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#### APPENDIX A

#### **MEMOREX 101 SECTOR FORMAT**

Usage

MOTE All signate are significantly and all and pice are commented to ground. The signal three

The track layout for the Memorex 101 (typical for 40 sectors) is shown below.

11	S	C	h	S	e	е	е	14	S	256	e	e	e	6
bytes	У	У	d	е	C	C	C	bytes	у	256 bytes data	C	C	C	bytes
00's	n	1		C	C	C	C	00's	n	data	С	С	C	00's
	C	533		- 17	2	1	0		C		12	1	0	

sync, cyl, hd, sec, 00, ecc0, ecc1, ecc2 = 1 byte

Track Capacity = 12000 bytes

298 bytes/sector

Number of cylinders = 243

Number of heads = 4

Number of drives = one, any drive select value

Step Rate (buffered mode) =  $100 \mu s$  period

Head Settling Time (after Seek Complete) = 25 ms

#### APPENDIX B HOST I/O CONNECTOR PIN ASSIGNMENT

The Host I/O Bus uses a 50-pin connector (AMP P/N 2-87227-5 or equivalent). The unused signal pins are considered to be spares for future use. The pin assignments are as follows:—

	Delia contrata de la contrata del contrata del contrata de la contrata del la contrata de la contrata del la contrata de la co		
Signal	Pin Number	all merchants as	Intelescendentals in
	autyd au 191		
DATA0	4 00 4 3	1 Mar 1 1 2 2 2 100	
DATA1	4		
DATA2	6		
DATA3	8		
DATA4	10		
DATA5	12		
DATA6	14	alvd.f	
DATA7	16		
PARITY	18		Track Capacity = 12300 bytes
	20		
-	22		The second secon
	24		
	26	Future	THE REAL PROPERTY OF THE PROPERTY OF
	28	Usage	
	30		F = absed to wide. A
	32		
AND CALLES	34		Number of drives - our day drive sales
BUSY	36		
ACK	38		ring the Office Inhom benefit and anti-
RST	40		
TDN	42	和野湖 二十	Hand Southing Plate 1996; Sook Consplate
SEL	44		
C/D	46		
REQ	48		
I/O	50		

NOTE: All signals are negative-true, and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5 V and 330 ohms to ground.

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0 - C - disable giggly

A - 9 - enable odd partty ab

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#### APPENDIX C

#### PROM SET AND SWITCH DEFINITION

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Prom Set AM12

CUSTOMER FIRMWARE: (DIP SWITCH set-up procedure)

Location: 16B

Switch Bits

Field

Definition

8 7	6 5	4 3	2 1
LUN 0	LUN 1	LUN 2	LUN 3
Drive	Drive	Drive	Drive
Type	Type	Type	Type

- 1. All FDD-100-8 drives are 26 sectored/track @128 bytes/sector (FM).
- All FDD-200-8 drives are 26 sectors/track @128 bytes/sector (FM) for track 00, and 26 sectors @256 bytes all others.

#### Example:

Location: 16B

8 7	6 5	4 3	2 1
LUN 0 Drive Type	LUN 1 Drive Type	LUN 2 Drive Type	LUN 3 Drive Type
on on	off on	off off	on on

Drive 0 is set up for Memorex 101

Drive 1 is set up for FDD-200-8

Drive 2 is set up for (FDD-100-8) (FM only)

Drive 3 is set up for Memorex 101

#### APPENDIX D MRX101D CONTROLLER POWER CONNECTIONS

- 1) +24 V @ 100 mA
- 2) Gnd
- 3) Gnd
- 4) -5 V @ 500 mA

\*\*Warning!\*\*

The Controller can only accept -5 V. No provisions have been made for other voltages on this pin.

- 5) +5 V @ 4.6 A
- 6) Gnd

PARITY JUMPER SETTING

APPENDIX E

Parity jumper W1 at location 6D:

A-B = enable odd parity checking and generation

B-C = disable parity

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All-Pint rolls diese ere 25 section and 6712 on discour (End) for frest 80, and 35 sectors

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#### APPENDIX F

#### ERROR DISPLAY IN LEDS

Once the controller detects an error, the error display maintains the error indication even though subsequent tests are performed correctly. In this way the controller can be left running for a long period of time. However, only the last error is displayed on the LED's. To reset the error display, stop the test and start again.

The table below lists the error indications as displayed by the controller.



Error Code (HEX, DS0 is LSB)	Interpretation
00	No error
01	No Index from drive
02	No Track 00 from drive
03	Sector Address Out of Bounds
04	Hard Disk not selected
05	No Seek Complete from Hard Disk
06	No ID Address Mark
07	No Data Address Mark
08	Seek Error (Cylinder or Head not correct)
09	Sector not found
0A	ID ECC error
OB	No ACK from Host Adaptor
0C	Invalid Command (controller will only accept 5 bytes of the command).
0D	Incorrect DATA MARK
0E	Incorrect ID MARK
0F	Incorrect cylinder address from drive
10	Incorrect sector address from drive
11	Incorrect head address from drive
12	Uncorrectable Data Error
13	Correctable Data Error
14	Drive not READY
15	Write fault
16	not used
17	Drive write protected
18	RAM diagnostic error
19 — 1F	not used
20	Parity Error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad Block detected from drive
22	Invalid function for this type
81	Fatal Error Code. Controller detected more than one Seek Complete signal asserted on the drive interface to the Memorex 101. Only "RESET" from the host cable will clear this condition. The controller will ignore all commands after detecting this error.