Issue: Enabling I/O Wait States Generator on SSI or HA-8-3-1 boards.

Delayed BWR_L signal circuit produces multiple write pulses in a given machine instruction cycle when used with any device that inserts I/O wait states. That includes the SSI board or the HA-8-3-1 board with the I/O wait state generator enabled, as well as the Trionyx Z-H8 CPU.

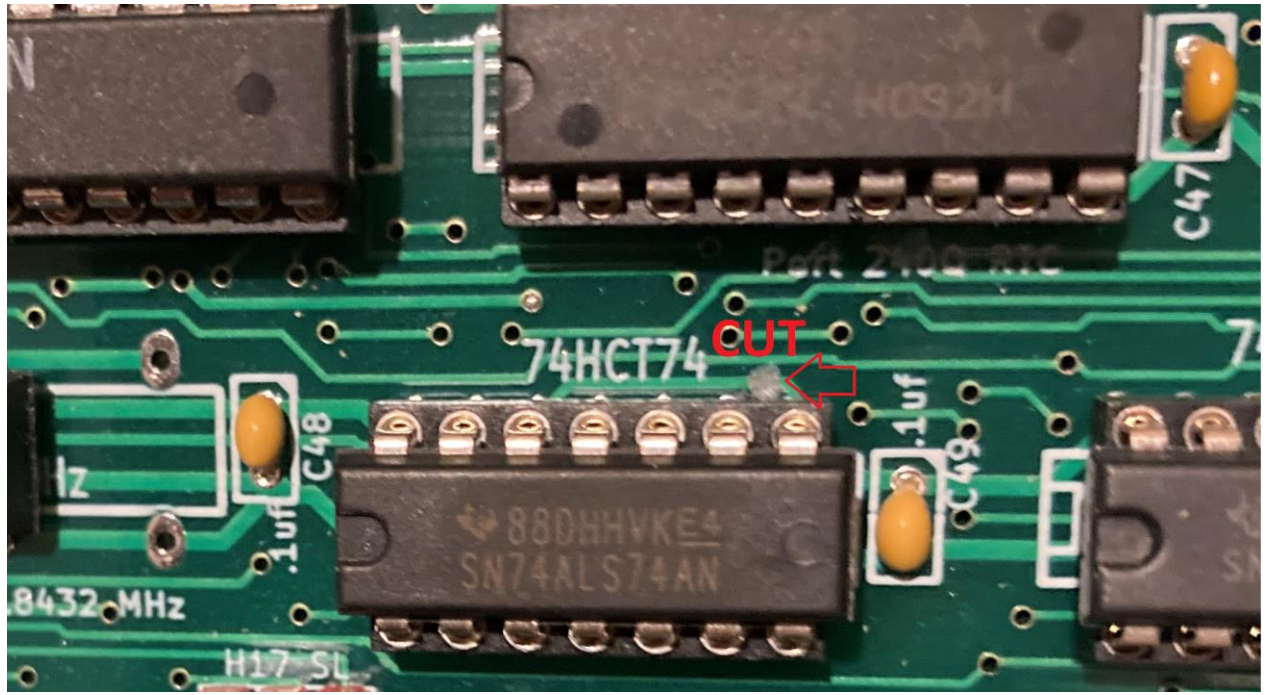
This affects the following boards:

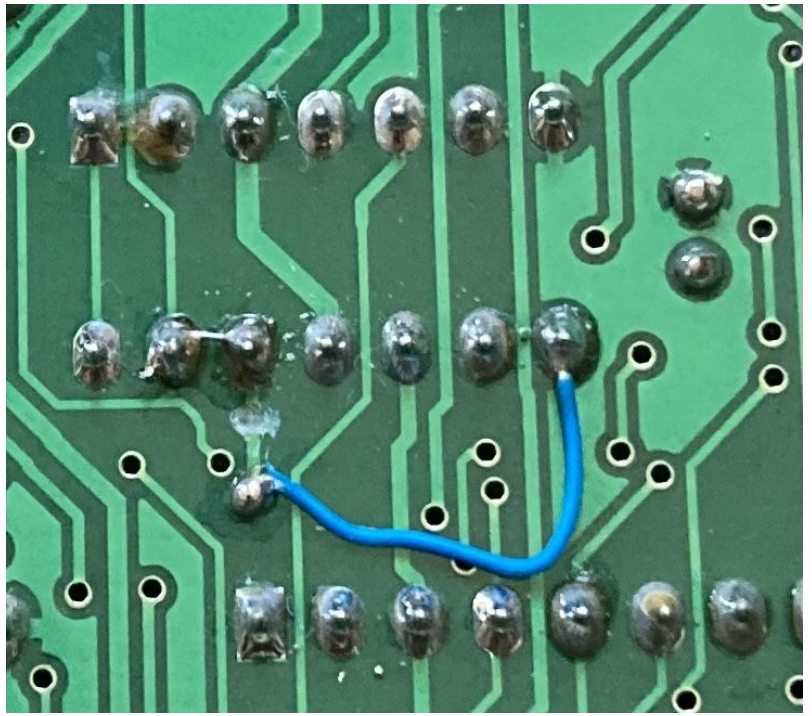
- H17/H37/67 combo boards
- Z80 V3.x board
- Z80 V4.x board

Once reworks has been applied, the H8 system can run smoothly at 16MHz with the I/O Wait State Generator enabled.

Z80 V3.x rework:

- ✓ Cut trace between pins 8-12 on U112 side 1.
- ✓ On IC U112 side 2 bridge pins 12-13.
- ✓ On IC U112 side 2 cut trace on pin 12 as shown.
- ✓ On IC U112 side 2 solder wire from pin 8 to via as shown. Clean via so that it is easy to solder.



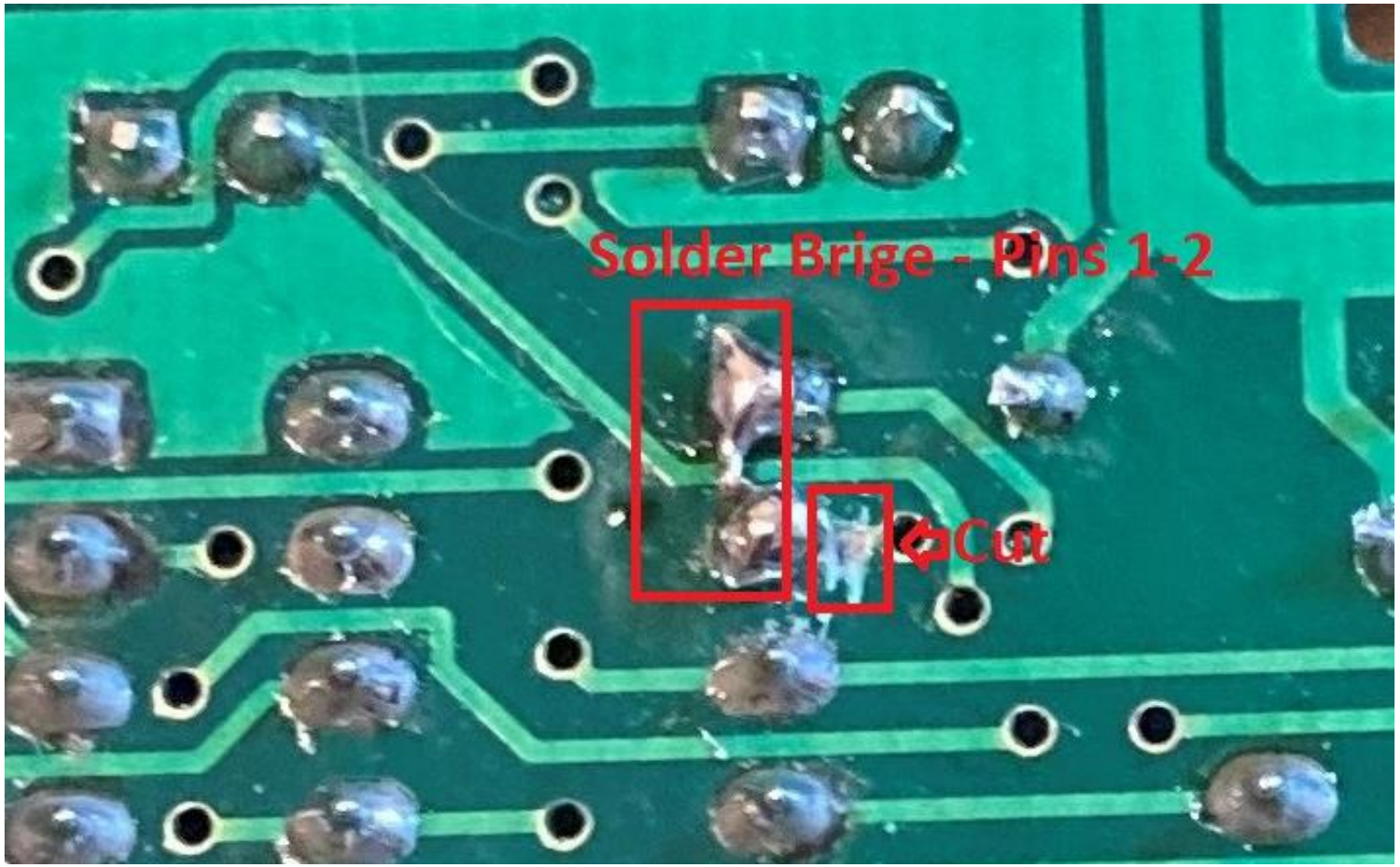


Z80 V4.0 rework:

- ✓ On JP25, insert jumper between pins 2-3 to bypass U112.

H17 Combo board rework:

- ✓ On IC U25 bridge pins 1-2 on side 2.
- ✓ Cut trace between pins 2-6 on side 2.



H37/H67 Combo board rework:

- ✓ On IC U40 bridge pins 1-2 on side 2.
- ✓ Cut trace on pins 2-6 on side 2.