HEATH

Schlumberger

Service Data Manual

H/WH19

VIDEO TERMINAL

H/WH19 VIDEO TERMINAL

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HEATH ZENITH

THE TECHNICAL EXCHANGE

Issue #78
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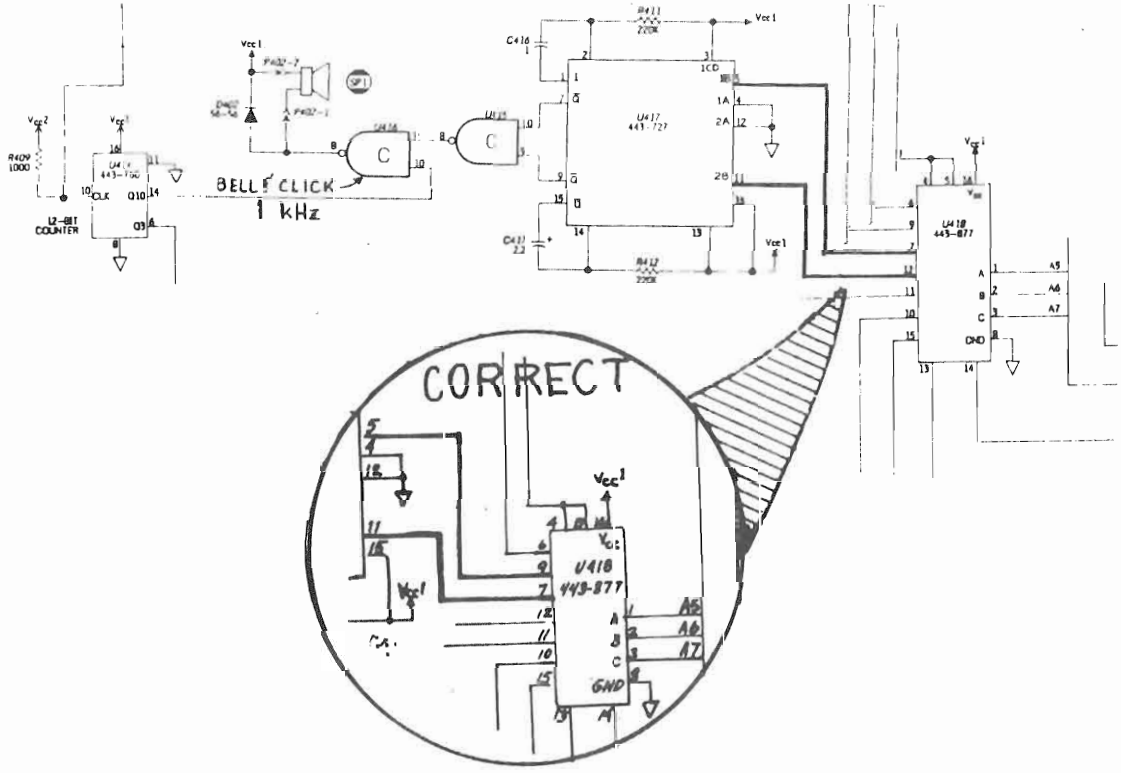
SUBJECT: H/WH19 Service Data Manual/Schematic Revisions

Please revise your H/WH19 Blue Book and schematic as follows:

Page 62, When the CPU wants to ring the bell, it bring U418, pin 7 to .....

Correct pictorial as shown:



Page 100, *from* ... (D101/D102 and D103/D104 respectively)..."

to ... (D103/D104 and D101/D102 respectively)..."

continued...

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Page 119, Circuit Component Location view;

Page 334, Parts List; and

Pages 338 and 339, Terminal Logic Board X-Ray views:

U473 *from* #444-37 *to* #444-29
U430 *from* #444-29 *to* #444-37

Also on page 334, under Miscellaneous:

ADD: Terminal Logic Board, wired #181-3043

Video Terminal Schematic, Video board:

At the emitter Q213, *ADD:* +55.3 volts.

Thank you,
Service Publications and Training

T.Hogben, Factory (TSI-25 ww)

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INTRODUCTION

The Heath Model H19 Video Terminal is a professional 24-line (with a programmable 25th line) video terminal. Not only does it have the features commonly found in other high-quality video terminals, but it also has many exclusive features. The terminal will connect to other equipment that uses an EIA RS-232C serial interface; and the high-quality keyboard, video display, and state-of-the-art logic circuitry make this video terminal an outstanding peripheral for a computer or MODEM.

The information is displayed on a 12" (diagonal) cathode-ray tube that is capable of displaying up to 2000 characters at one time (25 rows of 80 characters). Well-designed video and sweep circuits, along with the P4 phosphor used in the CRT, provide superb character definition. Upper-case characters are formed by a 5 x 7 dot matrix. Lower-chase characters that have descenders use a 5 x 9 dot matrix. The Terminal can also display 33 special graphic characters that can be arranged and grouped to form any number of graphic displays and effects. The graphic symbols are formed on a 8 x 10 dot matrix.

Special local and software controllable Escape sequences allow you to select and use many special functions. These include:

- Using either Heath or ANSI Escape sequences.
- Eight user-defined speical function keys.
- Automatic scrolling, by line or by page (24 lines).
- Cursor control (left, right, up, down, home).
- Direct cursor addressing.
- Transmit page.
- Transmit 25th line.
- Insert and delete characters and lines.
- Enter and exit the graphics and reverse video modes.
- Mix graphics with characters.
- Erase lines or page of text.
- Modify baud rates.

The highly reliable, standard-size electronic keyboard uses the universally accepted, standard typewriter format. Each key stroke is affirmed by an audible key click (defeatable).

The 12-key keypad duplicates the numeric keys in a calculator format. This lets you rapidly enter numbers in programs that call for just numbers. In addition, the shifted keypad functions allow you to insert and delete lines and characters, and move the cursor. Plus, an alternate mode allows you to interchange the shifted and unshifted functions and send special codes to your computer.

SPECIFICATIONS

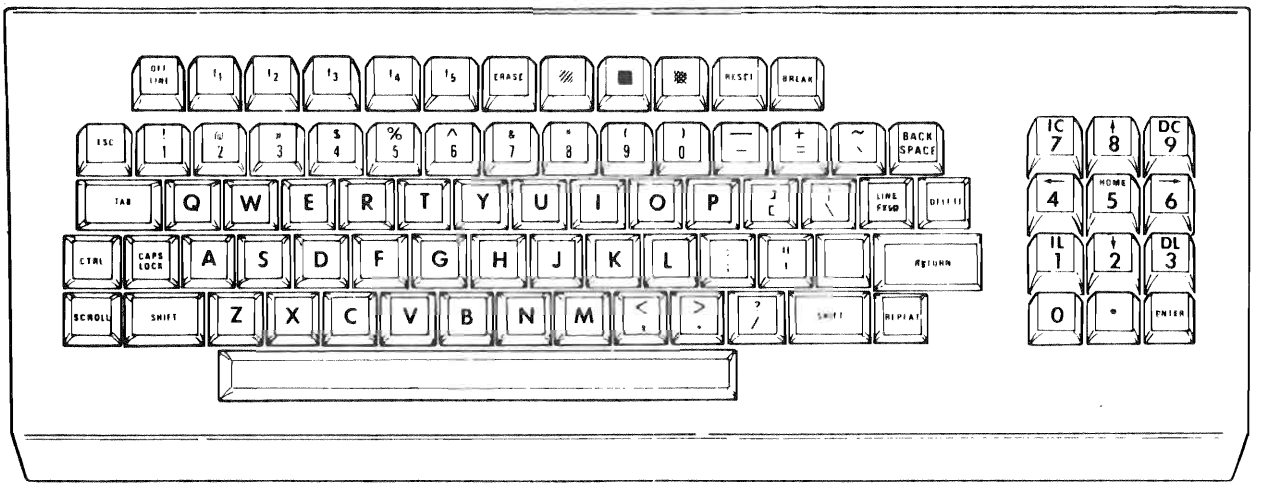
CRT	12" diagonal, P4 phosphor.
Display Format	24 lines of 80 characters.
Display Size	6.5" H x 8.5" W.
Character Size	0.2" H x 0.1" W (approximate).
Character Set	128 characters (95 ASCII and 33 graphic.
Character Type	5 x 7 dot matrix (upper case), 5 x 9 dot matrix (lower case with descenders).
Keyboard	84 keys (60 alphanumeric, 12 function/ control) plus a 12-key numeric pad.
Cursor	Blinking, nondestructive underline.
Cursor Controls	Up, Down. Left, Right, Home, CR, LF, Back Space, and TAB.
Cursor Addressing	Relative and direct.
Tab	Standard 8-column tab.
Refresh Rate	60 Hz at 60 Hz line frequency; 50 Hz at 50 Hz line frequency.
Edit Functions	Insert and delete character or line.
Erase Functions	Erase page, erase to end of line, and erase to end of page.

Scroll	Auto or line/page freeze.
Bell	Audible alarm on receipt of ASCII BEL.
Video	Normal and reverse by character.
Interface	EIA RS-232C at 110 to 9600 baud.
Communications Mode	Full or half duplex.
Parity	Even, odd, stick, or none.
Operating Temperature	0-40 degrees Celsius ambient.
Power Requirements	120 VAC (105-135 VAC), 50/60 Hz, 45 watts, 240 VAC (210-270 VAC), 50/60 Hz, 45 watts.
Dimensions	13" H x 17" W x 20" D (33 x 43.2 x 50.8 cm).
Weight	45 lbs. (20.4 Kg).

OPERATION

Because of the large number of modes available on the H19 Video Terminal, only the more common functions necessary to gain a basic understanding of the operation will be covered here. For complete operating information, refer to the H19 Operations Manual (#595-2284) or the WH19 manual (#595-2192).

The Power ON/OFF switch is located on the right rear corner of the back panel. When the Terminal is turned on, it will beep once and in about 30 seconds, a cursor (underline or block) will appear in the upper left-hand corner of the screen.



H19 Video Terminal Keyboard

The keyboard allows the user to send data to the computer or the CRT. Most of the keys are the same as found on most typewriters. A clicking sound indicates that each keystroke has been processed by the H19 Terminal.

When the terminal is on line, the keyboard can transmit any one of the 128 ASCII characters to the computer. Not all characters are displayable, however.

In the off-line mode, the keyboard is effectively disconnected from the computer and controls the screen directly. This way, the cursor can be positioned, the screen can be erased, or the characters can be manipulated without sending the associated code back to the computer and disrupting a program. Another way of controlling the screen without sending code to the computer is to use the CTRL key. Holding this key down while positioning the cursor (for example) will prevent anything from being sent to the remote device.

Note that if any of the escape codes are used, the lower and upper case letters must be entered just as they are called for in the escape code listing. See the H19 Operations manual (#595-2284) for a detailed listing of the escape codes.

The H19 Terminal has a 128-byte buffer for receiving and holding characters until the Terminal can process them. In some cases, this FIFO buffer can be filled faster than the Terminal can process the characters. In this case, the Terminal will send a *control S* to the external device when the buffer has received 112 characters. After the buffer has emptied down to 96 characters, the Terminal will send a *control Q* to tell the computer to start transmitting again. If the external device is not programmed to respond to *control S*, the buffer will continue to load until all 128 locations are filled. At this time the bell will sound and any more incoming characters will be lost.

NORMAL MODES AND KEYS

Alphabetic Keys: The Terminal has the standard 26 letters of the alphabet. These keys can transmit either lower-case or upper-case codes, as well as display them on the screen. Holding either the SHIFT key down or pushing the CAPS LOCK key will obtain upper-case letters.

Nonalphabetic Keys: The nonalphabetic keys are those with double markings. These include the numbers Ø through 9, punctuation marks, and special characters. The lower marking is generated when both of the SHIFT keys are released, while the upper marking is generated when either or both SHIFT keys are held down. The CAPS LOCK key will not shift these keys.

Miscellaneous:

Return: Moves the cursor to the first character position of the line that it is currently in. If the cursor is already at the first character position, it remains there. RETURN is a nondisplayable character.

Line Feed: Moves the cursor down one line. LINE FEED is a nondisplayable character. If the cursor is at the bottom line, a LINE FEED causes it to remain there, but all of the data on the screen moves up one line. Data on the top line is lost as it is shifted up and off the screen.

Space Bar: Causes the cursor to move one character position to the right. A SPACE is a nondisplayable character. If the SPACE BAR is typed when the cursor is positioned below a displayed character, the character is replaced by a space and

the cursor moves one character position to the right. If the SPACE BAR is typed when the cursor is at the right end of a line, the cursor will remain there since neither a carriage return nor a line feed is generated.

Back Space: Moves the cursor one space to the left. If the cursor is at the start (left end) of a line, it will not move when a BACK SPACE is typed.

Delete: Transmits the ASCII code 177. It is a nondisplayable character.

Tab: Software controlled to move the cursor to the next tab stop (eight character spaces) to the right. The tab stops are fixed at 9, 17, 25, 33, 41, 49, 57, 65, and 73. If the cursor is at character position 73 through 79, it will only move one character position to the right when the TAB key is typed. Unless the wrap-around feature has been selected, the cursor will not tab from position 80.

ESC (Escape): A nondisplayable character that transmits the ACII code 033. This key is used in combination with other keys to enter and exit special moces.*

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*See the H19 Operations Manual (#595-2284) for a detailed listing of the Escape sequences.

Repeat: Holding this key in, along with another key, it will repeat the function of the other key as long as both keys are held down. The repeat rate is approximately 15 characters per second. However, if the baud rate that has been selected is less than the repeat rate, the repeat function will operate at a slower rate.

Shift: When this key is used in conjunction with another key, the character printed on the upper portion of that key will be displayed. An alphabetic key will display an upper case character.

Caps Lock: When this latching key is down, the Terminal will transmit the ASCII code for upper-case (capital) alphabetic letters. The upper-case letter will also be displayed on the screen. It does not shift the keys with the double markings.

Off Line: When this latching key is down, the Terminal is inhibited from transmitting or receiving data. However, all displayable characters will appear on the screen and any control codes that the Terminal can process will be processed.

Break: Typing this key will generate a continuous space at the output of the Terminal. It is generally used to tell the computer to interrupt execution.

Reset: Pressing this key and the right-hand shift key will hardware-reset the H19 Terminal to its preset condition. It exits all Escape modes and resets the baud rate to the rate selected by the switches on the Terminal Logic circuit board. To use this key, press the right-hand SHIFT key and the RESET key at the same time. This two-key combination prevents inadvertent reset.

Scroll: When this is used with Heath software in the Hold Screen mode, typing the SCROLL key will instruct the Terminal to display another line of information onto the screen. Use the SHIFT SCROLL to display another 24 lines of information onto the screen.

Control Key: The CTRL key is held down in conjunction with other keys to send the 32 ASCII control codes to the computer. The control keys are nondisplayable characters. The Terminal responds to only seven of the control characters from the keyboard or from the serial input port. These seven characters are:

Bell (BEL or CTRL G): Causes the Terminal to sound an audible tone through an internal speaker.

Back Space (BS or CTRL H): Duplicates the BACK SPACE key.

Horizontal Tab (HT or CTRL I): Duplicates the TAB key.

Line Feed (LF or CTRL J): Duplicates the LINE FEED key.

Carriage Return (CR or CTRL M): Duplicates the RETURN key.

Escape (ESC or CTRL [): Duplicates the ESC key.

SPECIAL MODES AND KEYS

Due to the large number of special functions available, only the more common ones will be presented here. Refer to the H19 Operation manual for complete listing of all available functions.

Cursor Functions

Cursor Home-ESC H -[Shift 5 (Home) of keypad]

Moves the cursor to the first character position on the first line (home).

Cursor Forward - ESC C -[Shift 6 (→) of keypad]

Moves the cursor one character position to the right. If the cursor is at the end of the line, it will remain there.

Cursor Backward - ESC D -[Shift 4 (←) of keypad]

Moves the cursone one character position to the left (backspaces). If the cursor is at the end (left end) of a line, it will remain there.

Cursor Down - ESC B -[Shift 2 (↓) of keypad]

Moves the cursor down one line. If the cursor is at the bottom line, it will remain there; however, a scroll will not occur.

Cursor Up - ESC A -[Shift 8 (↑) of keypad]

Moves the cursor up one line. If the cursor is at the top line, it will remain there; however, a scroll will not occur.

Insert Line - ESC L [Shift 1 (IL) of keypad]

Inserts a new blank line by moving the line that the cursor is on, and all following lines , down one line. Then the cursor is moved to the beginning of the blank line.

Delete Line - ESC M [Shift 3 (DL) of keypad]

Deletes the contents of the line that the cursor is on, places the cursor at the beginning of the line, moves all the folllowing lines up one line, and adds a blank line at line 24.

Delete Character - ESC N (Shift 9 (DC) of keypad)

Deletes the character at the cursor position and shifts any existing text that is to the right of the cursor, and on the same line, one character position to the left.

Enter Insert Character Mode -[ESC @ Shift 7 (IC) of keypad)

Lets you insert characters or words into text already displayed on the screen. The first time you type IC, the Terminal enters the Insert Character mode. You can then use the cursor controls to place the cursor at the point where you want to insert characters. As you type in the desired characters, any existing text directly above and to the right of the cursor is shifted to the right. This feature lets you add letters or words to existing text without having to retype the whole text. When you finish inserting characters, type IC again to exit the Insert Character mode. The Terminal transmits and ESC@ to enter, and an ESC O to exit the Insert Character mode.

Exit Insert Character Mode - ESC O

Exits the insert Character mode. (See Enter Insert Character mode above.)

Special Function Keys

The eight special function keys (f_1, f_2, f_3, f_4, f_5, Blue, Red, and Gray), on the top row of the keyboard, transmit two-character escape codes to the computer. The operator can define the meanings of each of these keys to suit their particular application (the software program must recognize the particular escape codes associated with the keys).

SUMMARY OF HEATH ESCAPE SEQUENCES*

Escape Sequence	Mnemonic	Definition
CURSOR FUNCTIONS		
ESC H	HCUH	Cursor home
ESC C	HCUF	Cursor foward
ESC D	HCUB	Cursor backward
ESC B	HCUD	Cursor down
ESC A	HCUU	Cursor up
ESC I	HRI	Reverse index
ESC n	HCPR	Cursor position report
ESC j	HSCP	Save cursor position
ESC k	HRCP	Set cursor to previously saved position
ESC Y	HDCA	Direct cursor addressing (same as VT52)
ERASING AND EDITING		
ESC E	HCD	Clear display (shift erase)
ESC b	HBD	Erase beginning of display
ESC J	HEOP	Erase to end of page (Erase key)
ESC !	HEL	Erase entire line
ESC o	HEBL	Erase beginning of line
ESC K	HEOL	Erase to end of line
ESC L	HIL	Insert line
ESC M	HDL	Delete line
ESC N	HDCH	Delete character
ESC @	HEIM	Enter Insert Character mode
ESC O	HERM	Exit Insert Character mode
CONFIGURATION		
ESC z	HRAM	Reset to Power-Up configuration
ESC r B_n	HMBR	Modify baud rate B_n A = 110 B = 150 C = 300 D = 600 E = 1200 F = 1800 G = 2000 H = 2400 I = 3600 J = 4800 K = 7200 L = 9600
ESC x P_s	HSM	Set mode(s) P_s 1 = enable 25th line 2 = no key click 3 = hold screen mode 4 = block cursor 5 = cursor off 6 = keypad shifted 7 = alternate keypad mode 8 = auto line feed on receipt of CR 9 = auto CR on receipt of line feed

Escape Sequence	Mnemonic	Definition
Configuration (continued)		
ESC y P_s	HRM	Reset mode(s) P_s 1 = disable 25th line 2 = enable key click 3 = exit hold screen mode 4 = underscore cursor 5 = curson on 6 = keypad unshifted 7 = exit alternate keypad mode 8 = no auto line feed 9 = no auto CR
ESC <	HEAM	Enter ANSI mode
MODES OF OPERATION		
ESC [	HEHS	Enter Hold Screen mode
ESC \	HXHS	Exit Hold Screen mode
ESC p	HERV	Enter Reverse Video mode
ESC q	HXRV	Exit Reverse Video mode
ESC F	HEGM	Enter Graphics mode
ESC G	HXGM	Exit Graphics mode
ESC t	HEKS	Enter Keypad Shifted mode
ESC u	HXKS	Exit Keypad Shifted mode
ESC =	HAKM	Enter Alternate Keypad mode
ESC >	HXAM	Exit Alternate Keypad mode
ADDITIONAL FUNCTIONS		
ESC }	HDK	Keyboard disabled
ESC {	HEK	Keyboard enabled
ESC v	HEWA	Wrap around at end of line
ESC w	HXWA	Discard at end of line
ESC Z	HID	Identify as VT52 (ESC / K)
ESC)	HX25	Transmit 25th line
ESC #	HXMP	Transmit page
Note: The Terminal will transmit the following sequences, but it will not respond to them if they are received by the Terminal.		
ESC S	HF1	Function Key #1 (f_1)
ESC T	HF2	Function Key #2 (f_2)
ESC U	HF3	Function Key #3 (f_3)
ESC V	HF4	Function Key #4 (f_4)
ESC W	HF5	Function Key #5 (f_5)
ESC P	HF7	Function Key (BLUE)
ESC Q	HF8	Function Key (RED)
ESC R	HF9	Function Key (GRAY)

*See Operation Manual for the H19 Terminal (#595-2404) for a detailed explanation.

SUMMARY OF ANSI ESCAPE SEQUENCES*

Notes:

1. In the ANSI mode, the Terminal recognizes and responds only to escape sequences whose syntax and semantics are in accordance with ANSI specifications.

2. *Default* is a value that is assumed when no explicit value, or a value of zero, is specified.

3. P_n - Numeric Parameter. Any decimal value may be substituted for P_n.

4. P_s - Selective Parameter. Any decimal number that is taken from a list and used to select a subfunction. You can select several subfunctions at once by putting one number after another, but separating them with delimiters (semicolons).

   Example: To turn off the key click (ESC [>2h) and turn on the block cursor (ESC[>4h), type:

   ESC[>2;4h

Escape Sequence	Mnemonic	Definition
CURSOR FUNCTIONS		
ESC [H or ESC [0;0 H or ESC[1;1 H	CUP	Cursor home
ESC [f or ESC[0;0 f or ESC[1;1 f	HVP	
ESC [P_n C	CUF	Cursor forward
ESC [P_n D	CUB	Cursor backward
ESC [P_n B	CUD	Cursor down
ESC [P_n A	CUU	Cursor up
ESC [M	RI	Reverse index
ESC [n	CPR	Cursor position report
ESC [s	PSCP	Save cursor position
ESC [u	PRCP	Set cursor position
ESC [P_r;P_cH or ESC [P_r;P_cf	CUP	Direct cursor addressing

Escape Sequence	Mnemonic	Definition
ERASING AND EDITING		
ESC[2 j	ED	Clear display (shift erase)
ESC[1 j	ED	Erase beginning of display
ESC[j or ESC[0 J	ED	Erase to end of page (erase key)
ESC[2 K	EL	Erase entire line
ESC[1 K	EL	Erase beginning of line
ESC[K or ESC[0 K	EL	Erase to end of line
ESC[P_nL	IL	Insert line
ESC[P_nM	DL	Delete line
ESC[P_nP	DCH	Delete character
ESC[4 h	IRM	Insert/replacement (insert character) mode on
ESC[4 l	IRM	Insert/replacement (insert character) mode off

*See H19 Operation Manual for detailed explanation

CONFIGURATION

ESC [z	PRAM	Reset to power-up configuration
ESC [P_n r	PMBR	Modify baud rate P_n 1 = 110 2 = 150 3 = 300 4 = 600 5 = 1200 6 = 1800 7 = 2000 8 = 2400 9 = 3600 10 = 4800 11 = 7200 12 = 9600
ESC [> P_s h	SM	Set mode(s) P_s 1 = Enable 25th line 2 = No key click 3 = Hold screen mode 4 = Block cursor 5 = Cursor off 6 = Keypad shifted 7 = Alternate keypad mode 8 = Auto line feed on receipt of CR 9 = Auto CR on receipt of line feed
ESC [> P_s l	RM	Reset mode(s) P_s 1 = Disable 25th line 2 = Enable key click 3 = Exit hold screen mode 4 = Underscore cursor 5 = Cursor on 6 = Keypad unshifted 7 = Exit alternate keypad mode 8 = No auto line feed 9 = No auto CR
ESC [? 2 h	PEHM	Enter Heath mode

MODES OF OPERATION

ESC [7 m	SGR	Enter reverse video mode
ESC [m or ESC [0 m	SGR	Exit reverse video mode
ESC [> 7 h	SM	Enter alternate keypad mode (ESC =)*
ESC [> 7 l	RM	Exit alternate keypad mode (ESC >)*

ADDITIONAL FUNCTIONS

ESC [2 h	SM	Keyboard disabled
ESC [2 l	RM	Keyboard enabled
ESC [? 7 h	SM	Wrap around at end of line
ESC [? 7 l	RM	Discard at end of line
ESC [q	PX25	Transmit 25th line
ESC [p	PXMT	Transmit page

Note: The Terminal will transmit the following functions, but will not respond to them if they are received by the Terminal.

ESC O S	SS3	Function key #1 (f_1)
ESC O T	SS3	Function key #2 (f_2)
ESC O U	SS3	Function key #3 (f_3)
ESC O V	SS3	Function key #4 (f_4)
ESC O W	SS3	Function key #5 (f_5)
ESC O P	SS3	Function key (BLUE)
ESC O Q	SS3	Function key (RED)
ESC O R	SS3	Function key (GRAY)

*These escape modes may be used, but are not recommended.

ASCII CHARACTERS

The characters in the shaded areas are not processed by the Terminal.

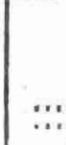
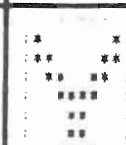
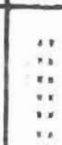
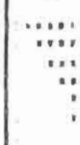
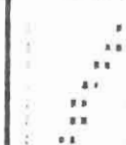
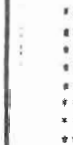
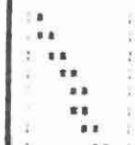
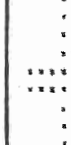
7-Bit Octal Code	Decimal Code	Hex Code	Characters	Control Keys	Description
000	0	0	NUL	@	Null, tape feed
001	1	1	SOH	A	Start of heading
002	2	2	STX	B	Start of text
003	3	3	ETX	C	End of text
004	4	4	EOT	D	End of transmission
005	5	5	ENQ	E	Enquiry; also WRU
006	6	6	ACK	F	Acknowledge; also RU
007	7	7	BEL	G	Rings the bell
010	8	8	BS	H	Backspace; also FEB (format effecter backspace)
011	9	9	HT	I	Horizontal tab
012	10	A	LF	J	Line feed; advances cursor to next line
013	11	B	VT	K	Vertical tab (VTAB)
014	12	C	FF	L	Form feed to top of next page
015	13	D	CR	M	Carriage return to beginning of line
016	14	E	SO	N	Shift out
017	15	F	SI	O	Shift in
020	16	10	DLE	P	Data line escape
021	17	11	DC1	Q	Device control 1: turns transmitter on (XON)
022	18	12	DC2	R	Device contr 2
023	19	13	DC3	S	Device control 3: turns transmitter off (XOFF)
024	20	14	DC4	T	Device control 4
025	21	15	NAK	U	Negative acknowledge: also ERR (error)
026	22	16	SYN	V	Synchronous idle (SYNC)
027	23	17	ETB	W	End of transmission block
030	24	18	CAN	X	Cancel (CANCL): cancels current escape sequence
031	25	19	EM	Y	End of medium
032	26	1A	SUB	Z	Substitute
033	27	1B	ESC	[	Escape
034	28	1C	FS	\	File separator
035	29	1D	GS	]	Group separator
036	30	1E	RS	^	Record separator
037	31	1F	US	-	Unit separator
040	32	20	SP		Space
041	33	21	!		Exclamation point
042	34	22	"		Quotation mark
043	35	23	#		Number Sign
044	36	24	$		Dollar sign
045	37	25	%		Percent sign
046	38	26	&		Ampersand
047	39	27	'		Acute accent or apostrophe
050	40	28	(		Open parenthesis
051	41	29	)		Close parenthesis
052	42	2A	*		Asterisk

7 Bit Octal Code	Decimal Code	Hex Code	Characters	Description
053	43	2B	+	Plus sign
054	44	2C	,	Comma
055	45	2D	-	Hyphen or minus
056	46	2E	.	Period
057	47	2F	/	Slash
060	48	30	0	Number 0
061	49	31	1	Number 1
062	50	32	2	Number 2
063	51	33	3	Number 3
064	52	34	4	Number 4
065	53	35	5	Number 5
066	54	36	6	Number 6
067	55	37	7	Number 7
070	56	38	8	Number 8
071	57	39	9	Number 9
072	58	3A	:	Colon
073	59	3B	;	Semicolon
074	60	3C	<	Less than
075	61	3D	=	Equal sign
076	62	3E	>	Greater than
077	63	3F	?	Question mark
100	64	40	@	At sign
101	65	41	A	Letter A
102	66	42	B	Letter B
103	67	43	C	Letter C
104	68	44	D	Letter D
105	69	45	E	Letter E
106	70	46	F	Letter F
107	71	47	G	Letter G
110	72	48	H	Letter H
111	73	49	I	Letter I
112	74	4A	J	Letter J
113	75	4B	K	Letter K
114	76	4C	L	Letter L
115	77	4D	M	Letter M
116	78	4E	N	Letter N
117	79	4F	O	Letter O
120	80	50	P	Letter P
121	81	51	Q	Letter Q
122	82	52	R	Letter R
123	83	53	S	Letter S
124	84	54	T	Letter T
125	85	55	U	Letter U
126	86	56	V	Letter V
127	87	57	W	Letter W
130	88	58	X	Letter X
131	89	59	Y	Letter Y
132	90	5A	Z	Letter Z

7-Bit Octal Code	Decimal Code	Hex Code	Character	Description
133	91	5B	[	Open brackets
134	92	5C	\	Reverse slash
135	93	5D	]	Close brackets
136	94	5E	↑	Up arrow/caret
137	95	5F	_	Underscore
140	96	60	`	Grave accent
141	97	61	a	Letter a
142	98	62	b	Letter b
143	99	63	c	Letter c
144	100	64	d	Letter d
145	101	65	e	Letter e
146	102	66	f	Letter f
147	103	67	g	Letter g
150	104	68	h	Letter h
151	105	69	i	Letter i
152	106	6A	j	Letter j
153	107	6B	k	Letter k
154	108	6C	l	Letter l
155	109	6D	m	Letter m
156	110	6E	n	Letter n
157	111	6F	o	Letter o
160	112	70	p	Letter p
161	113	71	q	Letter q
162	114	72	r	Letter r
163	115	73	s	Letter s
164	116	74	t	Letter t
165	117	75	u	Letter u
166	118	76	v	Letter v
167	119	77	w	Letter w
170	120	78	x	Letter x
171	121	79	y	Letter y
172	122	7A	z	Letter z
173	123	7B	{	Left brace
174	124	7C	|	Vertical bar (broken)
175	125	7D	}	Right brace
176	126	7E	~	Tilde
177	127	7F	DEL	Delete (rubout)

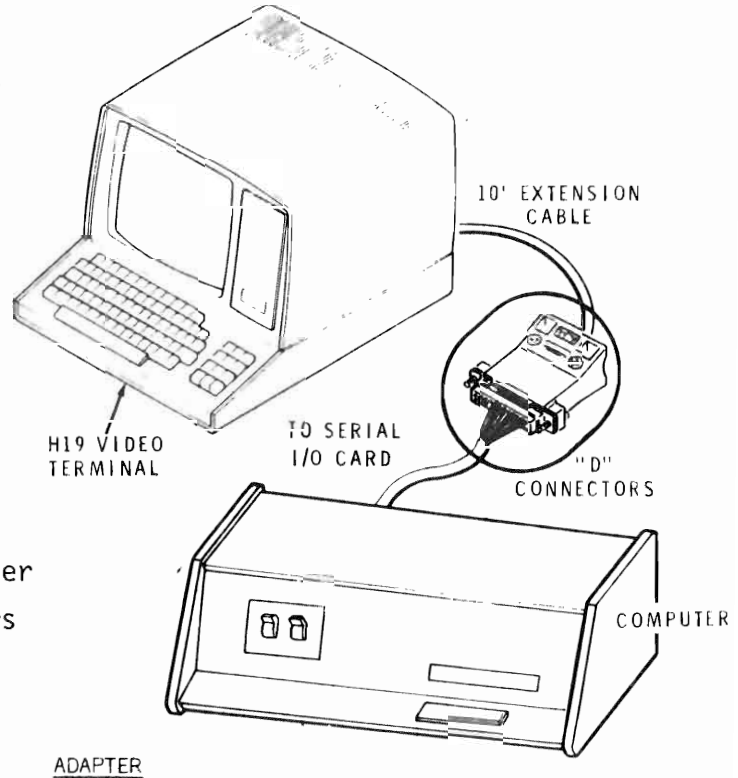
*Graphic symbols for 7-bit octal code 136 through 176 are on Page 18.

GRAPHIC SYMBOLS

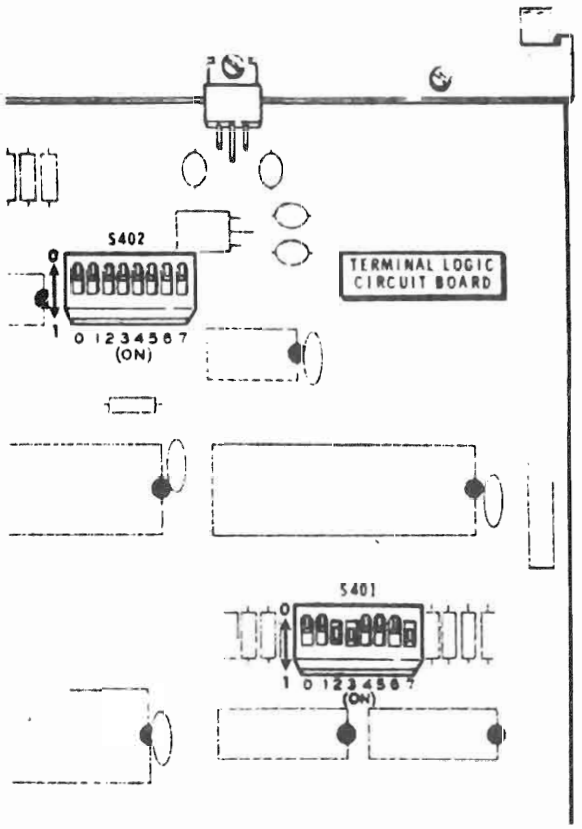
KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL	KEY (OCTAL) [DECIMAL]	SYMBOL
[illegible]		c (143) [99]		h (150) [104]		m (155) [109]		r (162) [114]		w (167) [119]		¦ (174) [124]	
~ (137) [95]		d (144) [100]		i (151) [105]		n (156) [110]		s (163) [115]		x (170) [120]		} (175) [125]	
` (140) [96]		e (145) [101]		j (152) [106]		o (157) [111]		t (164) [116]		y (171) [121]		~ (176) [126]	
a (141) [97]		f (146) [102]		k (153) [107]		p (160) [112]		u (165) [117]		z (172) [122]			
b (142) [98]		g (147) [103]		l (154) [108]		q (161) [113]		v (166) [118]		{ (173) [123]			

SYSTEM CONFIGURATION

The H19 Terminal serially communicates with the outside world through a rear panel "D" connector at RS-232C signal levels. It will mate with most equipment that conforms to this standard. The following adapter cables will convert earlier Heath equipment connectors to RS-232C connectors.



PRODUCT	ADAPTER
H9 Video Terminal	WH9-1
H8-5 Serial I/O	WH8-51
H8-4 4-Port Serial I/O	WH8-41
H11-5 Serial I/O	WH11-51



Two switch assemblies, S401 and S402 on the Terminal Logic circuit board, determine the H19 Terminal's operating mode when the unit is powered-up or reset. The "UP" position closes the switch (logic zero).

S401 determines the communications mode:

SWITCH SECTION	HEATH MODE	DESCRIPTION
0 - 3	4800 or 9600	Baud Rate - Selects any of 12 baud rates from 110 to 9600 baud. (See the Baud Rate Chart at the right.)
4	No Parity (0)	Parity - Programs the H19 Terminal to generate or eliminate the parity bit. UP (0) = No Parity DOWN (1) = Parity
5	Even (0)	Odd/Even Parity - Irrelevant if section 4 = 0. UP (0) = Even Parity DOWN (1) = Odd Parity
6	Normal (0)	Normal/Stick Parity - Irrelevant if section 4 = 0. UP (0) = Normal Parity DOWN (1) = Stick Parity
7	Full Duplex (1)	Full Duplex/Half Duplex - UP (0) = Half Duplex DOWN (1) = Full Duplex

SWITCH SECTION	BAUD RATE
0000	N/A
1000	110
0100	150
1100	300
0010	600
1010	1200
0110	1800
1110	2000
0001	2400
1001	3600
0101	4800
1101	7200
0011	9600

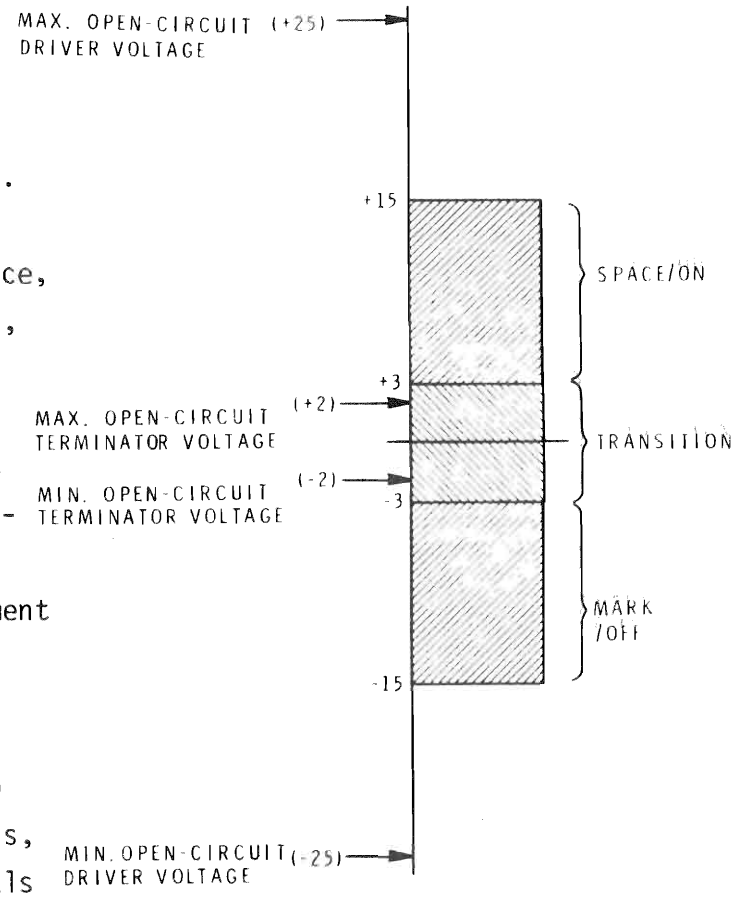
S401
BAUD RATE CHART

S402 determines display, keyboard, and Escape modes:

SWITCH SECTION	DESCRIPTION
0	UP (0) = Underscore Cursor DOWN (1) = Block Cursor
1	UP (0) = Key Click DOWN (1) = No Key Click
2	UP (0) = Discard past end of line (no Auto-Carry at end of line) DOWN (1) = Wrap Around (Auto-Carry at end of line)
3	UP (0) = No Auto LF on CR DOWN (1) = Auto LF on CR
4	UP (0) = No Auto CR on LF DOWN (1) = Auto CR on LF
5	UP (0) = Heath Escape Mode DOWN (1) = ANSI Escape Mode
6	UP (0) = Keypad Normal (Enters numbers when key is pressed.) DOWN (1) = Keypad Shifted (Enters display manipulation commands when a keypad key is pressed.)
7	UP (0) = 60 Hz Display Refresh DOWN (1) = 50 Hz Display Refresh

For Heath equipment, all S402 switch sections will normally be in their UP (logic zero) positions.

This Terminal is designed to interface with serial I/O modules that use the RS-232C standards of the Electronic Industries Association (EIA). This standard defines an ansynchronous serial interface, its voltages, its impedances, and its physical connectors.

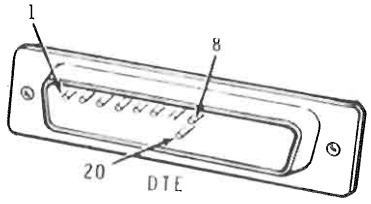


RS-232C places all equipment into one of two general categories.

DTE - Data Terminal Equipment

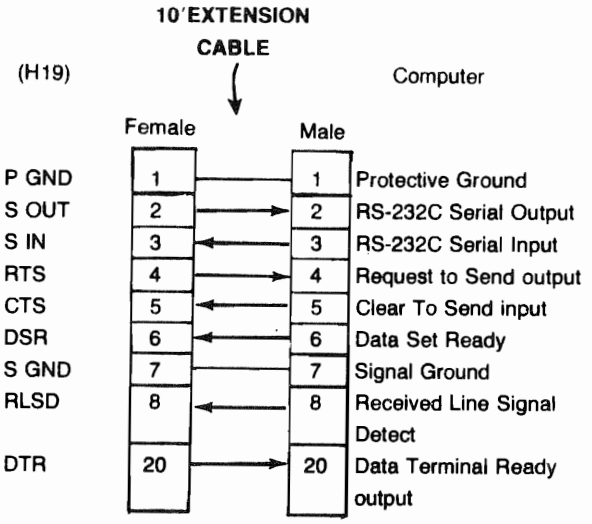
DCE - Data Communications Equipment

Computers and MODEMS are two types of DCE; while terminals, printers, and most peripherals are DTE. Always connect a DTE to a DCE. Nover connect two like types togehter.



The 25-pin D connector on the back panel of the Terminal is a DTE (DB-25P) connector. The pictorial at the left shows the pin numbering of this connector.

The chart at the right describes the DTE outputs of the rear panel connectors.



OPERATION NOTES:

NORMAL OPERATING CHARACTERISTICS

The operating conditions listed here are considered normal operation of the H19 Terminal. Become familiar with the characteristics before servicing the unit. To do so, may save you some troubleshooting time.

1. Faint vertical lines (due to ringing in the horizontal deflection yoke) may be visible on the left side of the CRT when the display is filled with reverse video spaces. If they are objectionable, most of them can be moved off screen by careful adjustment of the horizontal centering control and the CRT ring magnets.

2. The displayed characters should be stable. If they jitter, check the 50/60 Hz Display Refresh setting on S402 on the Terminal Logic circuit board.

3. Random blanking, approximately three characters wide by one scan line deep, will appear on the CRT when data is entered via the keyboard, the external input, or in the "transmit page" mode. If some of the shifted keypad functions are used, these blanked areas will appear to be sloping diagonally, several scan lines deep, and sometimes the length of the CRT. Both symptoms are due to the CPU blanking the display when it reads or writes the display memory, to prevent random garbage from appearing on the CRT. (See the Circuit Description.)

4. The displayed characters will be well-focused and linear across the CRT. If not, check the Video board adjustments.

5. Changing the settings of S401 and S402 on the Terminal Logic circuit board while the H19 is turned on will have no effect until the unit is reset, or turned off and then on again.

6. R212 on the Video board may get hot. It runs about 1.5 watts dissipation. Early production runs have have a two-watt resistor here. If so, replace it with a 1500 ohm, five-watt resistor (#3-57-5).

7. The power transformer will run warm.

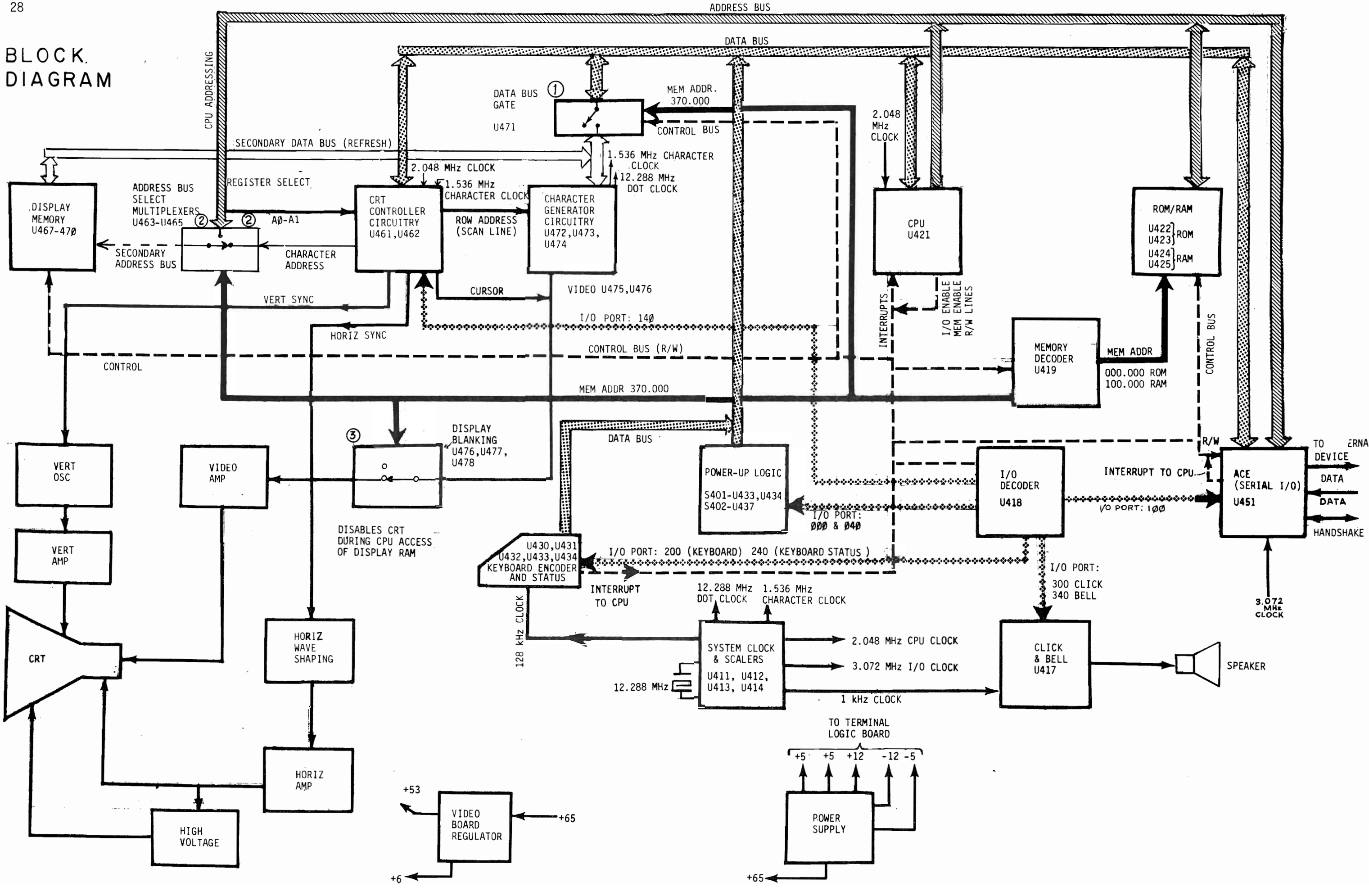
8. The LSI chips on the Terminal Logic circuit board will run warm, but not hot.

9. The bell will not sound when the end of line is reached.

10. Q401 and R406 may be missing on the Terminal Logic circuit board. This is part of the reset circuitry used in the H88/H89.

TECHNICIAN NOTES

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

OVERVIEW

Basically, the H19 Computer is made up of a dedicated microprocessor (Z80) that has three distinct memory blocks and eight I/O ports. Two of the memory blocks are strictly for the CPU's use. One is a read-only memory, starting at address 000.000A, 4 kilobytes long and contains the controlling program. The second block is a 256 byte scratchpad RAM, starting at 100.000A, that contains the stack, the initial operating mode (set up by the two sets of slide switches on the Terminal Logic circuit board), temporary data buffers for communicating with an external computer and display formatting information. Much of this scratchpad can be changed by using the proper Escape sequence. The last memory block (370.000A) is shared by the CPU and the Video Display circuits. It is here that the ASCII characters will be stored for display on the CRT. These memory locations are read from or written to via the data bus and pointed to by the memory decoder and the address bus.

Two of the eight I/O ports are for power-logic (000.000A and 000.040A). The controlling program will monitor the state of the slide switches at these ports on first turn-on and set the H19 Terminal's operating mode accordingly. This will occur if the right-hand Shift key and Reset keys are pressed at the same time.

If the CPU does not need to access the display RAMs, then the display circuits (CRT Controller, Character Generator, RAMs) will be operating in its own loop; fetching an ASCII character from the display RAMs, converting it to dots, sending it to the Video amplifier and fetching the next character.

Essentially, the CPU is doing the same thing. It is in a loop constantly; checking the status of the Off-Line key, certain buffer registers in the scratchpad RAM, and waiting for an interrupt to occur. An interrupt will occur if the Asynchronous Communications Element (ACE) has valid data in its internal buffer, if the Break key is closed or if a key is tapped on the keyboard. The CPU will then check the Keyboard Encoder and Keyboard Status circuits (ports 000.200A and 000.240A), the Break key (port 240A) and the status registers in the ACE (port 000.100A) to determine where the interrupt came from.

For example, if the letter *H* is tapped on the keyboard, the CPU will jump to the interrupt-handling routine, which will look at the Keyboard Status circuits; and thus determine that the Keyboard Encoder caused the interrupt. It will then jump to another routine to get the ASCII character from the Keyboard Encoder, determine that it is a printable character, and send it to the display RAMs. If the H19 is on-line, it will send the character to the ACE instead. In either case,

the CPU will also gate the 1 kHz clock to the speaker, via the Click circuits (port 000.300A), to provide an aural indication that the key was pressed. This feature can be disabled and enabled through software and hardware (the slide switches).

TERMINAL LOGIC CIRCUIT BOARD

POWER SUPPLIES

The Terminal Logic circuit board contains regulator circuits that take the +8 volt, +16 volt, and -16 volt supplies from the Power Supply circuit board and convert them to two +5 volt supplies, one +12 volt supply, a -12 volt supply, and a -5 volt supply. To minimize interaction with the Video circuits, these supplies are used exclusively on the Terminal Logic board.

CLOCK CIRCUIT

All system timing is generated by a 12.288 MHz crystal-controlled oscillator. It is buffered and used directly by the CRT Controller (CRTC) to generate video dot information. It is divided by four to provide 3.072 MHz timing for the Serial I/O. The 2.048 MHz is the clock for the CPU and the CRT Controller. The CRT Controller also receives 1.536 MHz to provide character display timing. The Keyboard Encoder uses a multiplexing technique to provide the correct code for a key closure, and so receives 128 kHz from the Clock circuits for it's timing needs. The 128 kHz is then divided by 128 to provide a 1 kHz tone which is used by the Bell and Click circuits.

BASIC OPERATION

On power-up, the CPU program counter is set to the starting address of the PROM*(000.000A). The firmware will initialize the H19 Computer by clearing the scratchpad RAM, writing ASCII "spaces" into the display RAM, setting the ACE (baud rate, parity, etc.), initializing the CRT Controller and setting various memory locations in the scratchpad RAM for internal housekeeping functions.

KEYBOARD ENCODER AND KEYBOARD STATUS

Though consisting of two ports, the Keyboard Encoder and the Keyboard Status circuits usually act together. If a key is pressed, the CPU receives an interrupt. It does not know if the interrupt came from the Keyboard Encoder, the Break Key (in the Keyboard Status circuits), or the Asynchronous Communications Element (ACE). So the CPU will use the I/O port decoder and read/write lines to check each one. Once the source of the interrupt has been determined, it will jump to the correct interrupt routine in ROM to process the data.

The Keyboard Encoder will convert all alphanumeric keys and most control keys to their ASCII equivalent and place the character on the data bus. This data is processed by the CPU to determine its ultimate destination (to the display output, to an external device, or a change in the H19's operating mode).

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*PROMs were used in the earlier productions because of the excessive lead times in obtaining ROMs from the manufacturer.

Some control keys, such as BREAK, CAPS LOCK, and OFF LINE, are fed directly to the data bus through the Keyboard Status buffer. Others, such as the SHIFT, REPEAT, and CTRL keys, are processed through the Keyboard Encoder and/or the Keyboard Status circuits; depending on the firmware requirements.

SERIAL I/O - ACE

The Asynchronous Communications Element (ACE) is the serial I/O port that the H19 Computer uses to talk to the outside world. It provides handshaking lines that effectively idle in the "ready" state when not connected. This permits the H19 Terminal to be used with the H8-4, the H8-5, and the H11-5 boards without hardware modification.

Incoming data will cause a CPU interrupt. The CPU will access the ACE status registers using the I/O decoder and read/write lines to see if the interrupt came from the ACE. If so, the CPU will process the data according to what the data is. For example, if it is a printable ASCII character, it will usually be sent directly to the CRT display circuitry via the data bus. If it's an Escape character (or sequence of characters), it will be processed by the CPU before the display is modified.

CLICK AND BELL

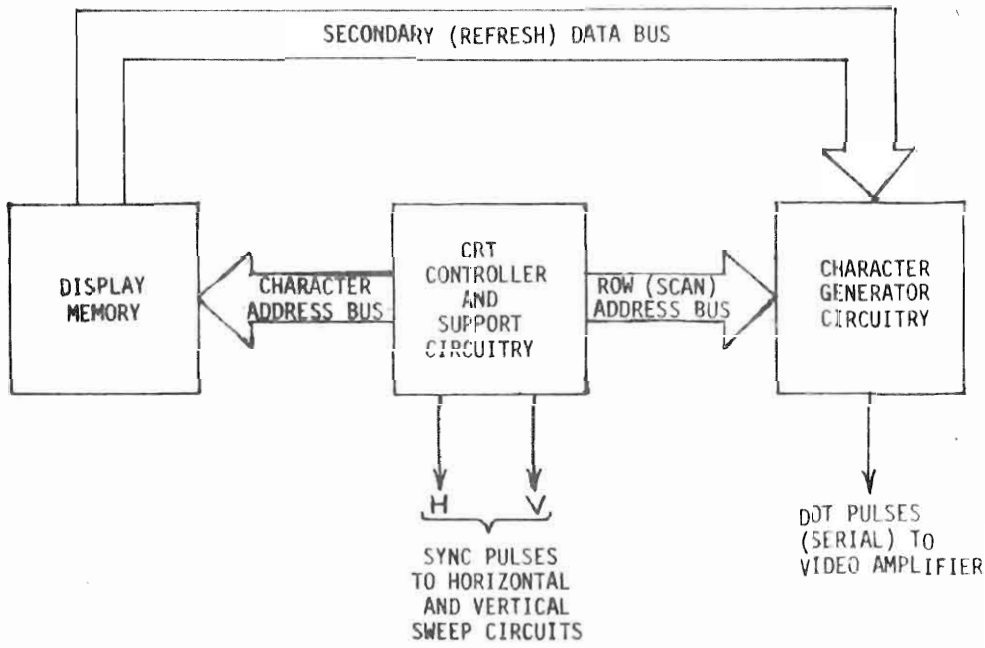
A click is heard as each key is pressed to provide the user with an aural indicator. If the user finds the click distracting, it can be turned off through either hardware (S402 and then resetting the H19) or software (enter 'ESC', 'x' (lower case) '2' through the keyboard).

The bell will ring when the terminal processes a 'control G' character (an octal '7').

Both the click and bell are derived from the system clock (1 kHz). The click is set to 6 milliseconds and the bell to 200 milliseconds. Both the frequency and duty cycle are fixed in hardware and cannot be varied as in the H8 Computer.

CHARACTER GENERATOR AND DISPLAY

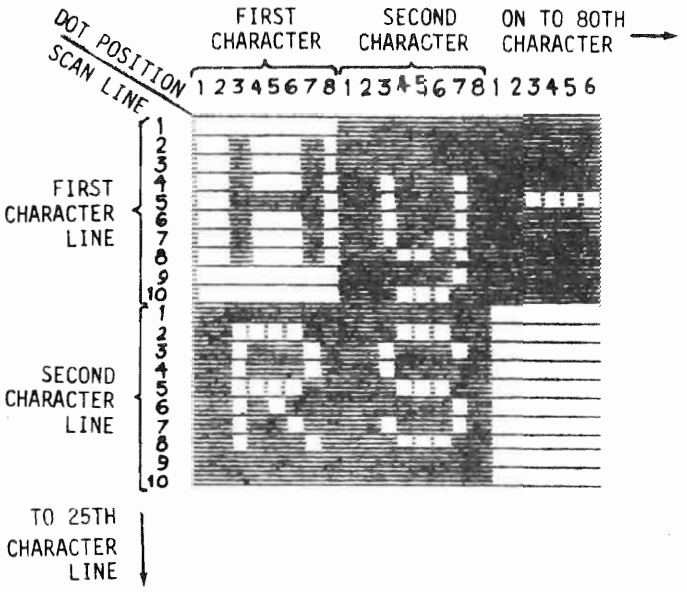
Basic Character Generator Operation



Block Diagram

The CRT Controller (CRTC) generates all the addressing and timing information required to place characters in their proper position on the screen. (Refer to the above Block Diagram.) This includes cursor positioning, intercharacter blanking, and horizontal and vertical timing. The CRTC chip contains nineteen programmable registers that allow computer control of such things as direct cursor positioning, number of scan lines per character row, type of scan (the H19 is non-interlace), and many other things. The CPU will address port 000.140A to read or write these registers.

Assume that the first line of information is about to be displayed. Through the Character Address bus, the controller points to the first character of the first line in the Display memory. This ASCII character is loaded into the Character Generator circuitry via the Refresh Data Bus. The CRTC then places an address on the Row Address Bus that tells the Character Generator that the first scan line of data is to be generated. Unless the H19 Terminal is in the graphics or reverse video mode, the first scan line of a character line will be blanked. Refer to the pictorial below.



Here the first character is a reverse-video capital *H*. The character generator recognizes this as a reverse-video character and unblanks the first scan line for a period of eight dot clocks. (However, for reverse video, bear in mind, that an unblanked scan line is a solid line rather than a string of dots.) At the end of eight dots, the CRTC addresses the second character in the first line of display memory and loads it into the Character Generator. The Row Address bus still points to

the first scan line. The second character is a lower case *y*, so the top scan line is blanked. The CRTC will maintain its Row Address counter at the first scan line until all 80 character positions for the first character line have been loaded and processed. At that time, it will increment the Row Address bus to the second scan line and reset the Character Address bus back to the first character location in the first line. The reverse video *H* is again loaded into the Character Generator and the information for the second scan line is extracted. In the upper-case mode, a 5 x 7 matrix is used (out of the available 8 x 10) for character display. The first two dots and the last dot positions are always blanked. This is also true of the lower case characters, except that two more scan lines will be used for a total of 5 x 9. Depending upon the character, the graphics mode will use all 8 x 10 dots. The reverse video *H* will be unblanked at the first two dot positions and blanked at the third dot position.

This scan line of unblanks and blanks are transmitted by the Character Generator in a serial stream in synchronization with the horizontal and vertical timing pulses. The process will then repeat. The Character Generator will load and convert the next character to dots for the current scan line. It will do this for 80 characters before incrementing the Row Address counter for the next scan line. The character generator will then get the first character in the current character line and repeat the process. At the end of ten scan lines, the CRTC will set its row address counter back to the first scan line position while the character address bus will access the first character in the second line of information (capital R). This is still the first

vertical sweep and the start of the eleventh scan line, so the first character on the second line will be displayed under the *H*. As before, the CRTC and Character Generator will process this line of information, 80 characters per scan line, for ten scan lines.

The next character line is accessed and the previous procedure is repeated for a total of 25 character lines. The electron beam will then retrace to the top of the raster. The CRTC will again address the first character in the first line and the Character Generator will again process this information for display.

H19 CHARACTER GENERATION

Refer again to the H19 Block Diagram and look at how the Character Generator interfaces to the rest of the circuitry.

Three groups of ICs can essentially be represented as switches: (1) the Data Bus Gate will connect or disconnect the CPU data bus to the refresh bus; (2) the Address Bus Select allows either the CPU or the CRTC to access the Display Memories; and (3) the Display Blanking removes dot data going to the Video Amplifier when the CPU is on the refresh bus.

Normally these three switches are in the "position" shown in the block diagram--the CPU is effectively disconnected while the controller is keeping the display updated. If the CPU has to read or write data in the display memories, it will activate

the Memory Decoder address line, 370.000A, which closes the Data Bus gate. The Address Bus Select multiplexer is switched over from the CRT Controller to the CPU address lines and the video information is blocked by the display blanking. The blanking is necessary to prevent garbage from appearing on the CRT because the Character Generator is still active.

Data on the control line from the CPU will inform the display RAM whether the operation is a read or a write.

DISPLAY CIRCUITS

The Video board consists of four major sections: the Vertical Sweep circuits, the Horizontal Sweep circuits, the Video Amplifier, and the Power Supplies. The main power supply converts the unregulated +65 volts to a regulated +53 volts and +6 volts source. These are used by the Video board exclusively. The Video Amplifier is a conventional cascode amplifier that direct couples the dot information to the cathode of the CRT.

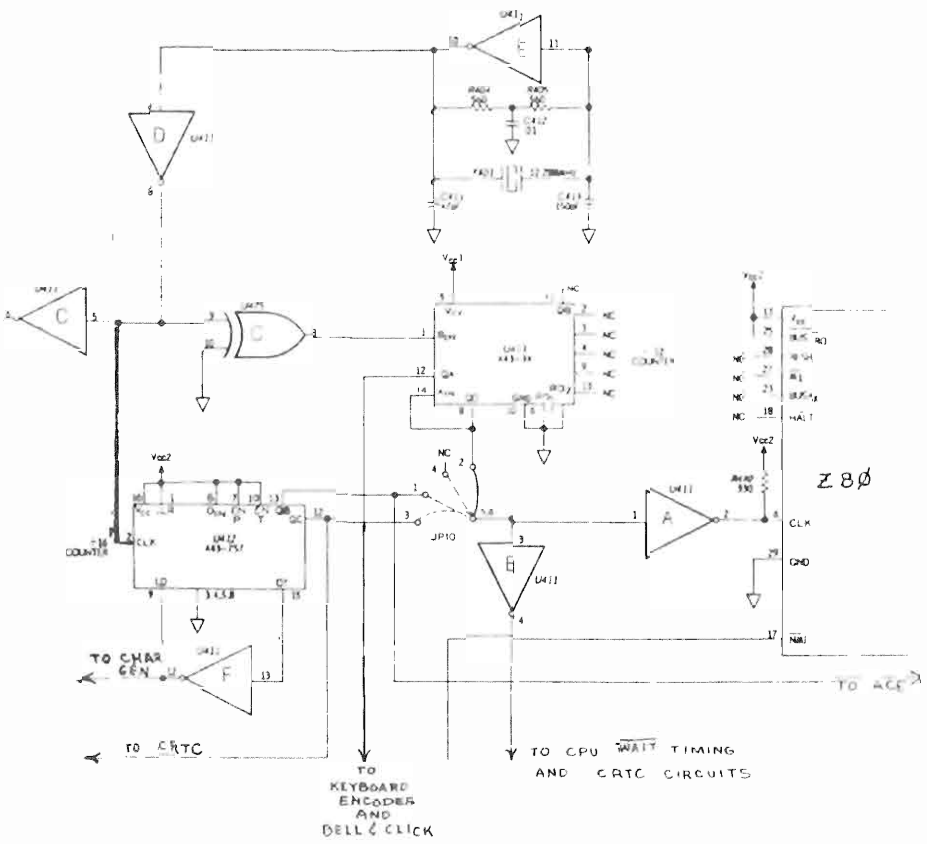
The Vertical Sweep circuits consists of a relaxation oscillator that is synchronized by the vertical timing pulse from the CRTC. This is then sent to the Vertical amplifier, where the waveform is shaped and amplified to obtain a linear vertical sweep.

The Horizontal Sweep circuits have no oscillator. The horizontal sync pulse is sent to a timing circuit where it is delayed for correct horizontal positioning, and then sent to the horizontal amplifier. The horizontal amplifier shapes and amplifies this pulse to the level required for a linear sweep.

The high voltage power supply is part of the horizontal amplifier and uses the horizontal sweep signal to generate the bias voltages for the CRT, including the filament voltage. The horizontal sync pulse from the CRTC is needed for generating the CRT operating voltages.

DETAILED CIRCUIT DESCRIPTION

CLOCK CIRCUITS



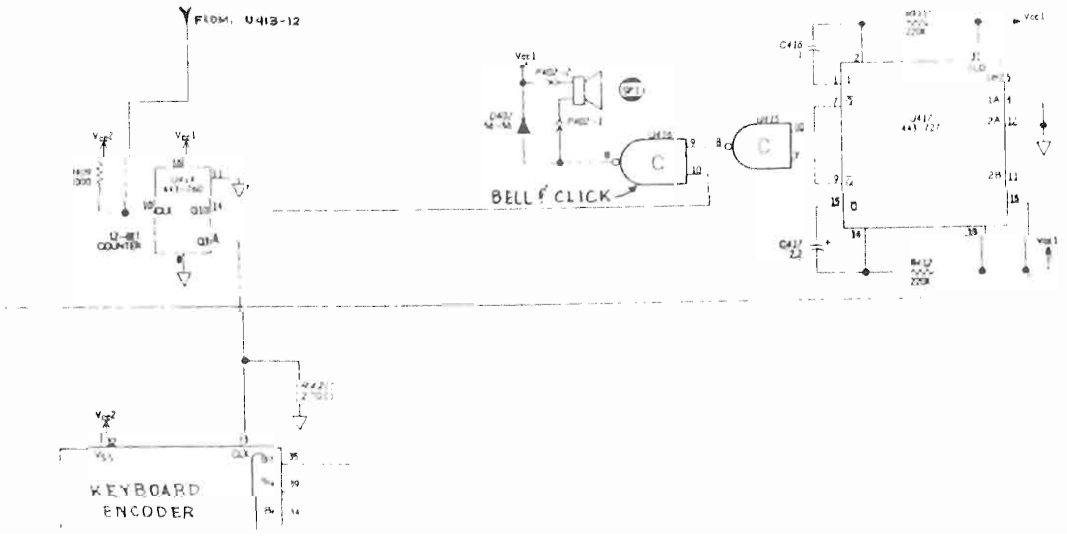
The Master Clock consists of section 'E' of the 7404 hex inverter, U411, and associated components. Y401 sets the operating frequency to 12.288 MHz by providing positive feedback at that frequency. R404 and R405 bias U411 into its linear region through negative feedback. C412 provides RF decoupling in this loop, while C411 and C413 match the crystal impedance to the rest of the circuit.

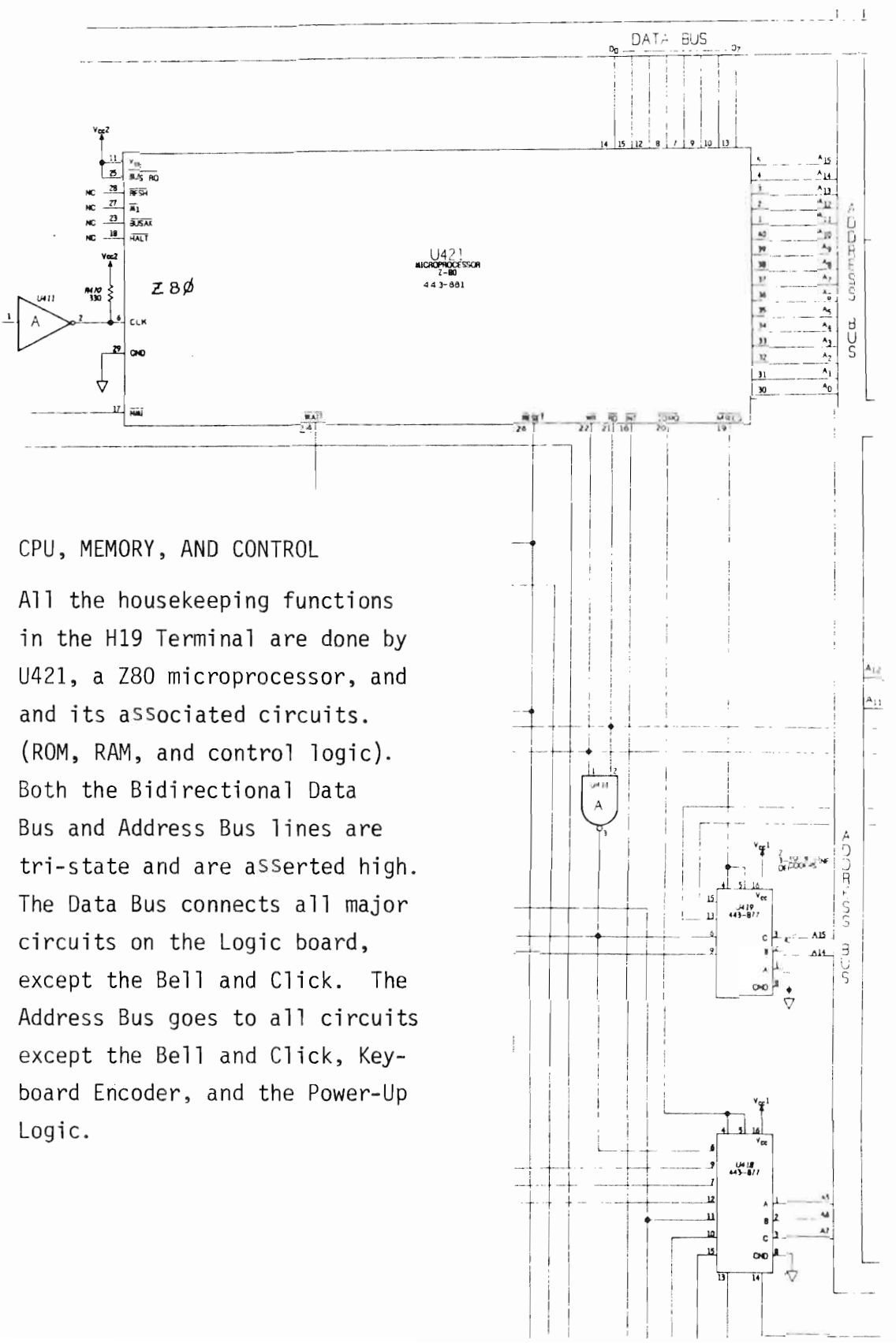
The Master Clock signal has an amplitude of 2 V P-P. This signal is fed through the inverter, U411D, and then sent to the three major circuits. U411C will again invert this signal and couple it to the display circuits as Dot Clock. It is sent to U413 through U475C to provide timing for the CPU, CRT Controller (CRTC), Keyboard Encoder, Bell and Click circuits. And it is connected to U412, pin 2 to provide Character Clock to the display circuits and timing to the Asynchronous Communications Element (ACE).

U412 is a synchronous 4-bit (divide-by-16) binary counter wired for divide-by-8 operation. This is done by preloading the counter with 1000B and counting up to 1111B. The MSD of the parallel input (pin 6) is wired to a logic 1, while the three remaining parallel inputs are grounded. Thus, whenever the data load line ($\overline{LD}$, pin 9) is brought low, the counter will load with 1000B. When the 12.288 MHz clock causes the count to become 1111B, the carry line (CY, pin 15) goes to a logic 1. This logic 1 is inverted by U411F and the resulting logic Ø is applied to $\overline{LD}$ of U412. This resets U412 to the count of 1000B. As the carry line (pin 15) only stays high as long as U412's QA (pin 14) line is high, this reset pulse is a spike approximately 100 ns long occuring at a 1.536 MHz rate. This signal is sent to the Character Generator as one of the character clocks. Output QC (pin 12) is changing states at the character clock rate, but has a 50% duty cycle. This times the CRTC and Video Processing circuitry. U412, pin 13 (QB) provides a 3.072 MHz signal for ACE timing.

As stated before, the 12.288 MHz clock connects to BIN (pin 1) of U413, a 7492 divide-by-12 counter. This clock signal is divided by 6 at the QD output and is the 2.048 MHz CPU clock. This 2.048 MHz clock is distributed in three directions; (1) to the CPU clock input through inverter U411A, (2) to the CRTC timing circuitry and CPU wait-timing circuits through U411B, and (3) to the 'A' input of U413. The clock signal will be divided by 2 at U413, pin 12, and the resulting 1.024 MHz signal is sent to the 12-bit counter, U414.

U414 is a CMOS 4040 12-bit binary counter. Of the twelve internal flip-flops, only two are tapped for a clock. The output signal at Q3 of this counter is the 128 kHz clock (1.024 MHz ÷ 8) for the Keyboard Encoder multiplex circuits. The output signal at Q10 is the 1.024 MHz clock divided by 1024, which is a 1 kHz tone. This tone is processed by U416C to produce the bell and click sounds.





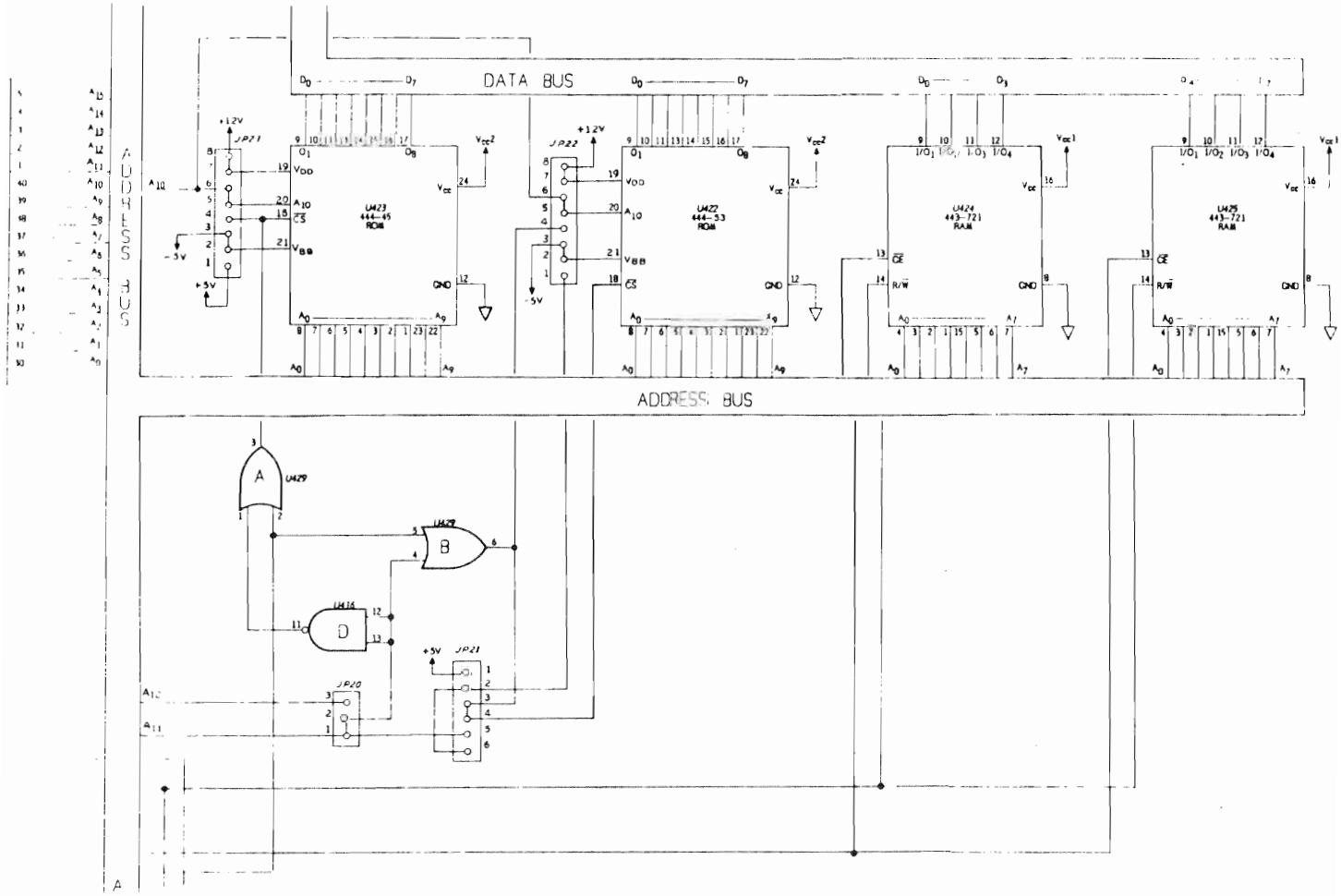
CPU, MEMORY, AND CONTROL

All the housekeeping functions in the H19 Terminal are done by U421, a Z80 microprocessor, and and its associated circuits. (ROM, RAM, and control logic). Both the Bidirectional Data Bus and Address Bus lines are tri-state and are asserted high. The Data Bus connects all major circuits on the Logic board, except the Bell and Click. The Address Bus goes to all circuits except the Bell and Click, Keyboard Encoder, and the Power-Up Logic.

Three enable pins must be asserted at U419 before a memory location can be accessed. When a memory location is to be read or written, the CPU will pull the $\overline{\text{MREQ}}$ line low (pin 19), which is fed to pins 4 (G2A) and 5 (G2B) of U419, the memory decoder. The CPU will then bring pin 21 or 22 low, depending on whether a read or write is to be performed, which will drive the output of U416A to a logic 1. U416A, pin 3 connects to three circuits: an address line multiplex IC in the display circuits (which will be discussed later), the I/O decoder (U418) and the memory decoder. Since pins 4 and 5 of U418 are at logic 1, only the memory decoder, U419, is active. U419 will decode address lines A14 and A15 and assert the appropriate output line low according to the Truth Table at the right.

A15	A14	PIN #	Component	Address
0	0	15	PROM (U422, U423)	000.000A
0	1	13	RAM (U424, U425)	100.000A
1	0	11	Not used	
1	1	9	Display RAMs (U467-U470)	370.000A

U429A, U429B, and U416D select the 2 K bank of PROM that is to be used. U422 is the lower 2 K. To select U422, address line A11 will go low at pin 4 of U429B. Since pin 5 is also low, pin 18 of U422 is asserted, enabling this IC. A11 is



also inverted by U416D, placing a logic 1 on pin 18 of U423 through U429, disabling the upper 2 K. When the upper 2 K is to be selected, A11 goes high, placing a logic 1 on $\overline{CE}$ of U422 and asserting U423 with a logic Ø from U416D and U429A.

Two 256 bit by 4 RAMs make up the scratch-pad. U424 holds the lower 4 bits of the byte; U425 the upper. When U419 selects these, starting at the 16 K point, they will be read from or written into without further external address decoding.

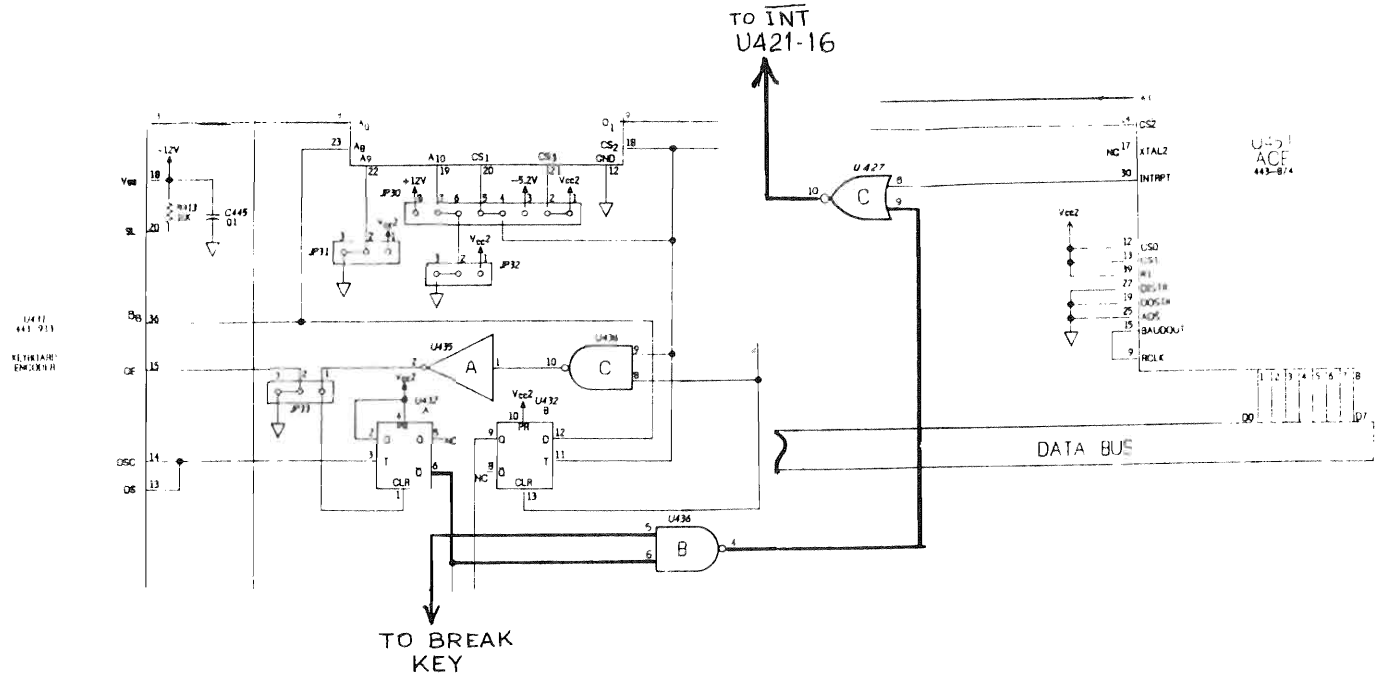
The I/O port decoder, U418 works on the same principle as U419. Here, pin 20 of U421 is brought low and U418 is activated when U416A detects a read or write command. For inputting or outputting data, the Z80 places the port address on the lower 8 bits of the address bus. Since only eight of the available 256 ports are being used, the port addresses are arranged so that full decoding isn't required. See the Truth Table at the right.

A7	A6	A5	PIN #	Circuit	Port
0	0	0	15	Power-Up Logic	000
0	0	1	14	Power-Up Logic	040
0	1	0	13	ACE	100
0	1	1	12	CRTC	140
1	0	0	11	Keyboard Encoder	200
1	0	1	10	Keyboard Status	240
1	1	0	9	Click	300
1	1	1	7	Bell	340

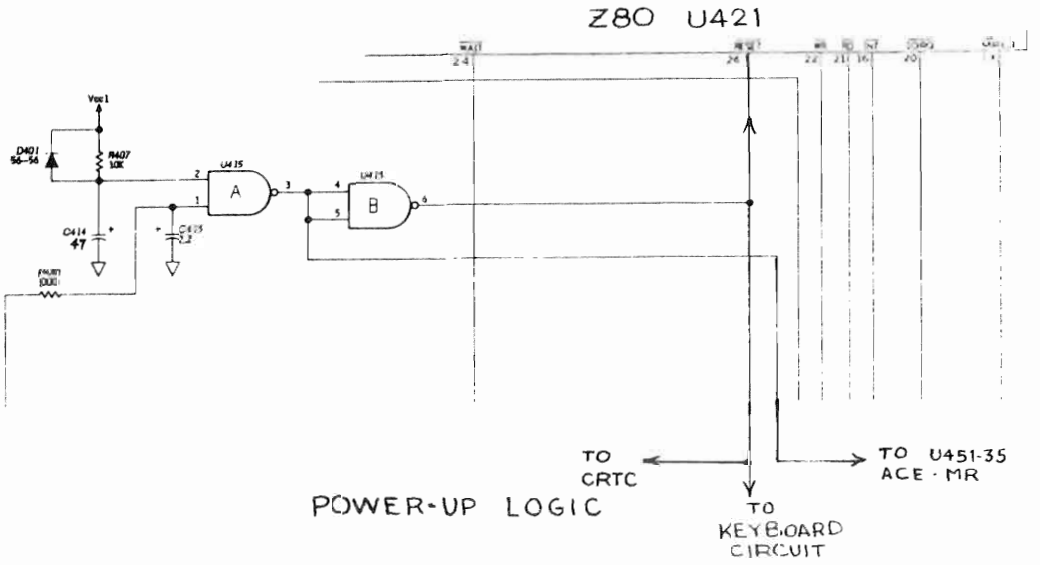
The final major circuit in the dedicated microcomputer portion of the H19 Terminal is the interrupt system. Pin 17 of CPU, U421, is the Non-Maskable Interrupt. During the vertical retrace, the $\overline{\text{NMI}}$ will be brought low and the CPU's program counter will point to address 000.146A (the Z80 NMI starting location) and execute the program there. If any of the display status has been changed, such as cursor position or cursor type (block or underscore), the CPU will write this into the CRTC's registers. This will be covered in more detail in the description of the Video Display circuits.

In some cases, other lines of the address bus will be used to address certain portions of the selected ports at this time, such as the status registers of the ACE. This will be covered later.

On first turn-on, or after a reset, the firmware will program the CPU for Mode One Interrupt. This sets the starting address for the maskable interrupt to 000.070A. If the Break key or a key from the Keyboard Encoder circuits is depressed, pins 5 or 6 of U436B will go low and pin 4 will go high, driving pin 10 of U427C low. This will initiate the maskable interrupt. $\overline{\text{INT}}$ (U421-16) will also be asserted when the data buffers in the ACE are full. Pin 30 of U451 will go high, causing the CPU program counter to jump to 000.070A. The firmware will then determine which of the three circuits caused the interrupt by checking the Keyboard Status circuits, the status registers inside the ACE, and the Break Key through U433, pin 5. It will then process the data accordingly.

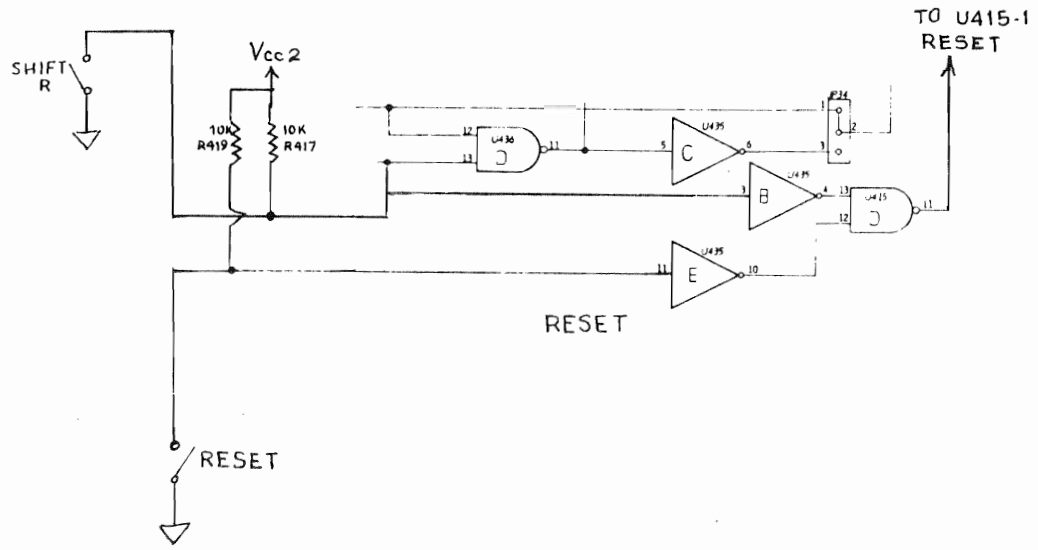


POWER-UP LOGIC AND RESET CIRCUITS

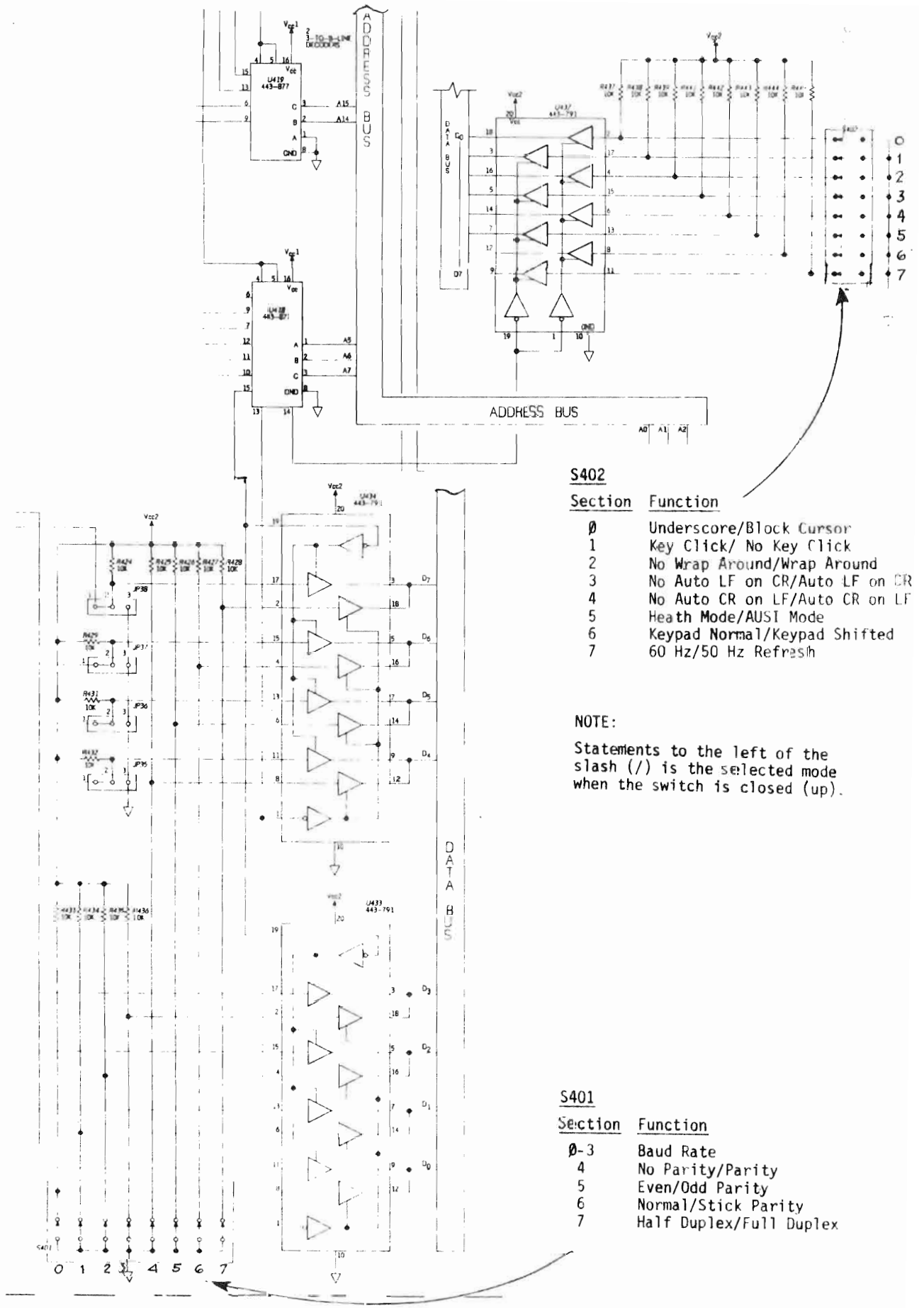


POWER-UP LOGIC

To insure that the H19 Terminal will operate in the correct mode, or to set the Terminal back to its original operating mode after extensive software modification (through Escape sequences), a reset must be performed. When the H19 Terminal is first turned on, $V_{CC}1$ will immediately go to +5 volts. U415A, pin 3 will remain at logic 1 for about 1/2-second, due to the time it takes for C414 to charge through R407. This logic 1 is inverted by U415B, which applies the reset signal to $\overline{\text{RESET}}$ of the CPU, the Keyboard Encoder, and the CRTC. U415A, pin 3 is also applied to the ACE which requires a logic 1 to reset, and to Q401, which drives the reset line on the CPU board in the H88/H89. When the H19 Terminal is turned off, $V_{CC}1$ instantly drops to zero volts. Since C414 is charged to +5 volts, D401 will conduct and quickly discharge C414. This insures a reset operation if the unit is turned off and then immediately on again.



The reset will also occur if the user presses the right SHIFT key and the RESET key at the same time. When the right SHIFT key is pressed, pin 3 of U435B will go low, placing a logic 1 on pin 13 of U415D. Pressing the RESET key will place a logic 1 on pin 12 of U415D through inverter U435E. The resulting logic Ø at pin 11 is applied to pin 1 of U415A through the de-bouncing network, R408/C415.



S402

Section	Function
Ø	Underscore/Block Cursor
1	Key Click/ No Key Click
2	No Wrap Around/Wrap Around
3	No Auto LF on CR/Auto LF on CR
4	No Auto CR on LF/Auto CR on LF
5	Heath Mode/AUSI Mode
6	Keypad Normal/Keypad Shifted
7	60 Hz/50 Hz Refresh

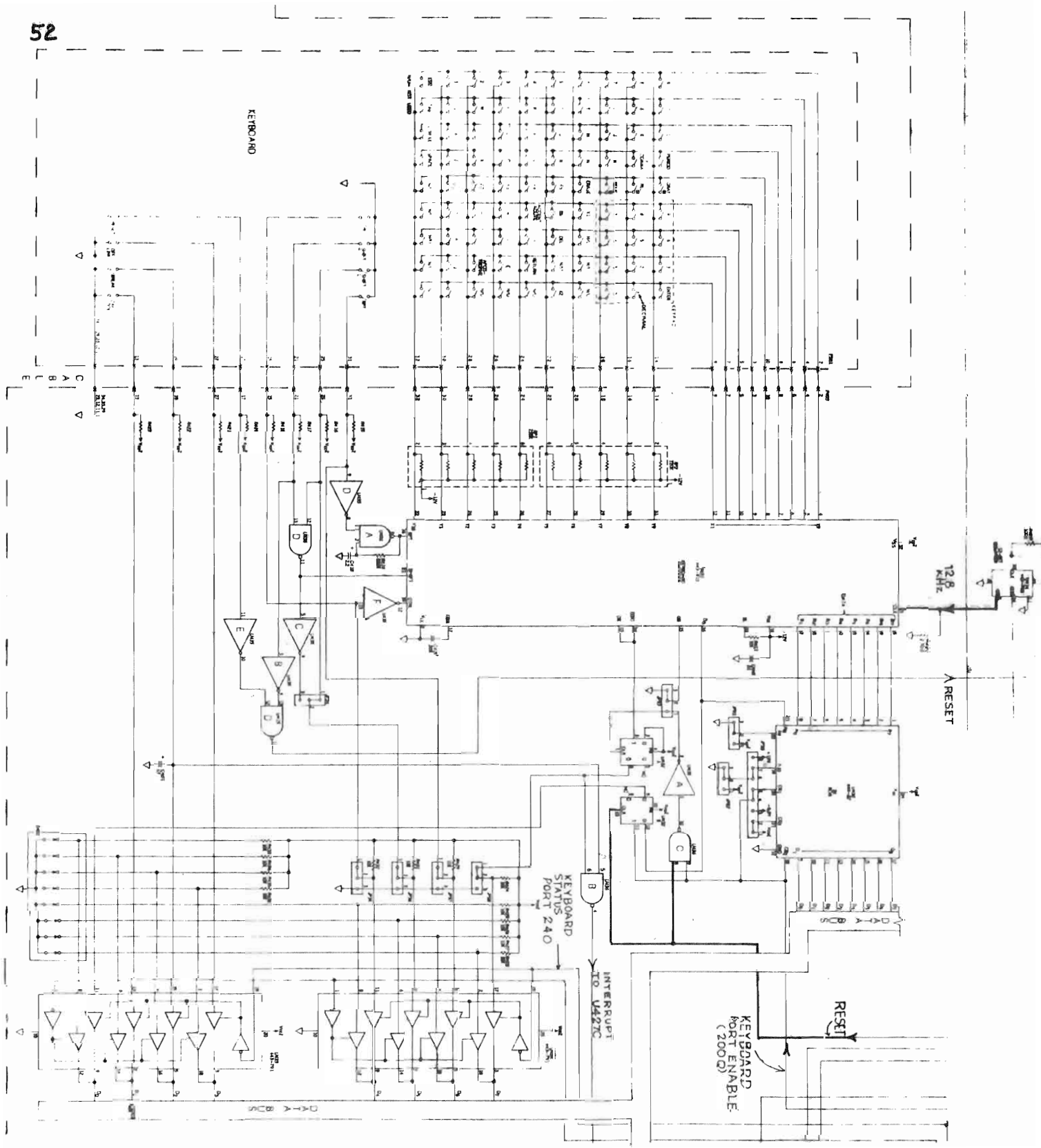
NOTE:

Statements to the left of the slash (/) is the selected mode when the switch is closed (up).

S401

Section	Function
Ø-3	Baud Rate
4	No Parity/Parity
5	Even/Odd Parity
6	Normal/Stick Parity
7	Half Duplex/Full Duplex

After reset, the program counter is set to 000.000A, the starting address of the PROM. This firmware will cause the CPU to jump to the initialization routine in the PROM prior to going to the main loop. This routine will clear the scratchpad (U424 and U425), then accesses the 8 bits of information represented by S401 (through port 000A) to set the baud rate, type of parity and full or half duplex mode for the ACE. It does this by bringing pin 1 of U433 and U434 low and reading S401 on the data bus. It will then apply a logic Ø at pins 1 and 19 of U437 to access the information at port 040A to determine Display, Keyboard, and Escape modes. The Video Display RAM will be cleared, the CRTC and ACE will be initialized and the program counter will jump to the main loop.


KEYBOARD
12.8 KHz
RESET
KEYBOARD STATUS PORT 240
INTERRUPT TO 8427C
KEYBOARD PORT ENABLE (200Q)
RESET

KEYBOARD ENCODER AND KEYBOARD STATUS

The Keyboard Encoder IC, U431, is timed by a 128 kHz clock at pin 3. This is used to develop a scanning pulse, 3.9 µs wide, that starts at output line X1, shifts it through X2, and on to X9. Approximately 70 µs later, X1 is pulsed high again. If, for example, the 'H' key was pressed, the pulse occurring at X7 time would be coupled to the Y6 input. U431 would internally decode this as an eight-bit character representing 'H'. Note that this wouldn't be an ASCII character. This is a 5740AAC encoder IC, and generates the code listed in the truth table in the #443-913 IC Data sheet rather than the ASCII code generated in the 7540AAE used in the H9 Terminal. Nine bits of this generated code are sent to U430 from output lines B1 through B9. U430 is a 2 K ROM that will translate the U431's code into ASCII. B8 is also connected to U432B, pin 12, in the Keyboard Status circuits for additional shift functions. This circuit is reserved for future expansion.

Pin 20 of U431 is the shift-lock input. This is tied to a logic 1 as the firmware in ROMs U422 and U423 provide a more sophisticated CAPS LOCK via the Keyboard Status circuits.

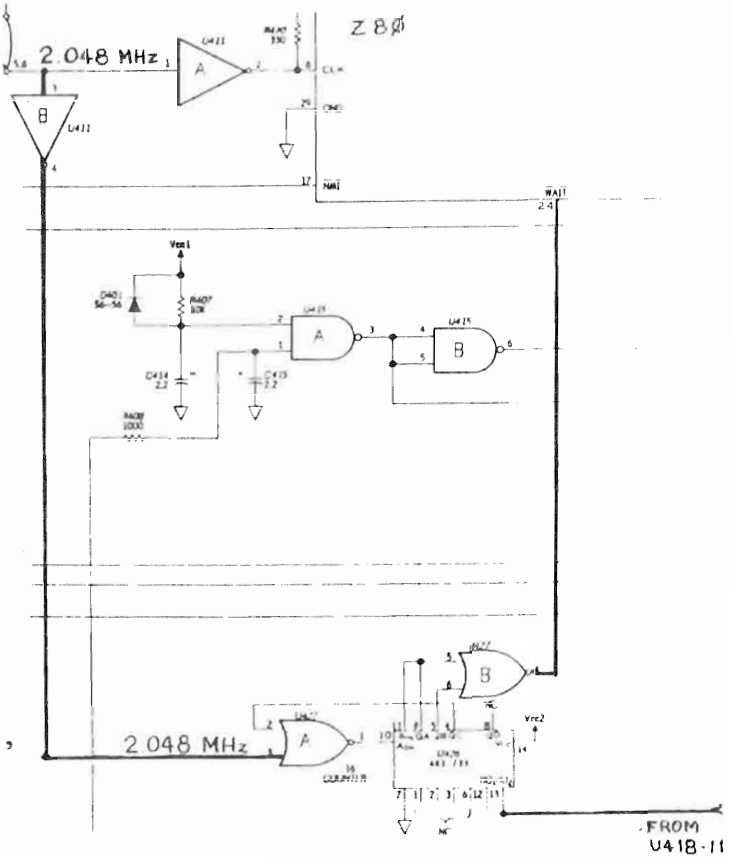
The .005 µF capacitor at pin 17 of U431 is used to eliminate key bounce.

Since U430 is enabled by a logic Ø at its chip selects (pins 18 and 20) when the I/O port 200A is addressed, U431 is set to a continuous enable state by grounding pin 15.

Pin 13 of keyboard encoder U431, is the data strobe output. It is connected to the data strobe control (pin 14), which limits the data strobe to 7.8 µs (one cycle of 128 kHz). This

data strobe is also sent to U432A, pin 3. U432A is cleared by the reset logic from U415B (pin 6). When the reset line goes low, it is inverted, first by U436C, and then by U435A, which presets U432A's $\overline{Q}$ output, pin 6, to a logic 1. The D input of this flip-flop is connected to +5 volts so that a data strobe will toggle the $\overline{Q}$ output to a logic Ø when a key is pressed on the keyboard. This logic Ø connects to U436B, pin 6, and drives the output of U436B, pin 4, to a logic 1, interrupting the computer via U427C. At this point, the CPU will go into its interrupt handling routine to process the keyboard data. When the CPU accesses the Keyboard encoder through port 200A, the logic Ø from U418, pin 11, will be coupled through U436C and U435A to clear U432A and turn off the interrupt line.

To insure valid logic levels on the data bus, the CPU will wait four clock cycles (2.048 MHz) before processing the data from the Keyboard Encoder. It does this with U426, U427A, and U427B. As long as RO1 and RO2 of U426 are high, outputs QA and QB will be logic Ø, so the $\overline{WAIT}$ line to the CPU isn't asserted. When the CPU drops U418, pin 11 to logic Ø to access the keyboard



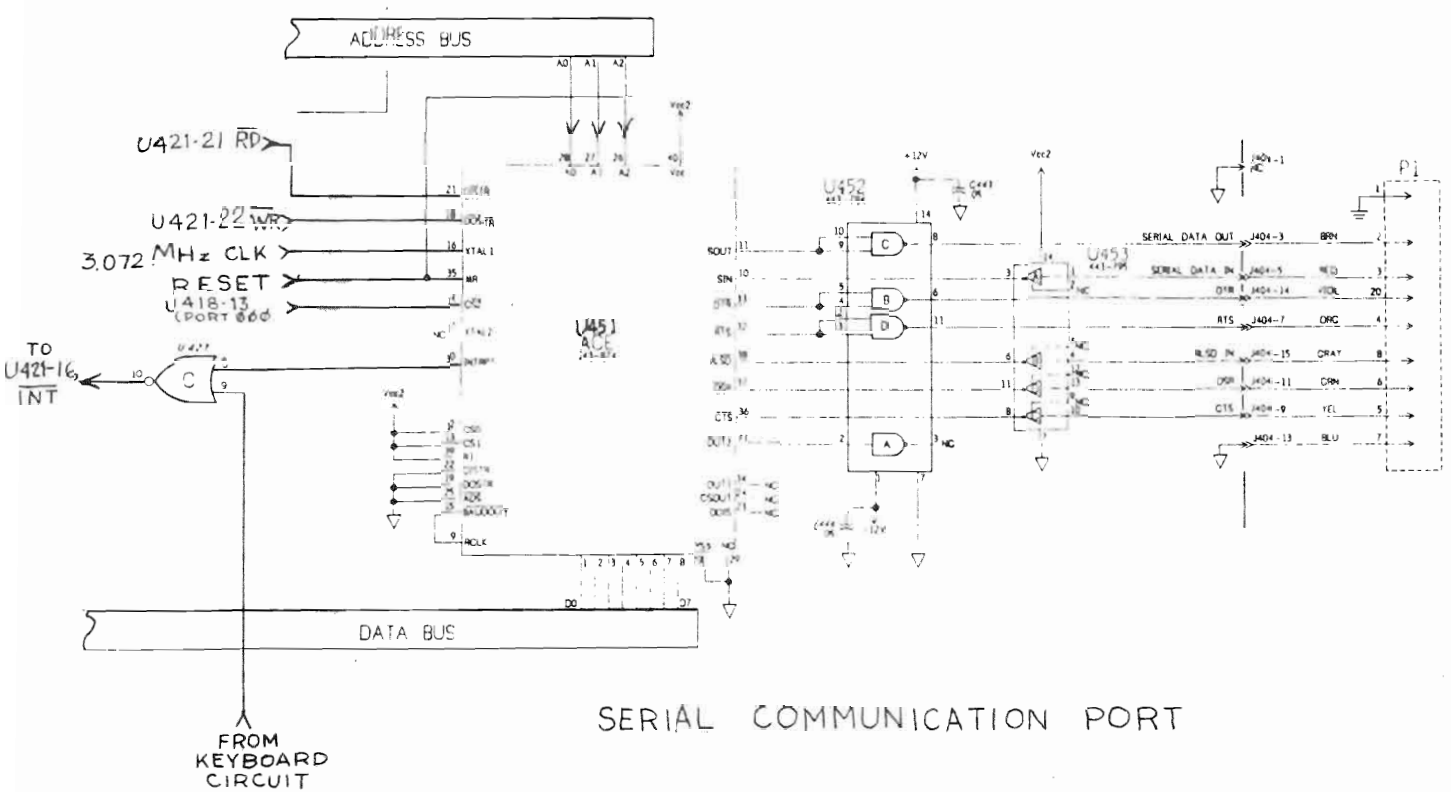
Encoder, it enables U426, a 4-bit binary counter wired for divide-by-3 operation. Since AC of U426 is low, then U427A will pass the 2.048 MHz clock pulses present on pin 3. For the next three clock pulses, QA, and then QB, and then both these outputs, will be high, which will maintain a logic Ø on the $\overline{\text{WAIT}}$ line, halting CPU operation.

On the fourth clock cycle, QA and QB will go to logic Ø, which reactivates the CPU, and QC goes to logic 1, which locks out the clock pulses at U427A until the CPU is finished servicing the Keyboard Encoder and U426 is again disabled. The Z80 automatically inserts one wait state during an I/O operation, so the wait state has been extended for a total of four clock cycles.

There are three other circuits that affect U431's operation. The REPEAT key will apply a logic 1 to pin 1 of U436A (through inverter U435D), which will enable the oscillator made up of U436A, R414, and C418. The time constant of this resistor and capacitor sets the repeat rate to about 15 characters per second. The repeat line to U434, pin 15 is reserved for future expansion.

If either SHIFT key is pressed, pin 11 of U436D will go to a logic 1, informing the Keyboard Encoder that a shift operation is to take place. U435C and the left-shift line to U434, pin 13 are reserved for future expansion.

The CTRL key is inverted by U435F to a logic 1 so the Keyboard Encoder can process a control function. The control line to U434, pin 11 is reserved for future expansion.



SERIAL COMMUNICATION PORT

Backing up to when the 'H' key was pressed, recall that U432A, pin 6 went to a logic Ø to interrupt the CPU. In order for the CPU to determine that it's the Keyboard Encoder that wants attention, it addresses the Keyboard Status circuit at port 240A. If it senses a logic Ø on pin 3 of U434, it will know that the Keyboard caused the interrupt. It will also check the OFF LINE key at U433, pin 3 to determine if the data is to be routed to the CRT or to the ACE (or to both if in the half-duplex mode). The BREAK key is also checked at pin 5 of U433 to make sure that it wasn't this line that caused the interrupt. C421 eliminates switch contact bounce. If the CAPS LOCK key is latched to its closed position, the CPU will mask the character to upper case (if it is a lower-case alphabetic character) when it accesses the Keyboard Encoder. Thus, the keys that serve two characters (such as the numeric keys) won't be shifted as they would be if the shift-lock line had been used (pin 20, U431).

SERIAL COMMUNICATIONS PORT

The Serial Communications Port is dominated by the Asynchronous Communications Element (ACE). This device permits the CPU to talk to the outside world. Essentially, the ACE does both parallel-to-serial and serial-to-parallel conversion, handles any parity processing, and provides any required handshaking.

When a reset condition occurs, pin 35 of the ACE (U451) is brought high and all internal registers are cleared or affected, except for the receiver buffer, transmitter holding register, and divisor latches (which determine baud rate). See the data sheet in this book for more information on the ACE.

Timing, supplied by the Master Clock, is divided down to 3.072 MHz and applied to pin 16 (XTAL1). XTAL2 isn't needed unless a crystal and RC network had been used.

In order to operate properly, certain registers in the ACE must be set to certain states. This is done by the CPU during initialization immediately after a reset. The CPU will address the ACE through the I/O decoder, U418, by bringing U418, pin 13 to a logic Ø (port 100A). This is applied to $\overline{CS2}$ (pin 14) of the ACE. At the same time, a unique address will be placed on AØ, A1, and A2 of the address bus, telling the ACE which of its internal registers will be accessed. When the initialization information becomes valid on the data bus, the CPU will issue a write command by bringing U451, pin 18 ($\overline{DOSTR}$) low. The information on the data bus will then be loaded into the appropriate register in the ACE. The baud rate will be set according to the switch positions of S401, which will set up the ACE's baud rate register to divide the incoming 3.072 MHz by such a factor that the internal transmit clock will be 16 times the desired baud rate. This 16x clock is outputted through $\overline{BAUDOUT}$ (pin 15) to pin 9 (RCLK) for proper receiver timing. Any parity information (odd, even, stick, or no parity) contained on S401 is next programmed into the ACE.

When the CPU needs to transmit data, such as when a key is pressed on the keyboard in the On-Line mode, the CPU will select the ACE in the same manner that it did when it initialized it. U418, pin 13, is used in conjunction with the lower three bits of the address bus to select the transmit register. When the data bus information is valid, $\overline{DOSTR}$ is asserted and the ACE will load the data, format it with the necessary stop bits, add any parity bits, and send it out at pin 11 as a serial bit stream.

On receive, the serial data entering the ACE at pin 10 will be placed in the internal receiver buffer register, causing an interrupt to be generated. Pin 30 (INTRPT) will go to logic 1, which will interrupt the CPU through U427C. The CPU will address the Interrupt Identification Register inside the ACE by asserting the port 100A line and placing the correct address on pins 28, 27, and 26; and then performing a memory read by bringing pin 21 low ($\overline{\text{DISTR}}$). Seeing that it's incoming data, the CPU will transfer this now-parallel information into a 128-byte buffer in the scratchpad RAM via the data bus. If the incoming data is too fast for the CPU to process, such as at 9600 baud, the CPU will send a 'control-S' (X-OFF) via the ACE to the external device to halt any more incoming information. This occurs when there is only 16 free bytes left in the scratchpad. When the CPU has processed enough data that there is at least 32 bytes free, it will send a 'control-Q' (X-ON) to tell the external device to continue transmitting. If the outside terminal isn't programmed to respond to a CTL-S, and continues to transmit data, the H19 Terminal will sound its bell when the 128 byte buffer is full. Any overflow data will be lost.

Five handshake lines are used by the H19 Terminal, two for transmit, and three for receive. These are required by some terminals such as MODEMS.

The $\overline{RLSD}$ is the Received Line Signal Detect and will be asserted whenever an externally connected MODEM detects incoming data. The DSR (Data Set Ready) will be asserted low when the MODEM or other device is ready to establish communications with the Terminal. The Clear To Send ($\overline{CTS}$) will assert when the external device is ready to accept data.

The $\overline{DTR}$ is the Data Terminal Ready and when asserted, will tell the external device that the H19 Terminal is ready to communicate. The $\overline{RTS}$ (Request to Send) is brought low when the H19 Terminal is ready to transmit data. $\overline{OUT2}$ is a programmable output currently reserved for future expansion.

Note that the ACE responds to a *change in state* of these handshakes and not to their levels. If a handshake should change states, the ACE will generate an interrupt which causes the CPU to look at the ACE registers that contain the status of the handshake lines. It will then process the data accordingly. If the lines are disconnected (as when the H19 Terminal is connected to an H8-5 board), then the handshake lines will remain at a steady state, and both the CPU and the ACE will effectively ignore them.

The Address Strobe ($\overline{ADS}$) isn't required, and so is permanently enabled by grounding it. This is true of the asserted-high versions of the Data Input and Output Strobes (DISTR and DOSTR), which are disabled. The unused chip selects (CSØ and CS1) are

permanently enabled by tying them to logic 1. Logic 1 is also used to disable the Ring Indicator ($\overline{RI}$). CSOUT, DDIS, and $\overline{OUT1}$ are all outputs. $\overline{OUT1}$, pin 34 is a user-programmable output that currently isn't accounted for in the firmware. $\overline{CSOUT}$, pin 24, will go high whenever the ACE is selected on pin 14. $\overline{DDIS}$, pin 23, will go low whenever the CPU is reading data from the ACE.

The output lines from the ACE are sent to a quadruple line-driver, U452, where the TTL levels are converted to the +12 volt (logic Ø or space) or -12 volt (logic 1 or Mark) required for the RS232C communications.

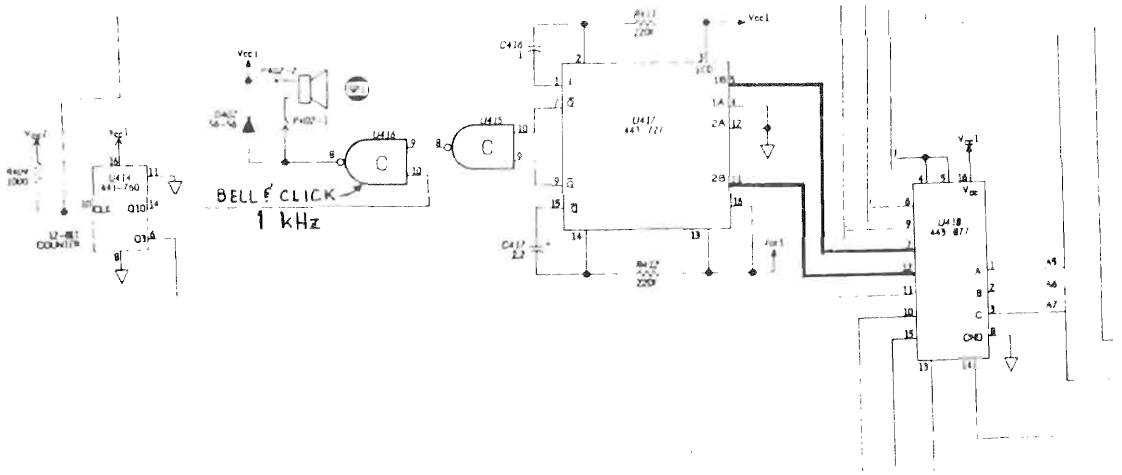
The incoming data is handled by U453. Since the control lines are not connected (pins 2, 5, 12, and 9), this quadruple line receiver will respond to signals at TTL levels and above.

The Serial I/O circuits connect to external devices through a standard DTE (Data Terminal Equipment) D connector.

BELL AND CLICK

The purpose of the Bell is to inform the user that an event has occurred or is about to occur. Traditionally, the bell is used to inform the typist that the printing mechanism or cursor is nearing the end of the line. Many professional video terminals do not provide an end-of-line bell. The H19 Terminal falls in this category; it is up to the software to supply the bell. The bell will sound when control-G is entered on the keyboard or an octal '7' is received from the external device.

The reason for the click occuring when a key is tapped is psychological. The user feels more comfortable when the acoustic feedback informs him that the switch contact has actually closed. As mentioned before, this can be disabled through hardware (S402) or through software (entering the correct Escape code).



When the CPU wants to ring the bell, it brings U418, pin 12 to a logic Ø (port 340A) which pulses U417, pin 11, a retrig-gerable monostable multivibrator. This will cause the output, pin 9, to go to a logic Ø for 200 ms, which is set by the time constant R412 and C417. This logic Ø on the input of U415C drives pin 9 of U416C to a logic 1, which gates the 1000 cycle

clock to the speaker. D402 is used to shunt any excessive voltage to the +5 volt supply that may be caused by inductive kickback from the speaker coil.

The click is generated when the CPU addresses I/O port 300A. The negative-going pulse at U417, pin 5 will cause pin 7 to go to logic Ø for six milliseconds (determined by R411 and C416), gating the 1 kHz tone to the speaker only long enough to have a 'click' sound.

The 'clear' lines to U417 are connected to logic 1 to insure that this IC will always be enabled. To prevent triggering by the 'active high' inputs, pins 4 and 12 are grounded.

CHARACTER GENERATION AND DISPLAY

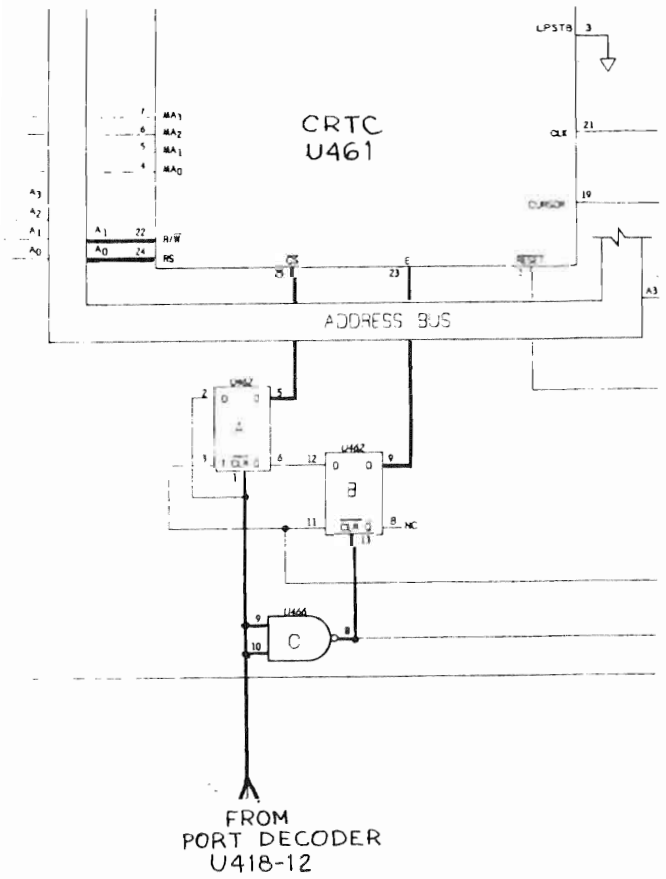
The nucleus of the character generation and display system is the CRT Controller (CRTC), R461. This IC determines when data should be transferred from the display RAM to the character generation circuits, where the cursor should be placed, and when blanking, vertical and horizontal synchronization pulses should occur. The CRTC has two major modes of operation: a video processing mode where the characters are fetched from display memory, converted to dots, and sent to the video amplifier; and a register-access mode that allows the CPU to read or write any of the CRTC's nineteen internal registers.

Four control lines are used to transfer information on the data bus to or from one of the internal registers:

1) $\overline{CS}$ (pin 25): When the $\overline{Chip\ Select}$ line is asserted, it tells the CRTC to stop processing video data and prepare to have its internal registers written into or read from.
2) E (pin 23): $\overline{CS}$ must be asserted before the Enable (E) line is brought high. Then when the E input is again brought low, the falling edge will clock any data in the registers out to the bus or from the bus to the selected registers, depending upon the logic states of RS and R/$\overline{W}$.
3) RS (pin 24): This is the register select line. The CPU indirectly selects the register it wants to program by loading the register location into an address register (inside the CRTC) via the data bus when pin 24 is logic Ø. The CPU will then read or write the information at one of the eighteen registers pointed to by the address register when RS goes to logic 1.
4) R/$\overline{W}$ (pin 22): The logic state on this line will tell the CRTC whether the register being accessed is to be read from or written into. A logic Ø is a write command, logic 1 is a read command.

The CRTC must be initialized by the CPU before it can function. Prior to initializing the CRTC, the CPU will load the scratch-pad RAM with the information that the CRTC requires for proper display. The type of cursor (block or underscore) and the refresh reate (50 Hz or 60 Hz), is supplied by S402 while other data, such as the number of horizontal lines, sync timing and cursor home position is loaded into the scratchpad from the ROMs (U422 and U423). This data will later be transferred to the CRTC internal registers.

There are seventeen registers (including the address register) in the CRTC that determine the horizontal and vertical display, the type and position of the cursor and the type of scan that is to be used (interlace or non-interlace). There are also two light pen registers, currently not being used. The MC6845 data sheets (#443-906) provide a detailed discussion of these registers.



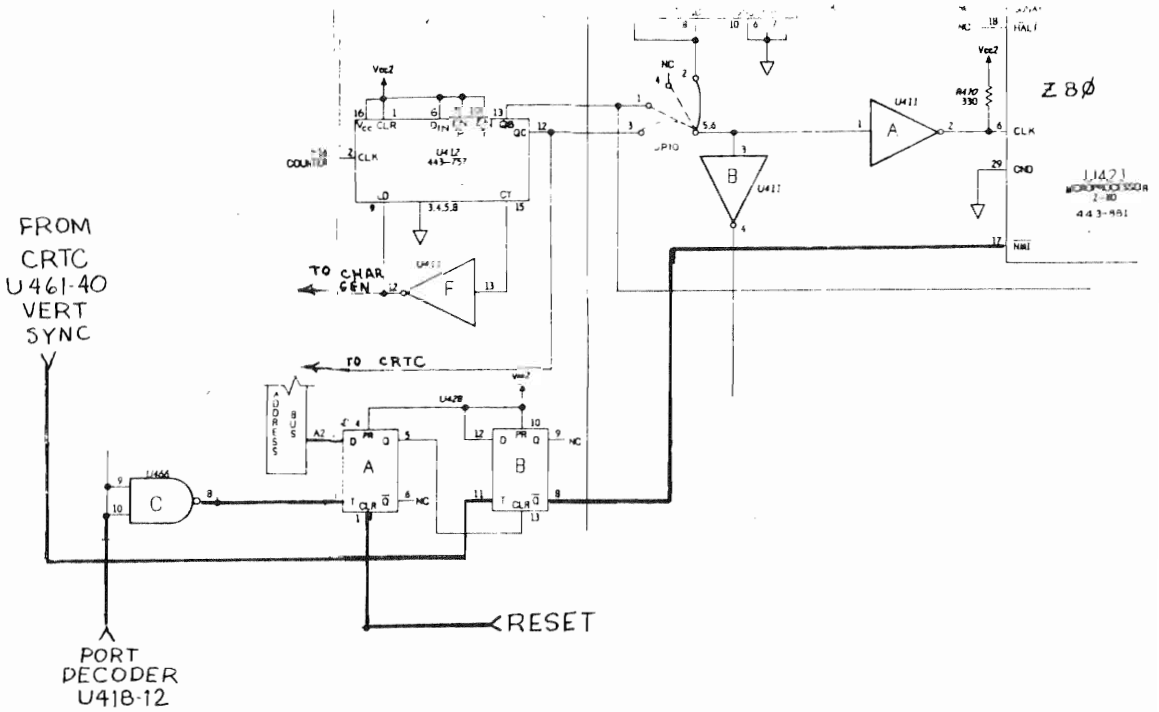
To initialize the CRTC, the CPU sends an I/O request to U461 by addressing port 140A. Port Decoder, U418, pin 12 goes to logic Ø. This clears U462A and transfers the logic Ø to pin 25. At the same time, the output of U466C, pin 8, goes to logic 1, removing the 'clear' from U462B. The logic 1 on U462, pin 6 is passed to U462, pin 12; so when the next CPU clock pulse occurs, U462, pin 9 will also toggle to a logic 1. This insures that there is at least one clock cycle delay between the time $\overline{CS}$ is asserted to when U461, pin 23 (E) goes high. Address line A1 will be logic Ø to tell the CRTC that this is a write operation (pin 22), while address lines AØ (U461, pin 24) is also logic Ø to indicate that the information on the data bus is to be loaded into the CRTC's address register. The $\overline{IORQ}$ and $\overline{WR}$ lines on the CPU will go to a logic 1 approximately 1/2 clock cycle before the information on the data bus becomes invalid. This causes Port

Decoder U418, pin 12 to go to a logic 1, which is inverted by U466C to clear U462B. The falling edge at U461, pin 23 will clock the data on the data bus (CRTC, pins 26 through 33) into the CRTC's address register. One clock cycle later, the logic 1 on pins 1 and 2 of U462A will be transferred to U461, pin 25, taking the CRTC out of the register-access mode.

The CRTC's address register now holds the address of the internal register that is to be programmed. The CPU will again address port 140A and assert $\overline{CS}$ through U462A, pin 5 and then assert U461, pin 23 one clock cycle later via U466C and U462B, pin 9. This time, the CRTC's register-select line, RS pin 24, is logic 1, while the Read/$\overline{Write}$ line is still logic Ø. When the enable line (U461, pin 23) is brought low, the programming information on the data bus will be latched into the CRTC register that is specified by the address register.

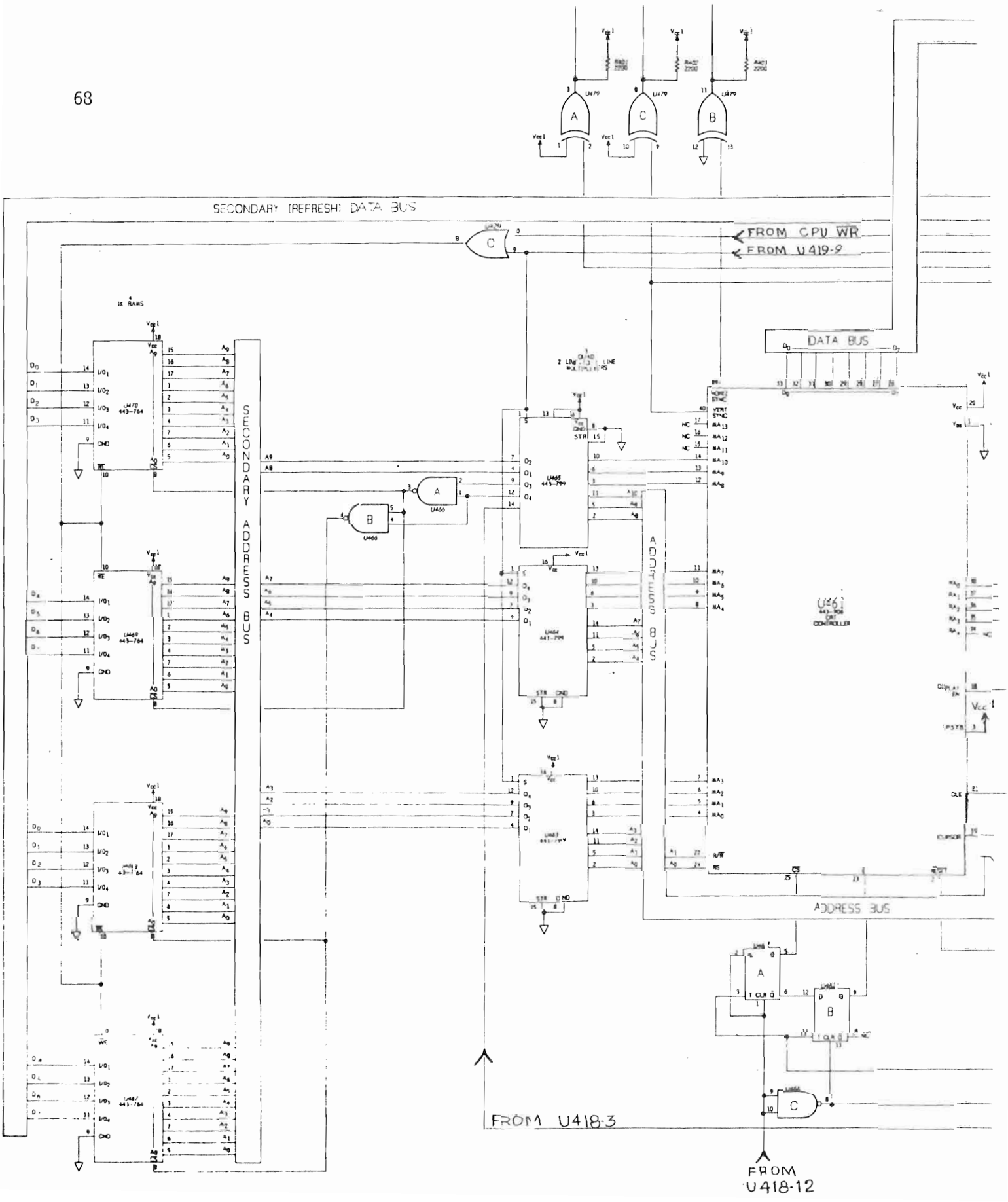
The CPU will continue this procedure, sending an address to the CRTC's address register, then sending data to the register selected by the address register. The CPU will program all CRTC registers, starting at address 000A to the 'Cursor (L)' register, 017A, in this manner. See Table 2, CRTC Internal Register Assignment in the IC Data Section.

Periodically, the CPU must update the contents of the CRTC registers, This can include updating the current cursor position, number of lines to be displayed, type of cursor to be displayed and any scrolling information.* It does this by allowing the CRTC to send a non-maskable interrupt (NMI) to the CPU during vertical retrace time.



U427A and U428B will trigger the NMI. Normally these ICs are in the cleared state (pins 5 and 9 are zero). When the system is turned on (or reset), U428B, pin 13 is latched to a zero, placing a logic 1 on U421, pin 17 ($\overline{NMI}$). When the CPU has to update the CRTC, it will place a logic 1 on A2 of the address bus and access I/O port 140A through U418. The logic Ø on pins 9 and 10 of U466C will be inverted by this

*Rather than move the ASCII data from one display RAM location to another, scrolling is more quickly performed by programming the CRTC to address a different display memory location at the start of vertical or horizontal sweep. This allows the display to be scrolled by line, page, or character. See "Programming Considerations" (#443-906 IC Data Sheet).


SECONDARY (REFRESH) DATA BUS
FROM CPU WR
FROM U419-9
DATA BUS
SECONDARY ADDRESS BUS
ADDRESS BUS
FROM U418-3
FROM U418-12

IC and fed to the clock input of the positive edge-triggered flip-flop, U428A, pin 3, transferring the "1" on pin 2 to the Q output. This enables U428B. At the end of the vertical sweep, the CRTC will generate a vertical sync pulse that is coupled to pin 11 of U428B. Since pin 12 of this flip-flop is wired to a logic 1, pin 8 will go to logic Ø, initiating a non-maskable interrupt. The CPU will then jump to the NMI handling routine in ROM (U423 and U422) to update the CRTC. Prior to returning to the main loop, the CPU will restore U428A and B to their cleared state.

The other pins on the CRTC are used for processing video information. Memory Address lines MAØ to MA10 (pins 4 to 14) point to one of the 2000 characters in memory to be converted to dots. Row Address lines RAØ to RA3 (pins 38 to 35) select the scan line of the ASCII character that is to be converted to dots. The Display Enable (pin 18) will go to a logic 1 to unblank the CRT when the dot information is to be displayed and to a logic Ø during retrace to provide retrace blanking. The clock input (pin 21) is fed a 1.536 MHz signal to process the data at a character rate. When the cursor is to be displayed, pin 19 is brought to a logic 1. When the $\overline{\text{RESET}}$ line is asserted, some of the CRTC registers will be cleared. The logic 1 at the light pen status strobe (LPSTB) prevents a total reset. If pin 3 of the CRTC were logic Ø, a reset would kill the horizontal sync pulse, which would cause a bright vertical line on the CRT, similiar to what is seen prior to powering-down the H19 Terminal. The ROMs (U422 and U423) will take care of any unreset registers during initialization.

Horizontal and vertical sync pulses are generated at pins 39 and 40 respectively.

The major components in the video processing circuitry are the CRTC, three quad 2-line to 1-line multiplexers (74LS157), the display RAMs (2114), character buffer, and character generator ROM (#444-29), and the video timing circuits.

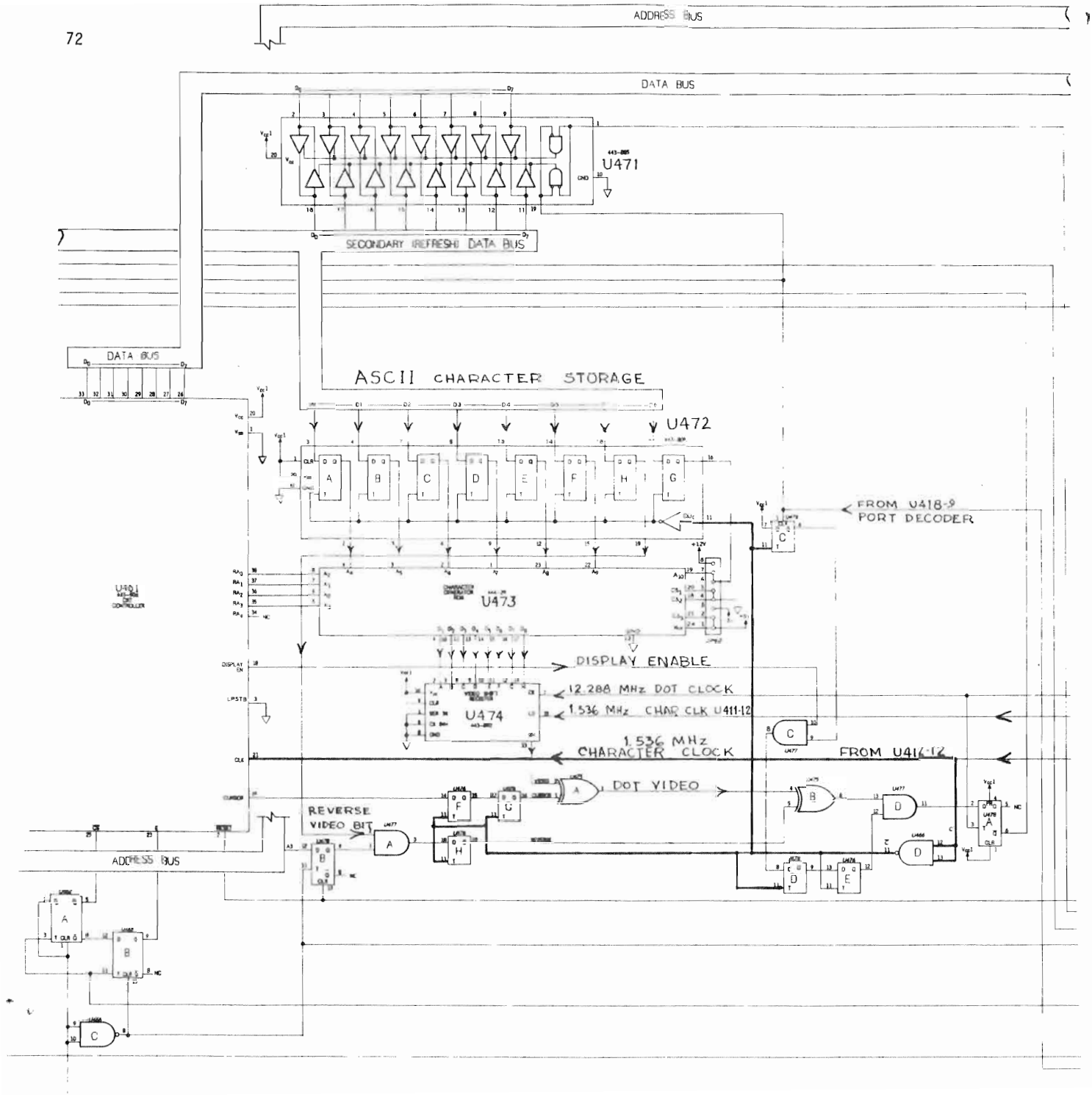
Starting at the first character position to be displayed, the CRTC will sequentially address each of the 2000 character addresses. It does this by connecting MAØ through MA10 (pins 4 through 14) to the display RAMs via multiplexers U463, U464, and U465. The multiplexers act as electronic switches to gate between the CPU address bus and the CRTC memory address lines. The CPU address bus is connected to the "A" input pins (2, 5, 11, and 14) of U463 through U465, while the CRTC address bus is connected to the "B" inputs (pins 3, 6, 10, and 13) of these ICs. The logic state on pin 1 will determine whether the data on "A" or "B" will be coupled to the secondary address bus (via pins 4, 7, 9, and 12).

In the video processing mode, these multiplexers are set to transfer the address information from the CRTC. The select line (pin 1) of ICs U463 through U465 connects to the memory decoder, U419, pin 9 (address 370.000A). This line is a logic 1 when the CPU isn't accessing the display RAMs, so the multiplexers will couple the CRTC address line data to the secondary address bus and to U466A and B. This logic 1 is also coupled through U429C to pin 10 of the display RAMs (U467 to U470), placing them in the "read" mode.

The 'B' input, pin 13 of U465, is connected to logic 1, which is passed to pins 1 and 4 of U466, enabling gates A and B. The CRTC can now access the first 1024 bytes of memory by setting the memory address lines MSD (U466A, pin 2) to logic Ø. This places a logic 1 on U466B, pin 5, driving the $\overline{CS}$ lines (pin 8) of U467 and U468 to logic Ø. The selected data byte will then be transferred to the secondary (refresh) data bus. The information on the secondary address bus will not affect the upper 1 K of RAM (U469 and U470), until U465, pin 9 goes to logic 1, driving U466, pin 3 to zero (chip selecting U469 and U470) and placing a logic 1 on U466B, pin 6 (disabling U467 and U468).

The selected data on the refresh bus is connected to two ICs, U471 and U472. U471 will not be affected as pin 19 is at logic 1 (from U418, pin 9) and thus disabled. However, the data will be latched into the octal D flip-flop, U472, when clocked by the $\overline{C}$ pulse which is the character clock from U412, pin 12, inverted by U466D.

The ASCII character (DØ-D6) will be stored in flip-flops A through G. The eighth bit (D7) is the reverse video bit and is a logic 1 if the character is displayed in the reverse video mode. D7 is stored in the 'H' flip-flop and sent to the reverse video processing circuits. The seven bit ASCII character is sent to inputs A4 through A10 of the character generator ROM, U473. The other address lines, AØ-A3 come from row address outputs (RAØ-RA3) of the CRTC. This 11-bit address will cause U473 to output a patterns of 1s and Øs on lines O1 through O8 (pins 9, 10, 11, and 13 through 17) that represents the dot information for that character for that scan line.


ADDRESS BUS
DATA BUS
U471
SECONDARY (REFRESH) DATA BUS
DATA BUS
ASCII CHARACTER STORAGE
U472
FROM U418-9
PORT DECODER
U473
DISPLAY ENABLE
12.288 MHz DOT CLOCK
U474
1.536 MHz CHAR CLK U411-12
1.536 MHz
CHARACTER CLOCK
FROM U416-12
DOT VIDEO
REVERSE
VIDEO BIT
ADDRESS BUS

This data is sent to the parallel input of the video shift register U474 from 01 through 08. A pulse occurring at the character clock rate (from U411F) at pin 15 of U474 will load this parallel data into the shift register. The dot clock is applied to pin 7 to shift this data out serially at eight times the character clock rate (since an 8 x 10 matrix is being used). This serial dot (video) information is coupled from U474, pin 13 to pin 2 of exclusive-OR gate, U475A.

The cursor information is added to it at this point at pin 1. The CRTC cursor output line (pin 19) will go to a logic 1 when the cursor position (pointed to by the cursor address register in the CRTC) coincides with the character being addressed by lines MAØ through MA1Ø. However, when the data was transferred through U472 and U474 at the character clock rate, the dot information representing the character has been delayed by two character clock times. In order for the cursor to appear to the right of the proper character and not one character position left of it, the cursor must also be delayed by two character clock periods. This is done with U476F and U476G, part of another octal D flip-flop. Both T inputs (pin 11) are clocked by the inverted character clock ($\overline{C}$). One character clock time after the cursor line at pin 14 is asserted, it will be transferred to the 'D' input of U475G. The second character clock will transfer this logic 1 to pin 1 of U475A.

Unless the H19 Terminal is in the graphics mode*, there won't be any dot information from U474, pin 13 as the CRTC row address counters are pointing to the ninth scan line beneath that character location. The dot or cursor information is coupled from U475A to pin 4 of U475B where it is combined with any reverse video information at pin 5.

U477A is the focal point for reverse video processing. Pin 1 is normally held to a logic 1 by the output of U478B, the reverse video disable latch. A reset places the logic 1 at the $\overline{Q}$ output of U478B, allowing reverse video characters to be displayed as reverse video. To disable reverse video, A3 of the address bus must be held to logic 1 while the CPU addresses port 140A, pulsing pin 11 high. This will couple a logic Ø from pin 8 of U478B to U477A, disabling this gate.

In early production runs, U478B will remain in its reset position. It is reserved for future expansion.

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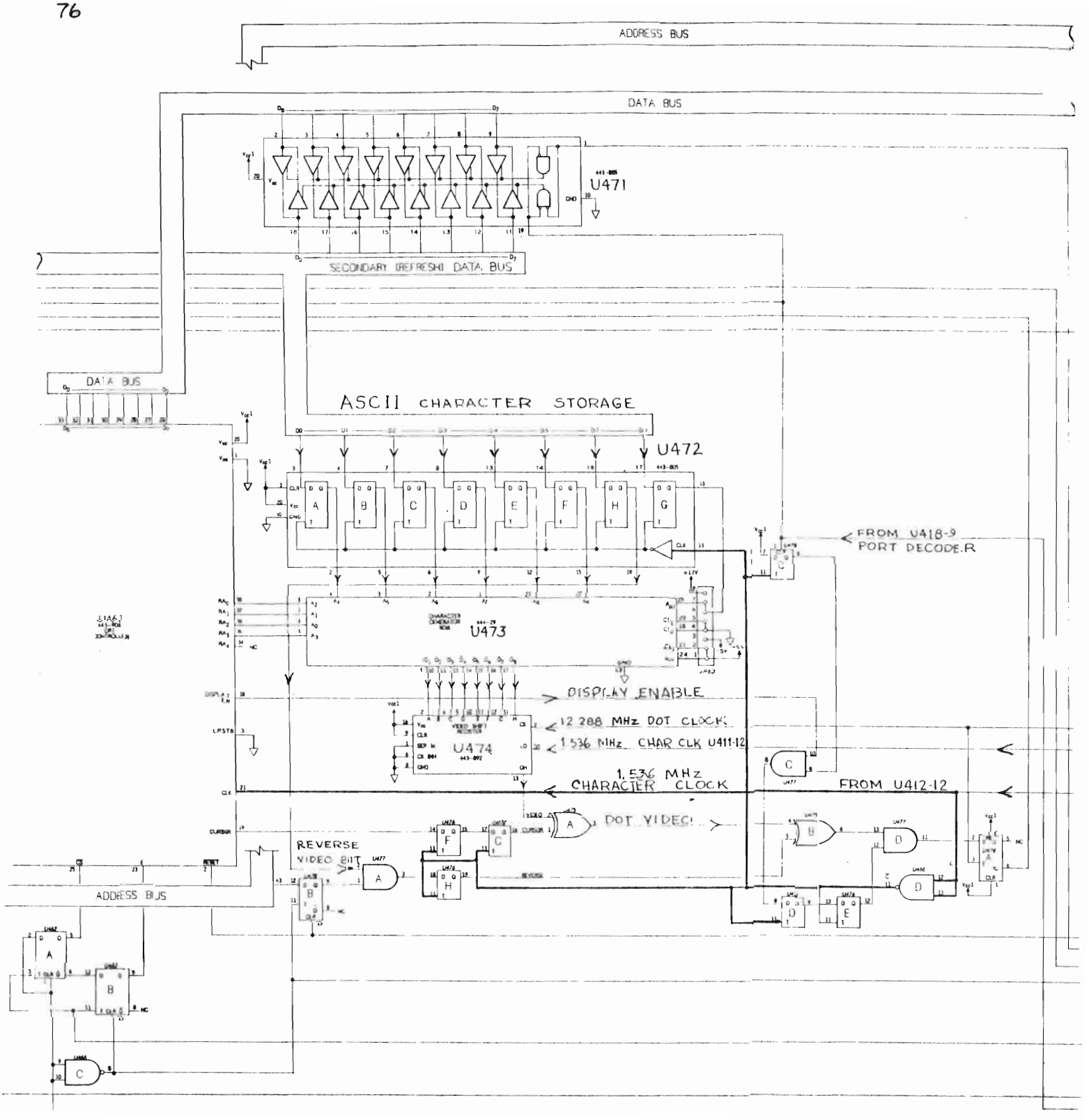
*If a graphics character is to be stored in display RAM, the CPU will first convert it to what is considered to be a non-displayable character by ANDing it with 037Q. When the character generator encounters this non-displayable character, it recognizes it as a graphic character and decodes it accordingly.

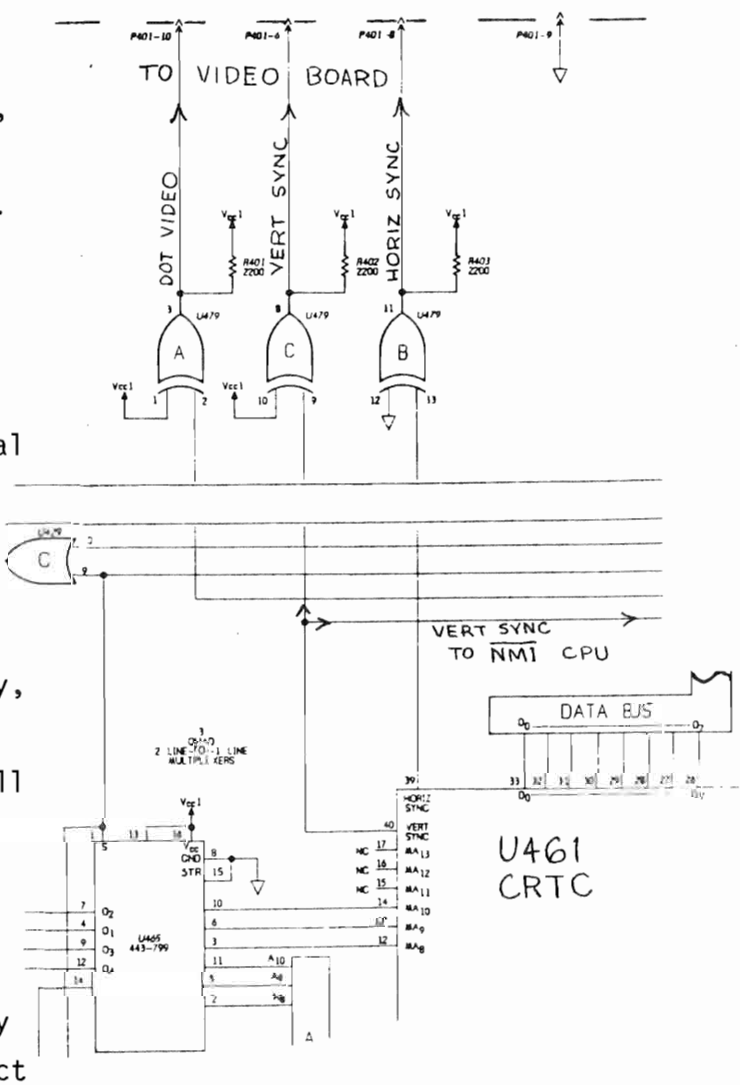
On a transmit page, when the CPU encounters a graphic character in the display RAM, it will convert it back to a displayable character, insert the proper Escape codes and transmit it on out the serial port.

When a reverse video character is loaded into U472, U477A, pin 2 will go to a logic 1. This logic 1 is applied to the 'D' input of U476A where the 'Q' output is asserted one character clock later. This one character delay compensates for the added delay caused by the data transfer in U474. The reverse video information is then coupled to pin 5 of U475B, along with any dot or cursor information at pin 4. The composite output is then coupled to U477D, pin 13, part of the blanking circuit. Pin 12 of this IC is the display blanking input.

Retrace blanking is provided at U461, pin 18, the Display Enable output. This line is normally a logic 1, and drops to a logic Ø at horizontal and vertical retrace time to prevent display of the retrace lines. This blanking/unblanking information is coupled to pin 10 of U477C. Unless the CPU is reading from or writing to the display memory, U477C, pin 9 is a logic 1, allowing the display enable information to be passed through this gate on to U476D, pin 8. U476D and U476E are clocked by the inverted character clock and provide a two character delay. If this delay wasn't present, it would be possible for the first two characters to be blanked in every character line. If the video signal is to be enabled, U476E, pin 12 will go to a logic 1. The video information is then presented to U478A, pin 2. This flip-flop is clocked at the dot clock rate (12.288 MHz) to provide approximately an 80 nanosecond delay in the video information. This retiming of the video information is necessary to compensate for the added propgation delays caused by the flip-flops, gates, and other character processing circuits that the video signal passed


ADDRESS BUS
DATA BUS
U471
SECONDARY (REFRESH) DATA BUS
DATA BUS
ASCII CHARACTER STORAGE
U472
FROM U418-9
PORT DECODER
U473
DISPLAY ENABLE
12.288 MHz DOT CLOCK
U474
1.536 MHz CHAR CLK U411-12
1.536 MHz
CHARACTER CLOCK
FROM U412-12
DOT VIDEO
REVERSE
VIDEO BIT
ADDRESS BUS

through. The video signal is inverted at U478A, pin 6 and coupled to U479A, pin 2, where it is again inverted due to the logic 1 on pin 1. Horizontal synchronization pulses are coupled from pin 39 of the CRTC, to buffer U479B, pin 13, and sent on to the video board. Vertical sync is inverted by U479C before being sent on to the video board.



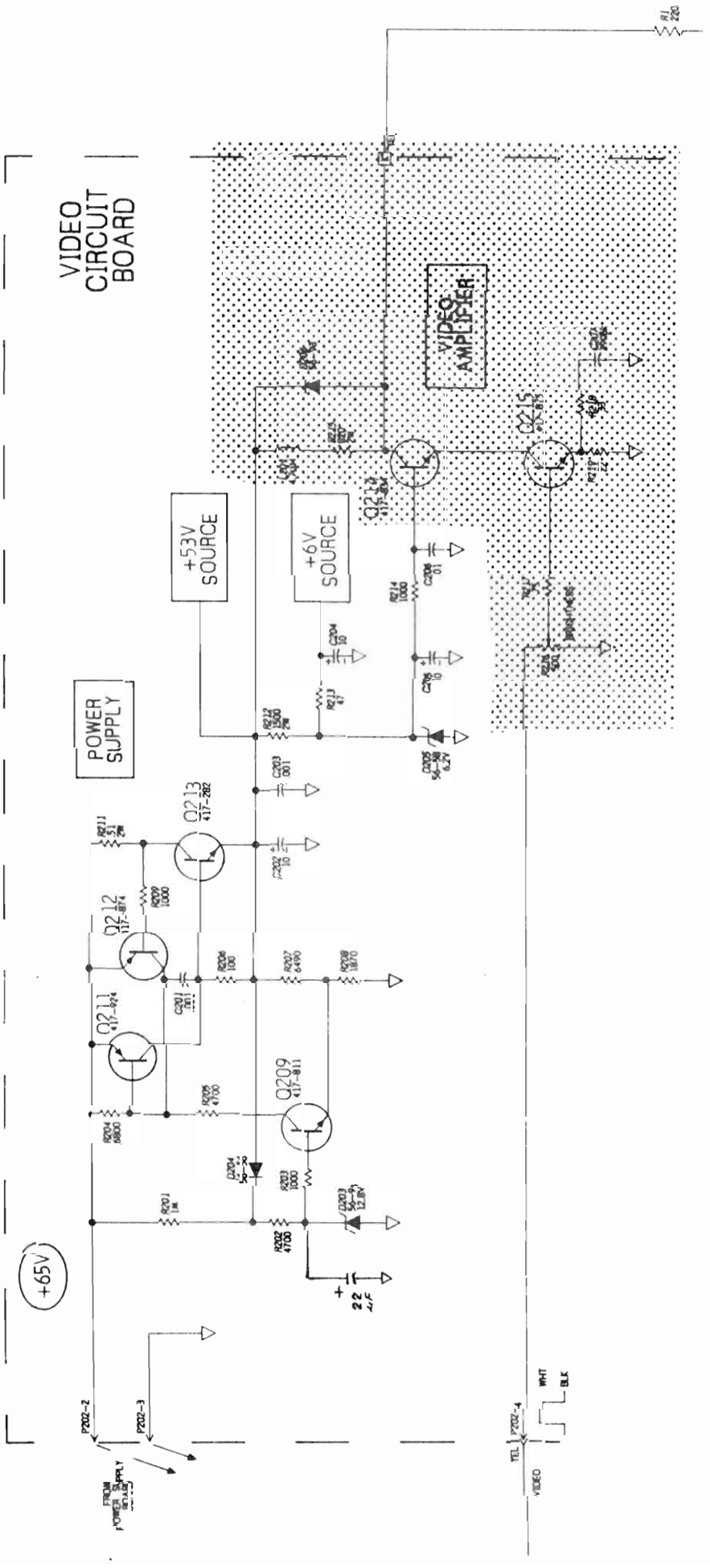
To access the display memory, the CPU will perform three preliminary actions. It will cause the two line-to-one multiplexers, U463-U465 to lock out the CRTC address lines and couple the CPU address bus to the secondary address bus. It will connect the main data bus to the refresh bus via the octal bus transceiver U471, and it will blank the display while the CPU has access to the secondary bus.

A memory request to address 370.000A initiates the whole process by bringing pin 9 of the memory decoder, U419, to logic Ø. This logic Ø is coupled to pin 1 of U463 through U465 to lock out the 'B' inputs and connect the CPU address bus to the secondary address bus. The signal on pin 14 of U465 comes from U416A, pin 3 and is logic 1 only during the time the CPU read ($\overline{RD}$) or write ($\overline{WR}$) are asserted. This enables U466A and U466B by placing a logic 1 on pins 1 and 4 so that address line A1Ø at U465, pin 11 can select which 1024 bytes of the 2 K of memory the secondary address bus is to access by its logic state at U466A, pin 2.

The $\overline{WR}$ line (U421, pin 22) will be a logic Ø at U429C, pin 10 during a memory write operation. Since U426C, pin 9, is also a zero, the $\overline{WE}$ lines of U467 through U470 will be asserted. This allows data on the refresh bus to be latched into the memory location that is selected by the secondary address bus. If this had been a read operation, pin 10 of U429C would not have been asserted. As a result, the OR gate would have coupled the logic 1 to the $\overline{WE}$ inputs of the display RAMs. This in turn, would cause the data at the addressed location to be placed on the refresh bus.

The logic Ø on U471, pin 19 (from U419, pin 9) will enable U471, the octal bus transceiver, and allow it to pass data to or from the diaplay RAM. The direction is determined by the logic state on pin 1. Pin 1 of U471 is connected to the $\overline{RD}$ line of the CPU. This line is brought to logic Ø when the CPU wants to read the display RAMs; thus, enabling the buffers and transferring data from the secondary bus to the CPU data bus. U471, pin 1 will be high during a memory write operation, so information on the CPU data bus will be transferred to the secondary bus.

During this time, CRTC row address lines (pins 35 through 38), along with the character generation circuitry, is still active. In order to prevent unwanted information from being printed on the CRT while the CPU is accessing the display RAMs, the logic Ø from U419, pin 9 is used to blank the display. This is done by clearing U476 via pin 1. Schematically, this is at U476C; however, this is a 74LS273 octal D flip-flop (like U472) and so all eight latches will be cleared the instant pin 1 is brought to logic Ø. U476E, pin 12 will thus go to a logic Ø, which will disable the dot video gate, U477D. When the CPU returns control to the CRTC, the data the CPU caused to be placed on the refresh bus will inadvertently be processed by U472, U473, U474, and on out to U477D. In order to give the CRTC time to transfer the data from the Display RAMs to U477D, pin 13, the logic level at U476E, pin 12, will remain zero until all the CPU generated data is done. This delay will last for three character clock periods and is set by D flip-flops U476C, D, and E. When pin 1 of U476 is brought back to logic 1, the Q outputs of these three flops-flops are at a logic Ø. All three are timed by the inverted character clock. The D input of U476C is wired to logic 1 and will be passed to U477C, pin 9, one character clock later. With the CRTC display enable line at pin 10 asserted, the logic 1 will be sent to U476D, pin 8. The second character clock will transfer this enable level to U476E, pin 13, and then to U477D, pin 12, on the third character clock, restoring the display. This blanking action can easily be seen by holding the space bar and Repeat key down on the keyboard while in the reverse video mode.


VIDEO CIRCUIT BOARD
VIDEO AMPLIFIER
+53V SOURCE
+6V SOURCE
POWER SUPPLY
+65V
Q213
Q212
Q211
Q209
Q215
P202-2
P202-3
P202-4
WHT
BLK
VIDEO

VIDEO CIRCUIT BOARD

The Video circuit board has its own power supply and grounding system to keep interference between it and the Terminal Logic board to a minimum. This is a +53 volt power supply and a +6 volt power supply. Both are derived from the +65 volt unregulated supply from the Power Supply board.

When the H19 is first turned on, Q209, Q211, Q212, and Q213 are not conducting. The point labeled '+53 V Source' is at this instant, zero volts. The +65 volts from the Power Supply board is fed through R201, causing base current to flow from Q209. D204 is reverse-biased and therefore, not conducting. As Q209 begins to conduct, current will flow from its collector through R205 and R204. The resulting voltage drop across R204 will forward bias Q211, causing it to conduct. Current enters the collector of Q211 from R206 and the base of Q213, turning Q213 on, which reduces the resistance between the +65 volt supply and the +53 volt line. C202 will quickly charge until the voltage on the anode of D204 becomes more positive than the cathode, causing it to conduct. This places D204, Q213, and R211 in parallel with R201, causing the volage at the junction of R201, R202, and the cathode of D204 to jump towards 53 volts. D203 will prevent the base voltage from rising beyond 12.8 volts (±1%) at the base of Q209. Q209 acts as a differential amplifier with the base as the reference input and the emitter as the error correction input.

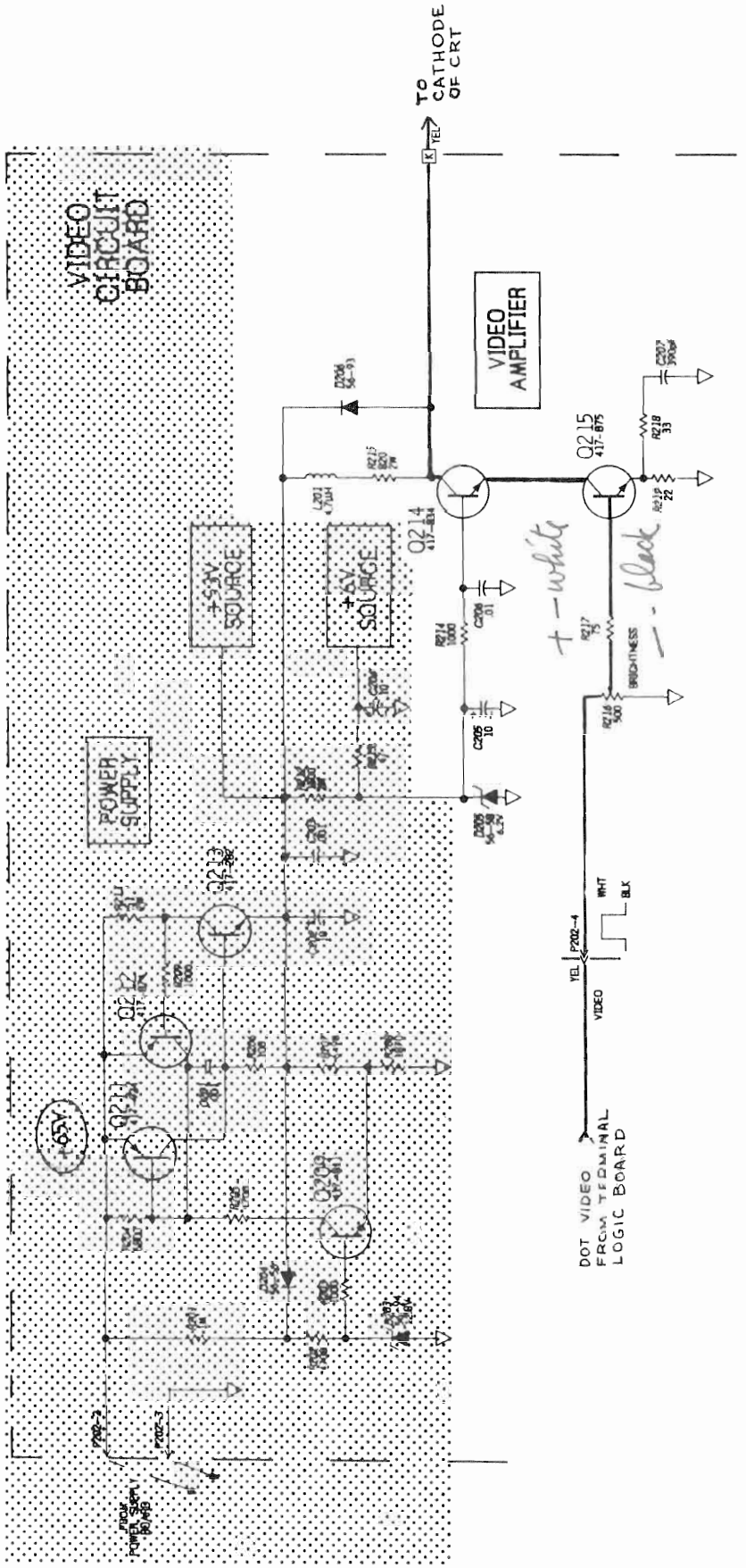
The negative feedback to the emitter is due to the voltage drop across R208 and R207. If the +53 volt supply should become more positive, Q209's emitter voltage becomes more positive , causing the collector current to drop. Q211 will, in turn, conduct less causing Q213 to conduct less. The voltage on the base of Q209 will be multipled by this value to provide the +53 volts at the emitter of Q213. Due to tolerances of R207, R208, and D203, this voltage will stablilize at approximately ±2% of 53 volts.

Q212 provides over-current protection. If the load on the +53 volt line increases such that the current through R211 rises above 1.1 amperes, the voltage drop across this resistor will be enough to turn on Q212. This shunts current past the base-emitter junction of Q211 so that Q211 conducts less. Q213 will also conduct less, so the current through R211 will drop to a safe value.

Even with the negative feedback provided by R207 and R208, the regulator circuit is subject to instability due to its high open-loop gain. C201 causes a high frequency roll-off by coupling the collector of Q211 back to its base, thus providing regulator stability.

R212 and D205 provide a six-volt source for the video amplifier and part of the horizontal circuit. C205, C206, and R214 filter Q214's bias voltage, while R213 and C204 decouple the horizontal circuits.

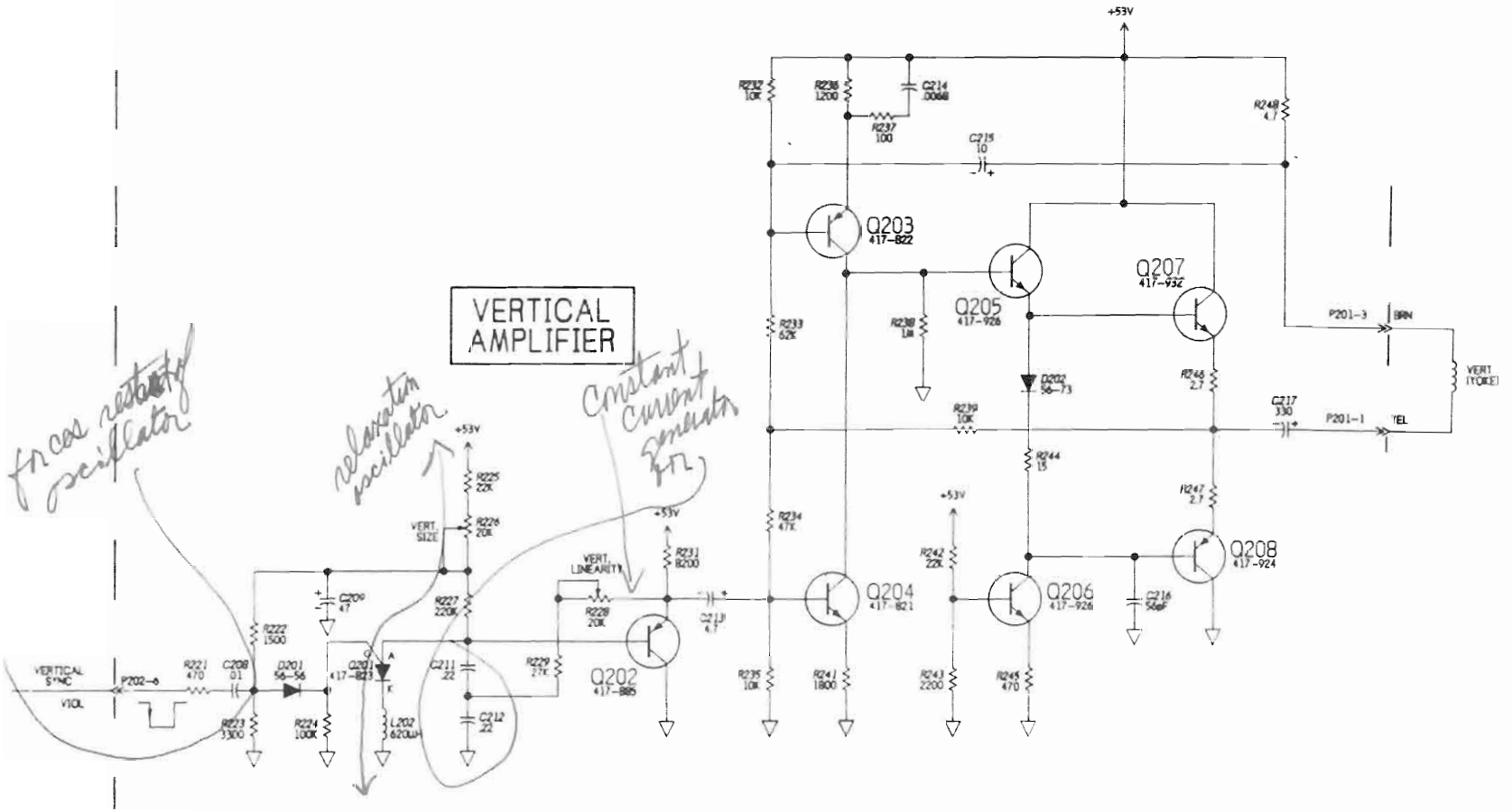
The 22 μF capacitor in parallel with D203 will slow down the time it takes for the power supply to reach full operating voltage. This is necessary because the +53 volt power supply will reach full operating voltage (in some units) before the CPU has had time to finish programming the CRTC for the proper sweep frequencies. In such a case, there will be heard a 'crackling' sound, similiar to a high voltage arc, at the instant of turn-on.


VIDEO CIRCUIT BOARD
TO CATHODE OF CRT
YEL
VIDEO AMPLIFIER
Q215
417-875
Q214
417-834
+93V SOURCE
+6V SOURCE
POWER SUPPLY
Q213
Q212
Q211
Q209
+65V
BRIGHTNESS
+ - white
- - black
WHT
BLK
P202-4
VIDEO
DOT VIDEO FROM TERMINAL LOGIC BOARD
P202-3
P202-2

VIDEO AMPLIFIER

The Video amplifier is a cascode amplifier consisting of Q214 and Q215. This circuit is characterized by its high gain, low noise, and low input and output capacitances. The video and dot information from the Terminal Logic board enters the Video board at P204, pin 4, and is applied across R216, the Brightness Level control. A positive voltage at this point is white information. The brightness of the display is determined by how much of this voltage is coupled from R216 to the base of Q215. R219 sets the overall amplifier gain.

R218 and C207 provide high frequency compensation by shaping up the rise and fall times of the dot video pulse. The greatest number of high frequency harmonics occur at the rise and fall times of the video pulse. At this time, the capacitive reactance of C207 will drop towards zero, placing R218 in parallel with R219 and increasing the amplifier gain. Peaking coil L201 also provides high frequency compensation by increasings its X_L for the leading and trailing edges. R215 provides resistive loading for the collector of Q214, while D206 prevents ringing by L201. The white level of the dot video signal on Q214's collector will be approximately +20 volts and the black level approximately +50 volts. This signal is fed through R1 to the cathode of the CRT.


VERTICAL AMPLIFIER
forces restoring oscillator
relaxation oscillator
Constant current generator
+53V
VERT. SIZE
VERT. LINEARITY
VERTICAL SYNC
VIOL
P202-6
R221 470
C208 .01
D201 56-56
R222 1500
R223 3300
R224 100K
C209 47
Q201 417-823
L202 620uH
R225 22K
R226 20K
R227 220K
C211 22
C212 22
R229 27K
R228 20K
Q202 417-885
R231 8200
C213 4.7
R232 10K
R236 1200
C214 .0068
R237 100
C215 10
R248 4.7
Q203 417-822
Q205 417-926
Q207 417-932
R233 62K
R238 1M
D202 56-73
R246 2.7
R239 10K
C217 330
P201-3
BRN
P201-1
YEL
VERT (YOKE)
R244 15
R247 2.7
R234 47K
R242 22K
Q204 417-821
Q206 417-926
Q208 417-924
C216 56pF
R235 10K
R241 1800
R243 2200
R245 470

VERTICAL CIRCUITS

The vertical sync pulse enters the Video board at P202, pin 6, and is coupled to the anode of D201 through R221 and C208. D201 is part of a relaxation oscillator circuit whose main component is the Programmable Unijunction Transistor (PUT), Q201. Like a neon lamp, the PUT will start conducting when its anode voltage reaches a certain level, and continue to conduct after the anode voltage drops below the firing voltage. After a certain minimum voltage is reached, the PUT will cut off. The programmability of the PUT is due to the gate input. The voltage on the gate will set the voltage at which the PUT will start conducting. For Q201, this is determined by the voltage divider R222 and R223, less the forward voltage drop across D201. Ignoring the vertical sync pulse for a moment, Q201 will conduct when its anode voltage rises approximately .6 volts above the gate voltage. The rate of this rise time is determined by the time constant of C212, C211, and R227. When Q201 conducts, current flows through Q201 and L202. The anode voltage will drop towards zero and discharge these two capacitors. Q201 will stop conducting and C211 and C212 will start charging again. The length of the sweep (and therefore the vertical height) is determined by the setting of R226.

Normally, Q201 will oscillate slightly lower than 60 Hz. When the vertical sync pulse occurs, the negative edge of the pulse will drop quickly towards zero. The instant the gate voltage drops below the anode voltage, Q201 will conduct somewhat sooner than if no sync pulse had been present.

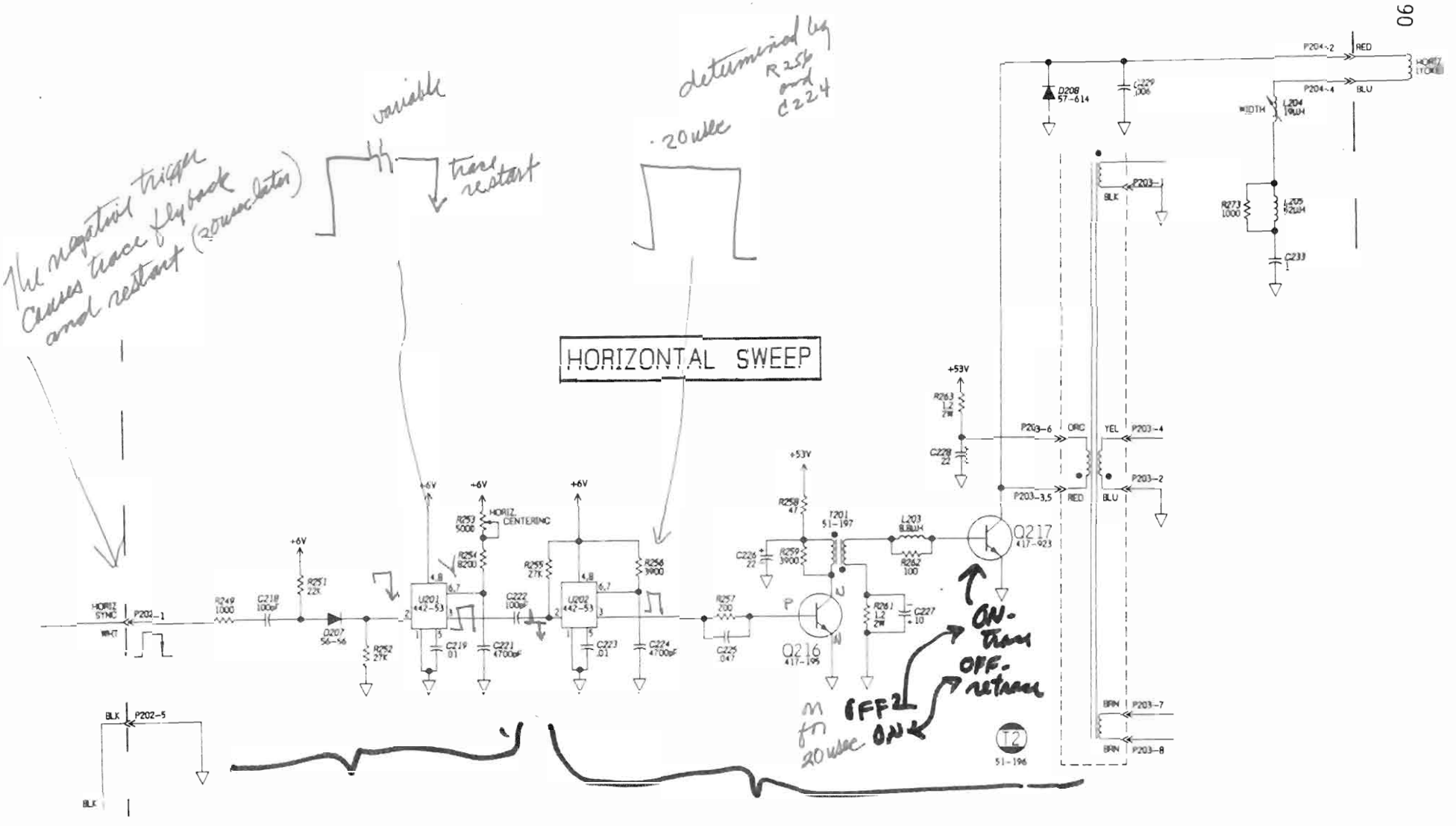
A constant current source must be applied to C211 and C212 to overcome the capacitors' characteristic of charging at an exponential rate. The Darlington transistor, Q202, provides a source of constant charging current to C212 so the voltage increase on C212 and C211 will be linear. Q202 has near unity gain, thus the voltage emitter will follow the base signal. When C211 and C212 begin to charge, the voltage at the junction of R228 and R231 will increase at the same rate. This maintains a constant voltage drop across R228, R229, and C211. Since R228 and R229 have a lower resistance than R227, the current through these resistors will have a major effect on the rate of charge of C212 and C211. Because the voltage drop across R229 and R228 is constant, the current through these resistors, and therefore the capacitors, will be constant.

From a practical standpoint, the voltage ramp will actually be slightly concave. This is because R228 is adjusted for a linear vertical display and must compensate for the CRT curvature.

The quiescent levels of the vertical amplifier are set up by resistors R232, R233, R234, R235, and emitter resistors R236 and R241. Approximately 2 mA of current flows through Q204 and 3 mA through Q203. The remaining one milliampere comes from the base of Q204 and through R238 (about 30 micro-amperes). Q206 is a constant current source and supplies

bias current to Q208's base and to the bias network D202 and R244. The stabistor (D202) insures bias stability over a wide ambient temperature range. The voltage on the anode of D202 will bias Q207 into a slightly conducting state to eliminate crossover distortion of the ramp voltage. The junction of R246 and R247 will be about 25 volts, which, when fed back to the input through R239, will maintain this quiescent level.

The ramp at Q202's emitter is coupled to the base of Q204 through C213, where it is inverted and applied to the base of Q205. At this point, the signal is about thirty volts peak-to-peak. Q205 acts as a predriver to the power amplifier, Q207 and Q208, which supply sufficient current to the deflection yoke. C216 provides high frequency roll-off to add to the amplifier stability. The sweep signal is connected to the vertical deflection yoke through C217 where the resultant magnetic field will deflect the beam. To maintain linearity, the yoke current is converted back to a ramp voltage when it flows through R248. This signal is used as a correction signal by negatively feeding it back to the base of Q203. Q203's collector current will change according to the amount of correction needed. C214 and R237 provide high frequency compensation.


The negative trigger causes trace flyback and restart (20usec later)
variable
trace restart
determined by R256 and C224
20usec
HORIZONTAL SWEEP
HORIZ SYNC
WHT
P202-1
BLK
P202-5
R249 1000
C218 100pF
R251 22K
D207 56-56
R252 27K
+6V
U201 442-53
U202 442-53
R253 5000
HORIZ. CENTERING
R254 8200
C219 .01
C221 4700pF
C222 100pF
R255 27K
R256 3900
C223 .01
C224 4700pF
R257 200
C225 .047
+53V
R258 47
C226 22
R259 3900
T201 51-197
Q216 417-195
R261 1.2 2W
C227 10
L203 8.8uH
R262 100
Q217 417-923
R263 1.2 2W
C228 22
P203-6
ORG
YEL
P203-4
P203-3,5
RED
BLU
P203-2
BRN
P203-7
P203-8
D208 57-614
C229 .006
P204-2
RED
HORIZ (TOP)
P204-4
BLU
WIDTH
L204 19uH
R273 1000
L205 52uH
C233 1
T2 51-196
ON-trace
OFF-retrace
OFF 2
ON
on for 20usec

HORIZONTAL CIRCUITS

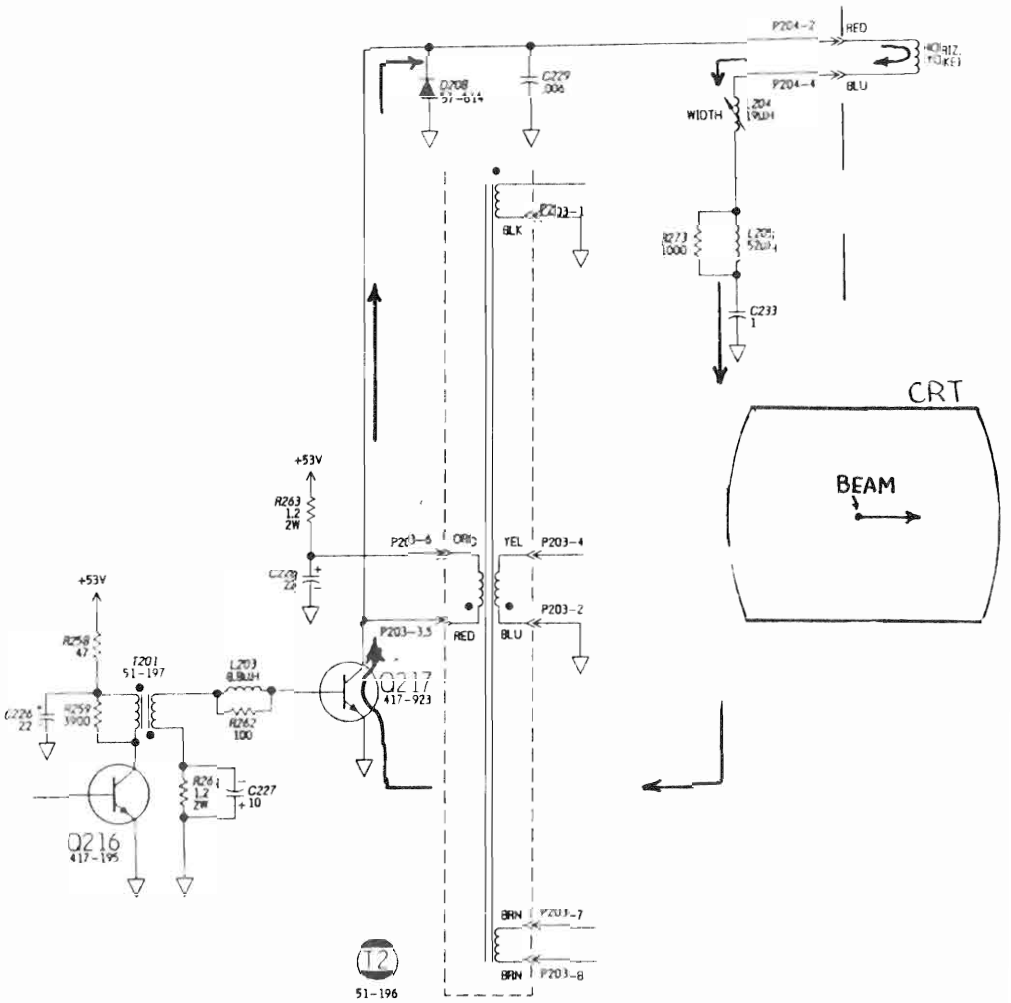
Rather than synchronize a free-running oscillator, the horizontal sync pulse directly drives the sweep amplifier after being retimed and reshaped. The pulse enters the Video board at P202, pin 1, and is coupled to the anode of D207 through R249 and C218. The negative-going edge of the pulse is coupled to pin 2 of the 555 timer (wired as a monostable multivibrator), U201, causing pin 3 to be triggered high. The retrace won't start until U201, pin 3 returns to zero volts. The length of time pin 3 remains high is determined by C221, R254, and R253. By varying the horizontal centering control (R253), the time before the sweep start can be varied, with respect to the video information, so that the position of the display is effected.

To improve stability and prevent false triggering in U201 and U202, the control lines (pin 5) are decoupled by C219 and C223 and the reset lines (pin 4) are tied to +6 volts.

The retrace will start when the falling edge of the signal at U201, pin 3, triggers U202, pin 2 through C222. Pin 3 will go high for about 20 μs (determined by R256 and C224) and turn on Q216 through R257 and C225.

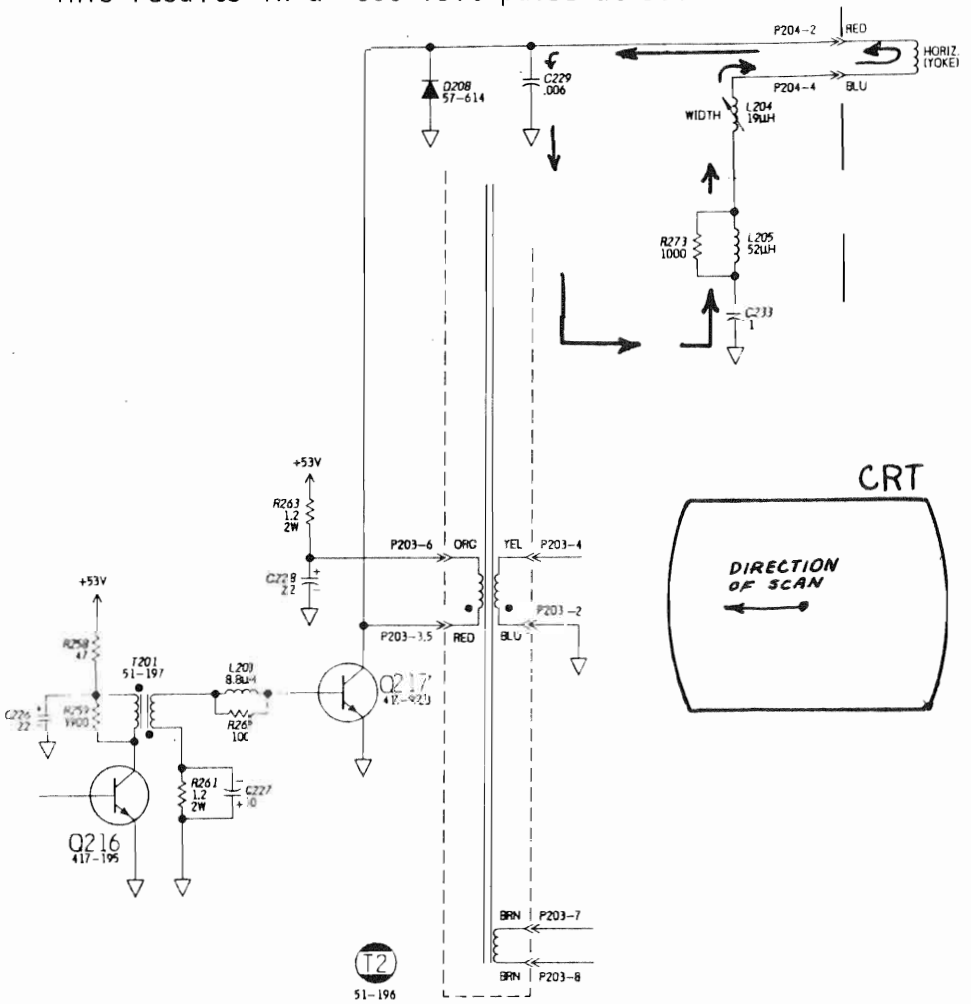
The resulting current flowing through T201's primary causes the secondary to generate a negative voltage at the base of Q217, reverse-biasing it. When the pulse at Q216's base returns to zero, Q216 will turn off and T201's secondary current will reverse and turn on Q217. The combined values of L203, R262, R261, C227, and the inductance of T201 will determine how long Q217 will conduct.

The action of Q217 switching on and off is the source of both the horizontal sweep and the CRT voltages. The sweep will be considered first.



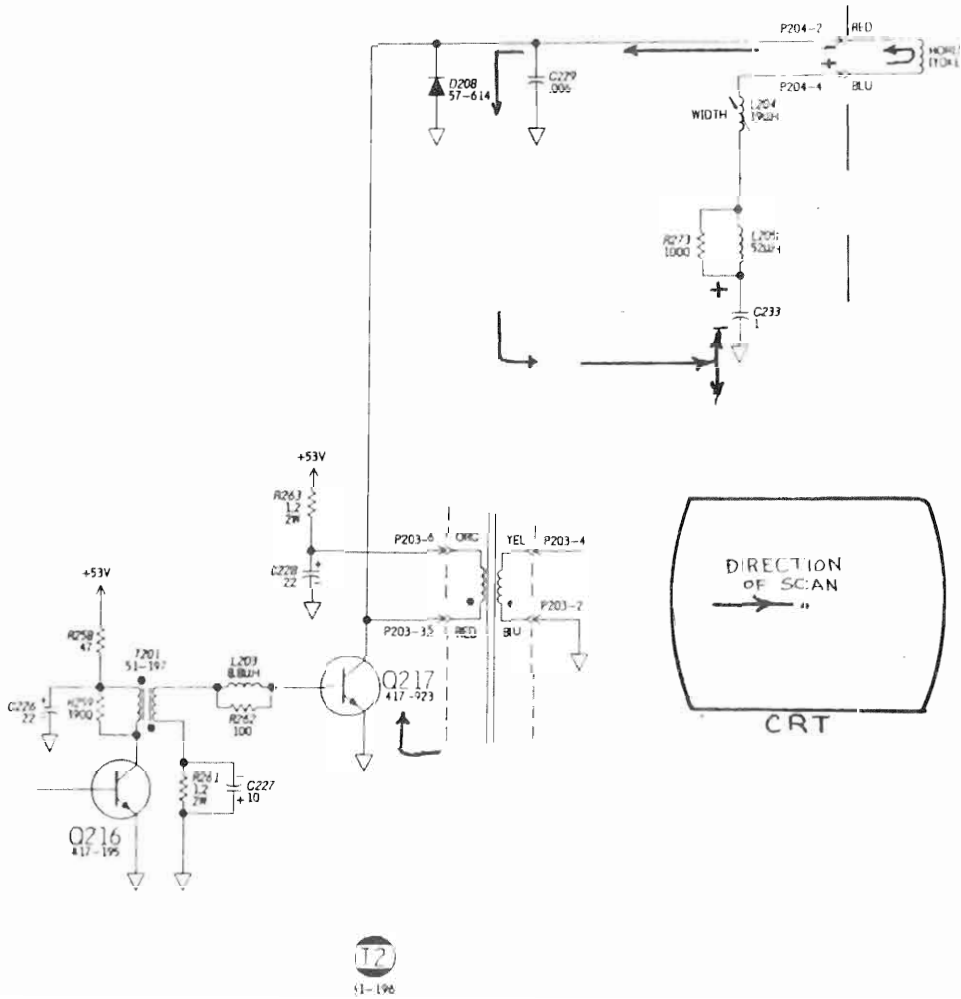
Assume the circuit has been in operation for several cycles the electron beam is at the center of the CRT, and Q217 has been turned on. Electrons will flow through Q217, T2's primary and to the +53 volt power supply. At this time, there is a charge on C233 so that its high end is positive with respect to ground. Electrons will leave the grounded side of C233, flow through Q217, through the horizontal yoke, L204, L205/R273, and to C233. The increasing yoke current causes the electron beam to deflect to the right (from the center of the CRT). At the right edge, Q216 will turn on and Q217 will cease conducting. The energy built up in the yoke and T2's primary will transfer to C229. When Q217 was conducting, P203, pin 3, was negative with repect to P203, pin 6, the counterelectromotive force generated by T2 now reverses

polarity to maintain current flow in the same direction. This pulls current up through C229, charging it positive with respect to ground. In the same manner, P204, pin 2, which was negative with respect to P204, pin 4, has also reversed polarity and is aiding current flow through C229. This results in a +550 volt pulse at D208's cathode.



At this time, C233 is nearly discharged and the yoke current is nearly zero (after the magnetic field has collapsed). The electron beam begins to "fly back" toward the center of the CRT. Then C229 begins to discharge, causing current to flow up through C233, L205/R273, L204, the yoke, and into the ungrounded side of C229. C233 begins to charge. The electron beam will start to deflect toward the left side of the CRT from the center.

C229 reaches zero volts and the energy in the yoke is maximum. CEMF causes the yoke polarity to reverse, P204; pin 2, becomes negative with respect to P204, pin 4. Current flows from P204, pin 2, through D208, up through C233 (further charging it), R273/L205, L204, and to the yoke. At this time, the yoke current is decreasing and the electron beam is scanning from the left side of the CRT towards the center. Just before it reaches center, Q216 turns off. At this time, C233 is almost fully charged and the yoke current is almost zero. Q217 turns on and C233 attempts to discharge through Q217 by pushing current into the emitter. At the same time,

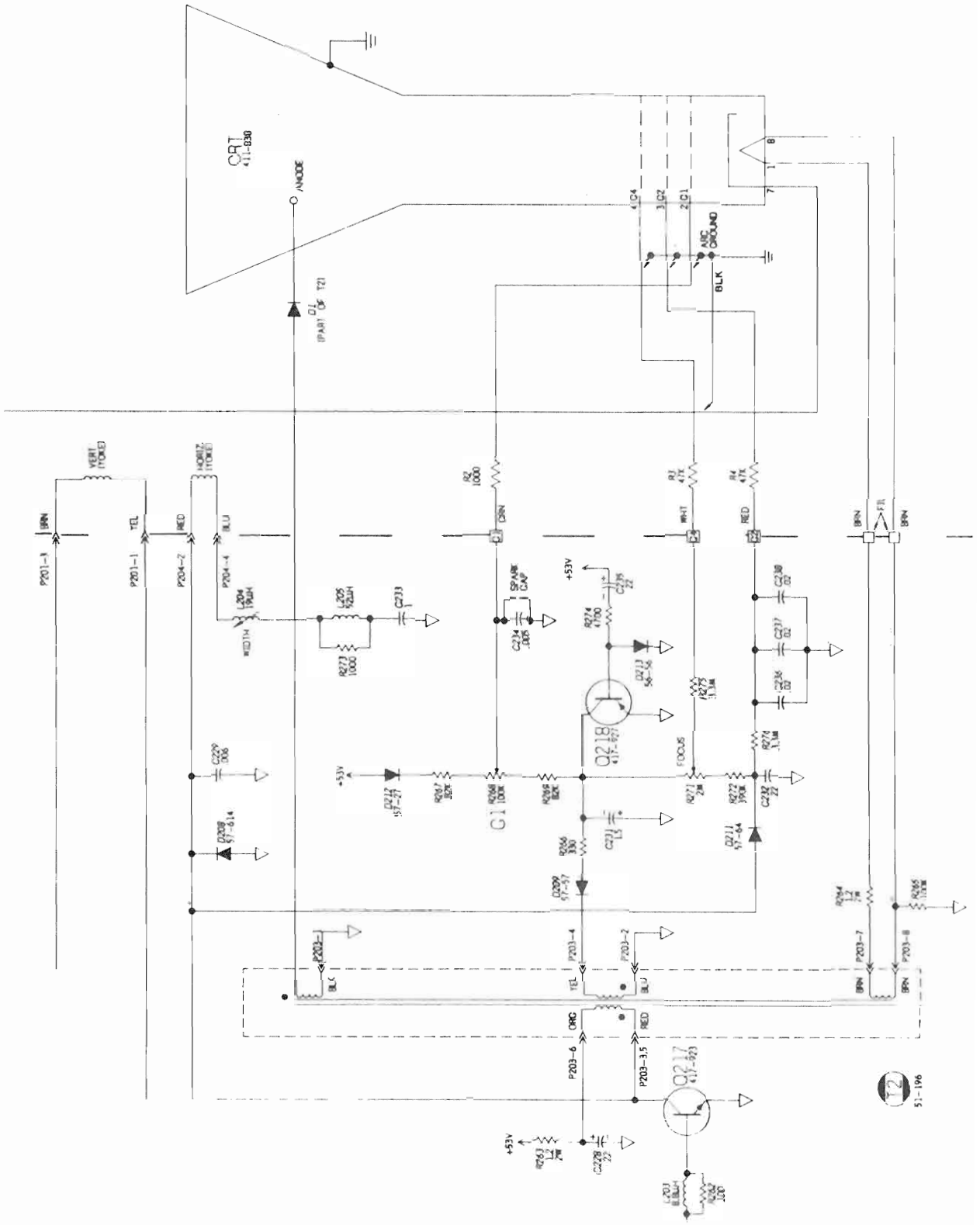


the remaining collapsing yoke electromagnetic field will continue to push current into the cathode of D208. These two effects cancel, so that the change of direction of current flow (now from P204, pin 2, to P204, pin 4) will be smooth, thus eliminating any crossover distortion in the center of the display.

At this point the cycle repeats.

Due to the curvature of the CRT faceplate, the electron beam striking the phosphor near the right and left edges will travel a greater distance for a given rate of change of yoke current than at the center of the CRT. To compensate for this, the current rate of change must be decreased (slowed down) slightly when at the edges. The values of C233, R273, and Horizontal linearity coil L205 are selected to do this by introducing an "S" shaped curve into the current waveform.

The amount of current through the yoke circuitry can be changed by adjusting L204. This will change the reactance of L204, which will control the scan width.


CRT
411-030
ANODE
D1
(PART OF T2)
ARC GROUND
BLK
VERT (YOKE)
HORIZ (YOKE)
BRN
YEL
RED
BLU
P201-3
P201-1
P204-2
P204-4
WIDTH
L204 19uH
L205 52uH
C233 1
R273 1000
R2 1000
CRN
SPARK CAP
C234 .005
+53V
C235 22
R274 4700
D213 56-56
Q218
417-927
R3 47K
WHT
R4 47K
R275 3.3M
FOCUS
R271 2M
R272 390K
C232 22
C238 .02
C237 .02
C236 .02
R276 3.3M
C229 .006
D208 57-614
D212 57-27
R267 82K
R268 100K
R269 82K
G1
C231 1.5
R266 330
D209 57-57
D211 57-64
R264 1.2 2W
R265 100K
P203-1
P203-4
P203-2
P203-7
P203-8
ORG
P203-6
P203-3,5
Q217
417-923
R263 1.2 2W
C228 22
L203 8.8uH
R262 100
T2
51-196

CRT POWER SUPPLIES

The +550 volt pulse that occurs when Q217 turns off is also rectified by D211 and filtered by C232, R276, C236, C237, and C238. This is applied to the "G2" grid of the CRT through R4. A secondary winding on T2 connects the flyback pulse to D209, R266, and C231. These components will rectify and filter a negative 110 volts source that is used by the focus and control grid bias circuits.

The focus circuitry is made up of R272 and control R271. The supplied voltage tapped off of R271 is applied to the "G4" grid of the CRT through R275 and R3.

R269, R268, R267, and D212 make up a divider network for the control grid voltage. Control G1 (R268) sets the display black level. This is applied to pin 2 of the CRT through R2.

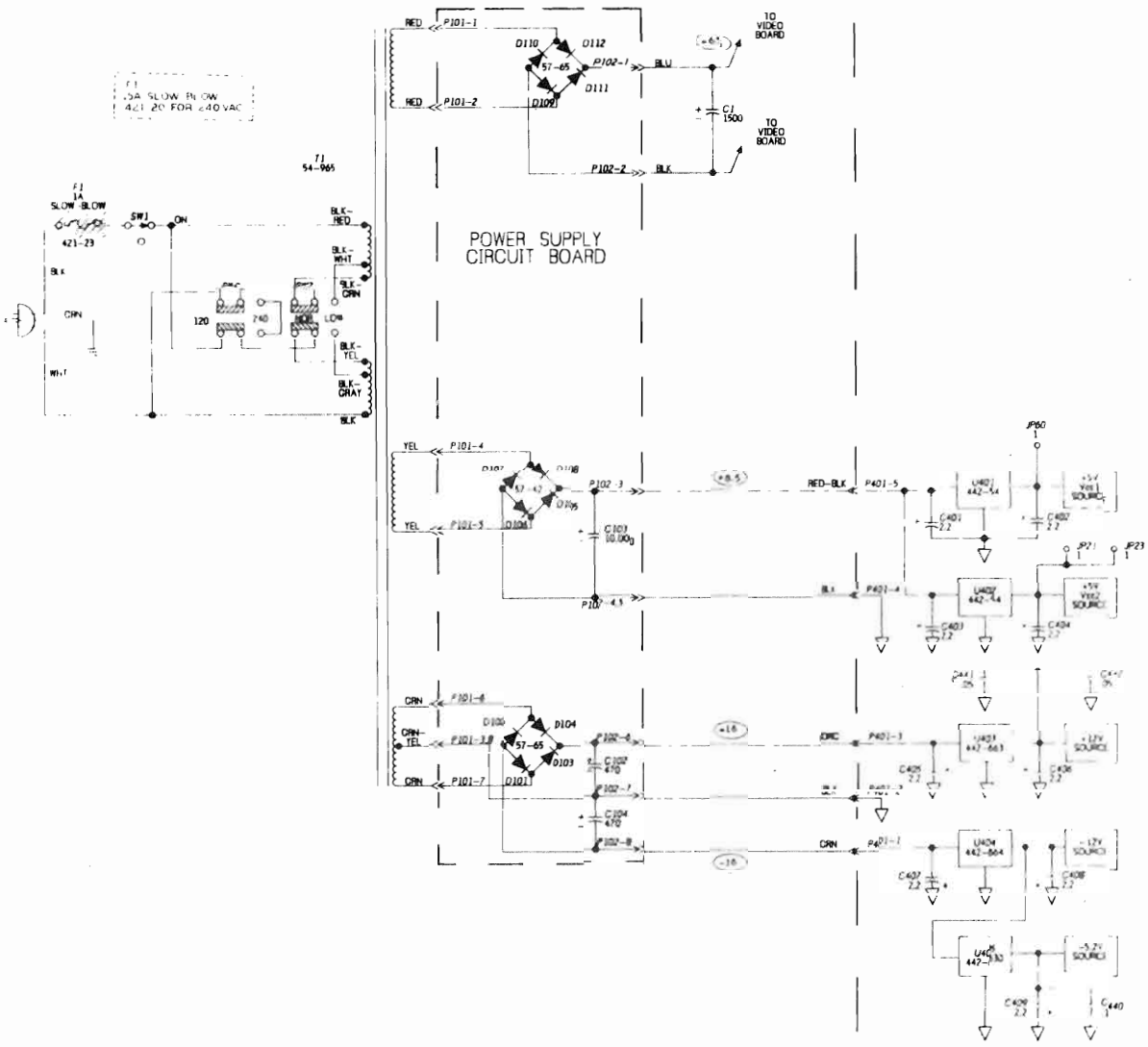
The CRT acceleration voltage consists of D1 (part of the flyback transformer) and the high voltage secondary. The cathode of D1 will measure about 15 kV.

A filament winding on T2 will tap 6.3 VAC from the flyback pulse and feed it through R264 to the CRT heater. R265 prevents possible breakdown by referencing the filament to ground.

R1 through R4, in line with the CRT leads, and a spark-gap circuit inside the socket will prevent damage to the video circuits due to an occasional arc over. The resistors provide current limiting.

Q218 provides CRT phosphor protection. Without it, a bright dot might appear in the CRT after turn-off, burning the phosphor. When the Terminal is first turned on, current will flow up through D213 and R274 to charge C235. Q218 will then remain inactive until power is removed from the H19. On turn off, several things will happen. The +53 volts supply will drop toward zero, causing C235 to discharge through R274 and the base-emitter of Q218. Q218 will then saturate and instantly short the -100 volt supply to ground. The control grid will become more positive with respect to the cathode, causing an increase in CRT current. The horizontal circuits will be inactive, but the +53 volts will keep the vertical circuits working a few milliseconds longer, causing a bright vertical line as the CRT current discharges the remaining high voltage stored in the CRT.

LOW VOLTAGE SUPPLIES



Power to the H19 Terminal can be either 120 VAC, 50-60 Hz, or 240 VAC, 50-60 Hz. SW2 will place the primaries of T1 in parallel for 120 VAC and in series for 240 VAC. SW3 will tap the primaries at a lower winding to boost the secondary voltages when placed in the "low" position.

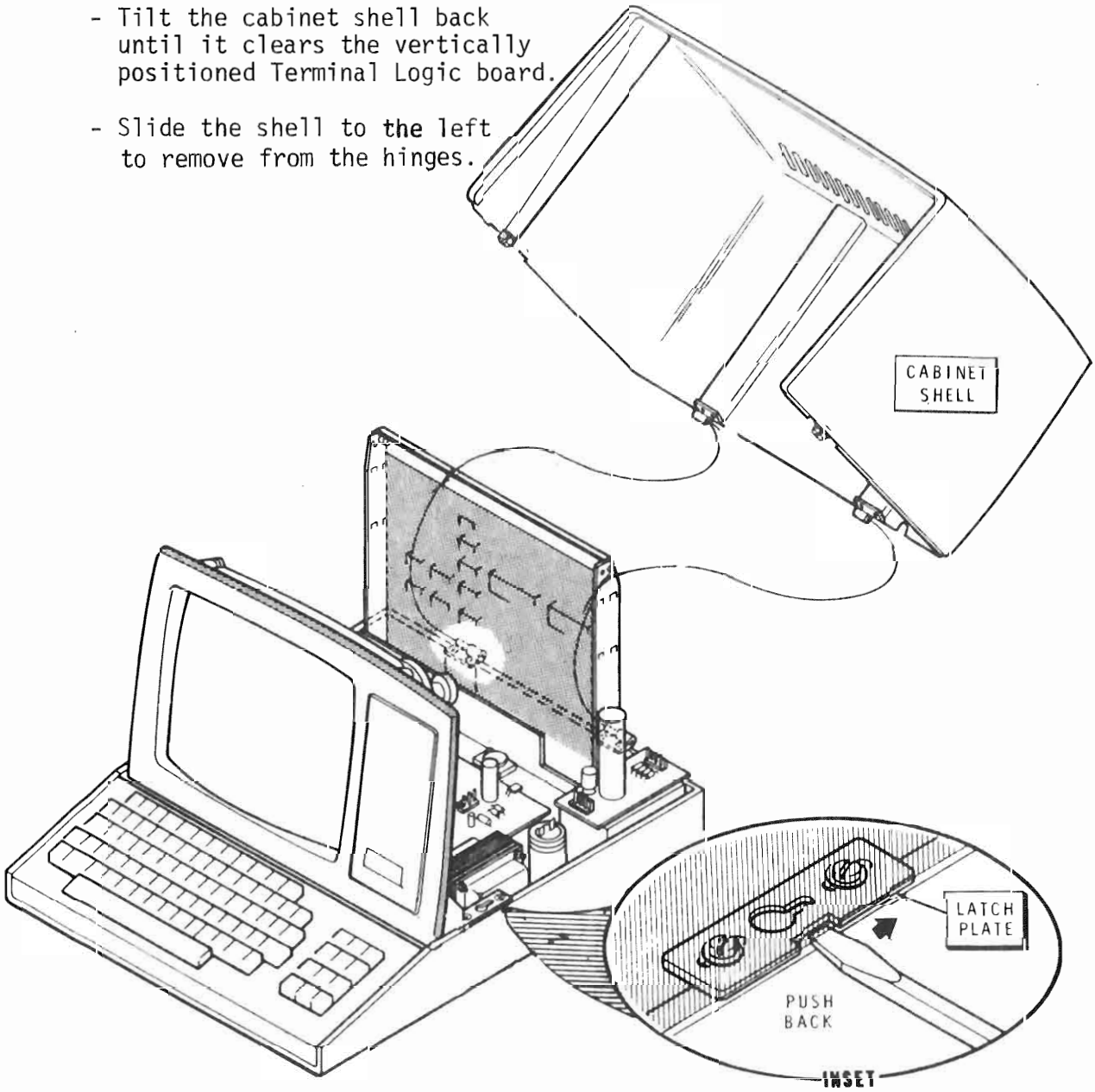
There are three secondary supplies. Bridge circuit D109 through D112 and C1 will provide rectification and filtering of the +65 volts to the Video board. The ground return for this supply is kept separate from the terminal logic grounds to keep interference between these two boards to a minimum. The +8.5 volt supply is rectified and filtered by the bridge network D105 through D108 and C103. This voltage is sent to the two +5 volt regulators U401 and U402. C401 and C403 at the inputs shunt to ground any noise induced in the wires between the Power Supply board and the Terminal Logic board. C402 and C404 improve the output transient response. The +16 volts and the -16 volts supplies are generated by two full-wave rectifiers (D101/D102 and D103/D104 respectively) sharing the same secondary. The +16 volt supply is filtered by C102 and conrected to U403 to provide the +12 volt supply. The -16 volts is filtered by C104 and regulated to -12 volts by U404. C405 and C407 improve regulator stability by filtering any noise picked up on the +16 volt lines and C406 and C408 insure correct transient response of the regulators. U405 will use the -12 volt source to provide the regulated -5 volt source.

All of the regulators are internally protected from damage by exterral short circuiting and excessive heating.

DISASSEMBLY

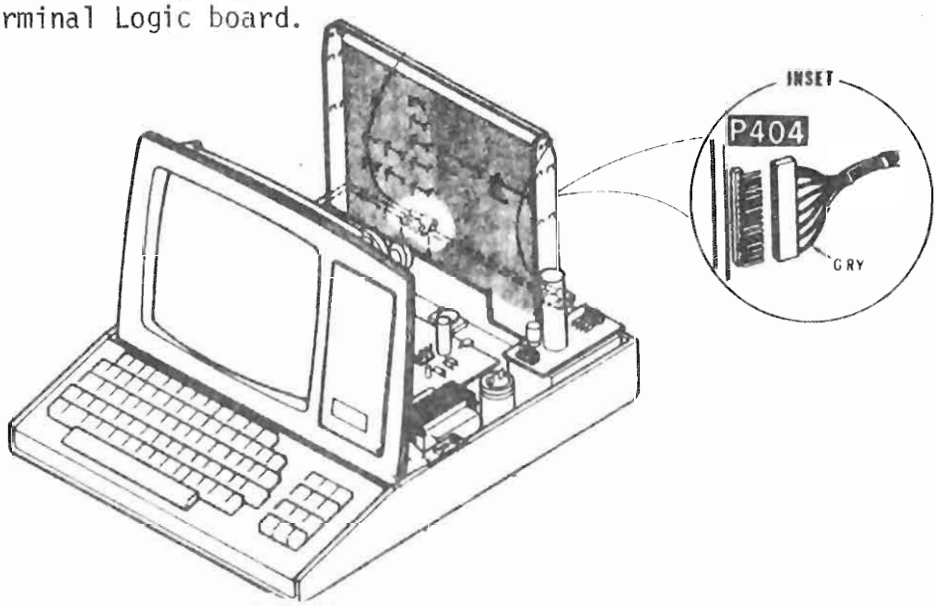
CABINET SHELL REMOVAL

- With a flat blade screwdriver, slide the latch plate toward the rear of the unit. Refer to the inset on the pictorial.
- Tilt the cabinet shell back until it clears the vertically positioned Terminal Logic board.
- Slide the shell to the left to remove from the hinges.

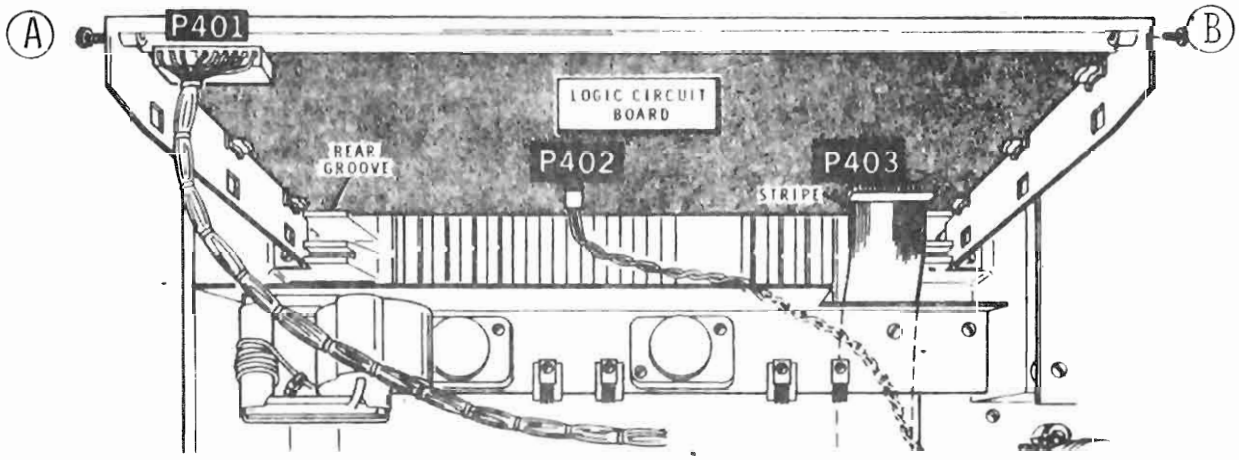


TERMINAL LOGIC BOARD REMOVAL

- Unplug P404 on the rear of the Terminal Logic board.



- Unplug P401, P402, and P403 on the front of the board.

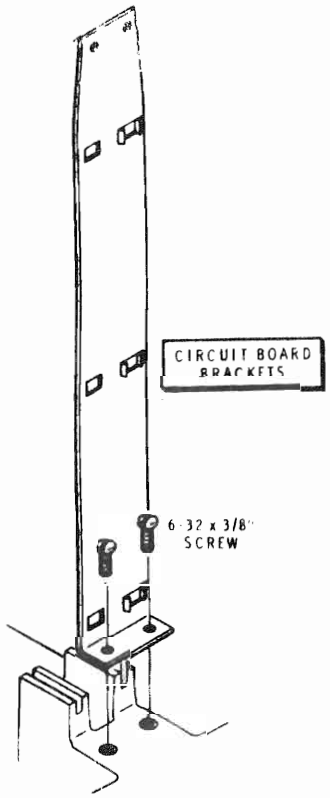


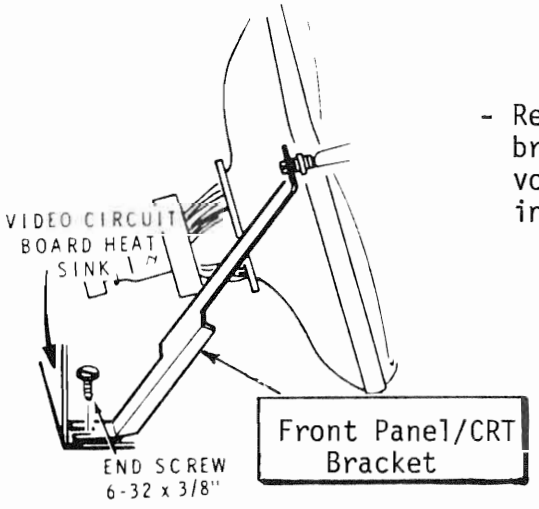
- Remove the screws at A and B holding the top of the Terminal Logic circuit board to the top of the circuit board brackets.

- Slide the Terminal Logic board upward to remove.

VIDEO AMPLIFIER CIRCUIT BOARD REMOVAL

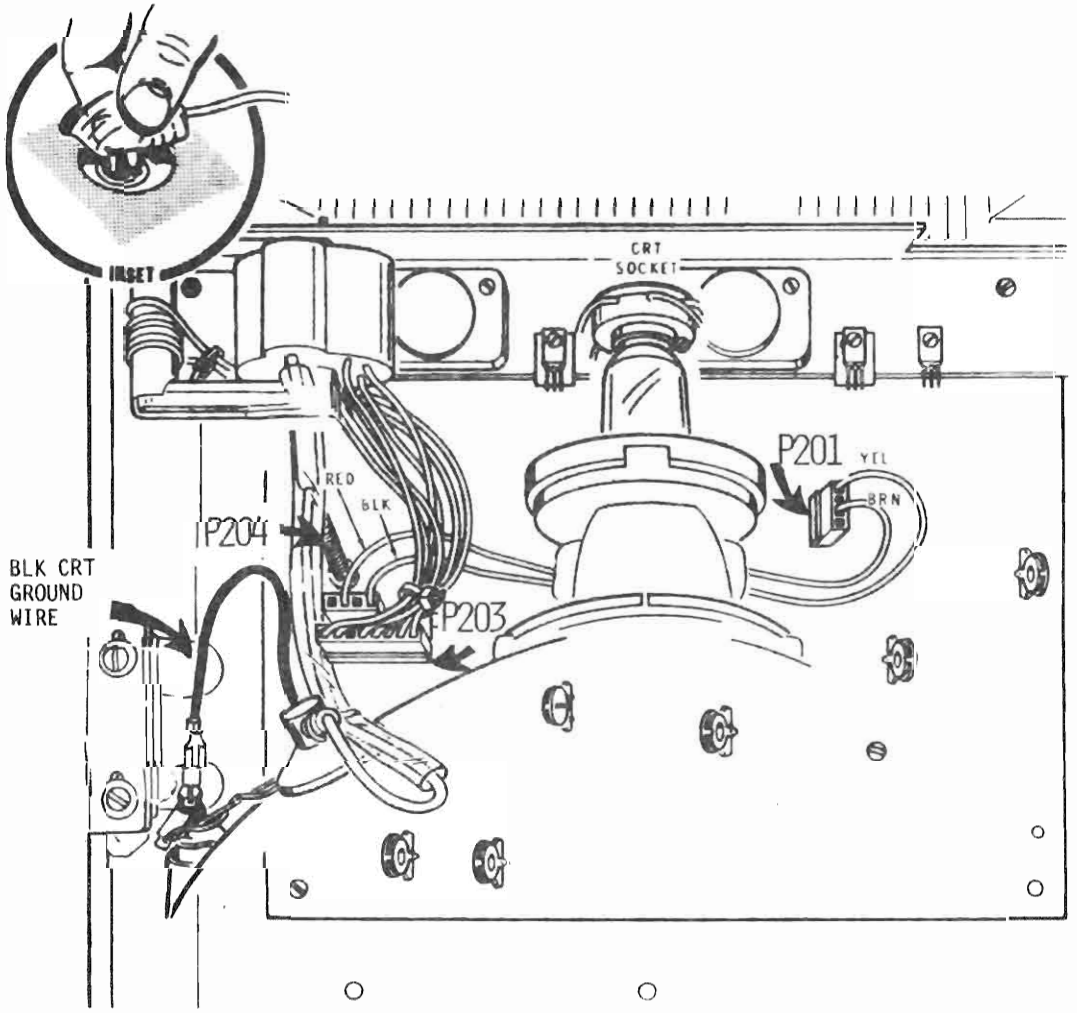
- Remove the two circuit board brackets.





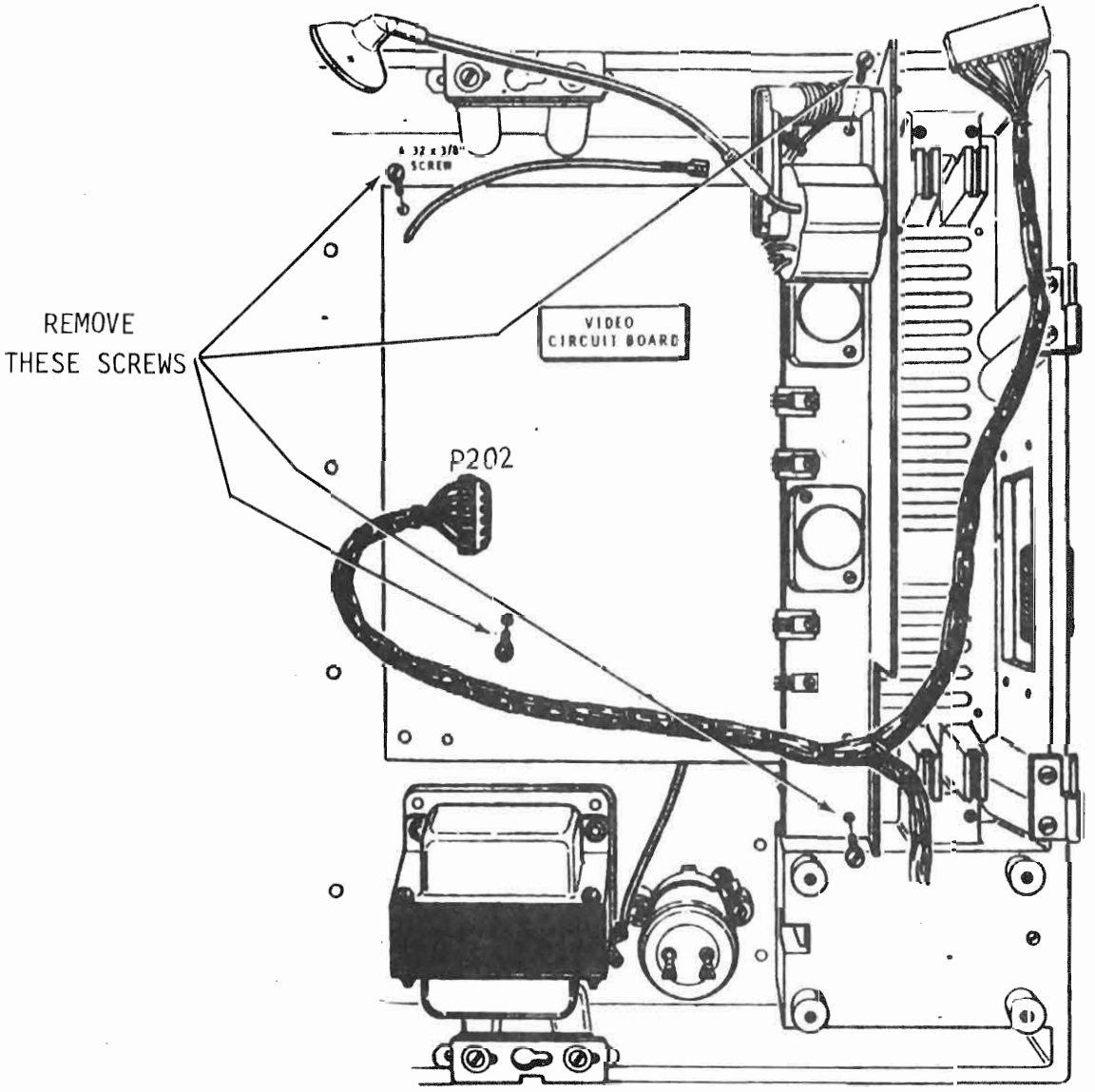
- Remove the front panel/CRT bracket next to the high voltage power supply (shown in the pictorial at the left).

- Discharge the CRT anode and remove the anode connector from the CRT. (Refer to the inset in the pictorial below.)



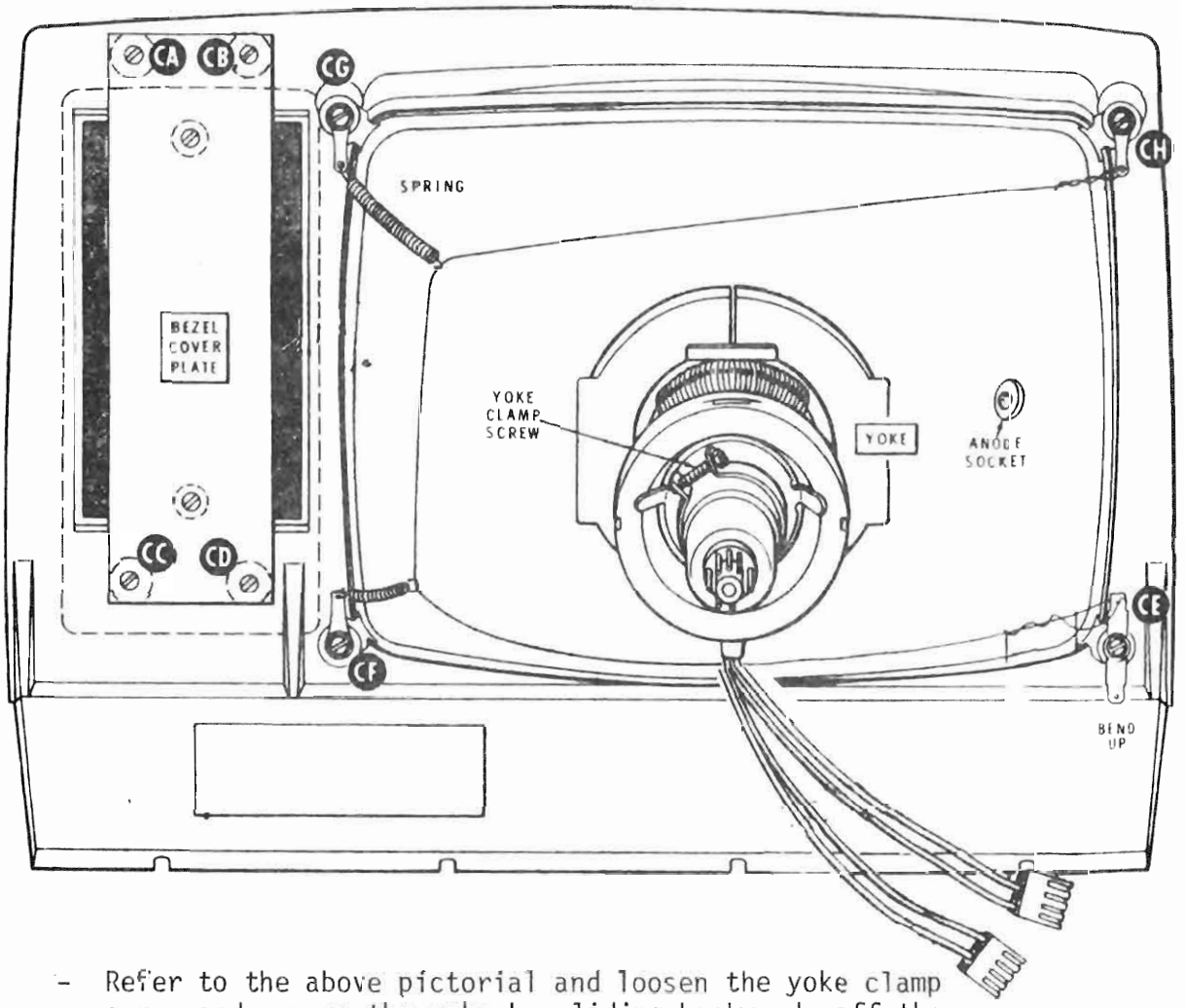
- Remove the black CRT ground wire.
- Unplug P201, P203, and P204.

- Refer to the pictorial below and unplug P202.



- Remove the four 6-32 x 3/8" screws (shown in the above pictorial).
- Slide the board toward the rear of the unit to remove.

CRT REMOVAL



- Refer to the above pictorial and loosen the yoke clamp screw and remove the yoke by sliding backwards off the neck of the CRT.

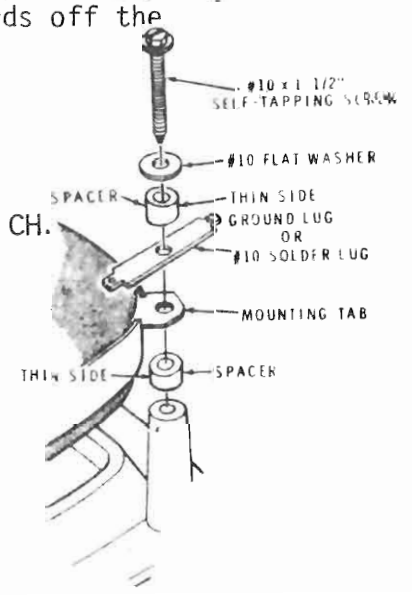
- Disconnect the *springs* at CG and CF.

To remove the ground wire:

- Remove the #10 x 1.5" self-tapping screw at CH.

- Remove the mounting hardware at CE. (Refer to the detail drawing at the right.)

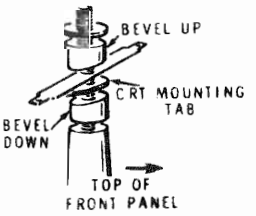
  The ground wire can now be removed and set aside.



- Remove the hardware at CF and, bracing the bell of the CRT with one hand, remove the hardware from CG.

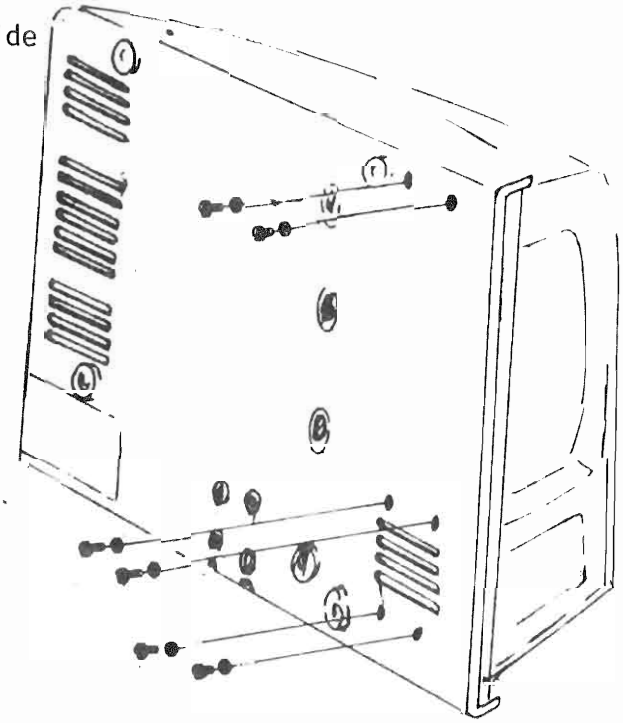
- Carefully lift out the CRT.

Using care and assistance, the CRT can be reinstalled in the opposite order listed above. Or, the front panel can be removed and then the CRT reinstalled with the front panel laying face down. Be sure to align the the beveled portions of the spacers as shown in the pictorial at the right.

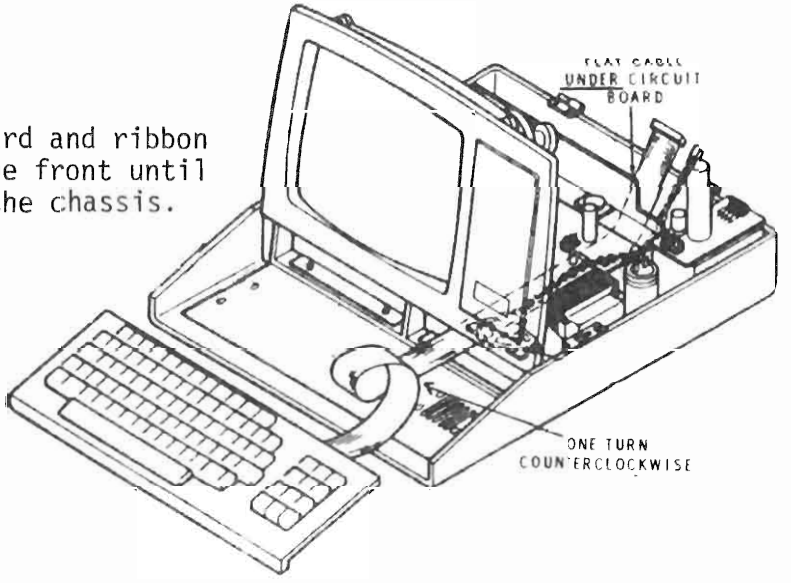


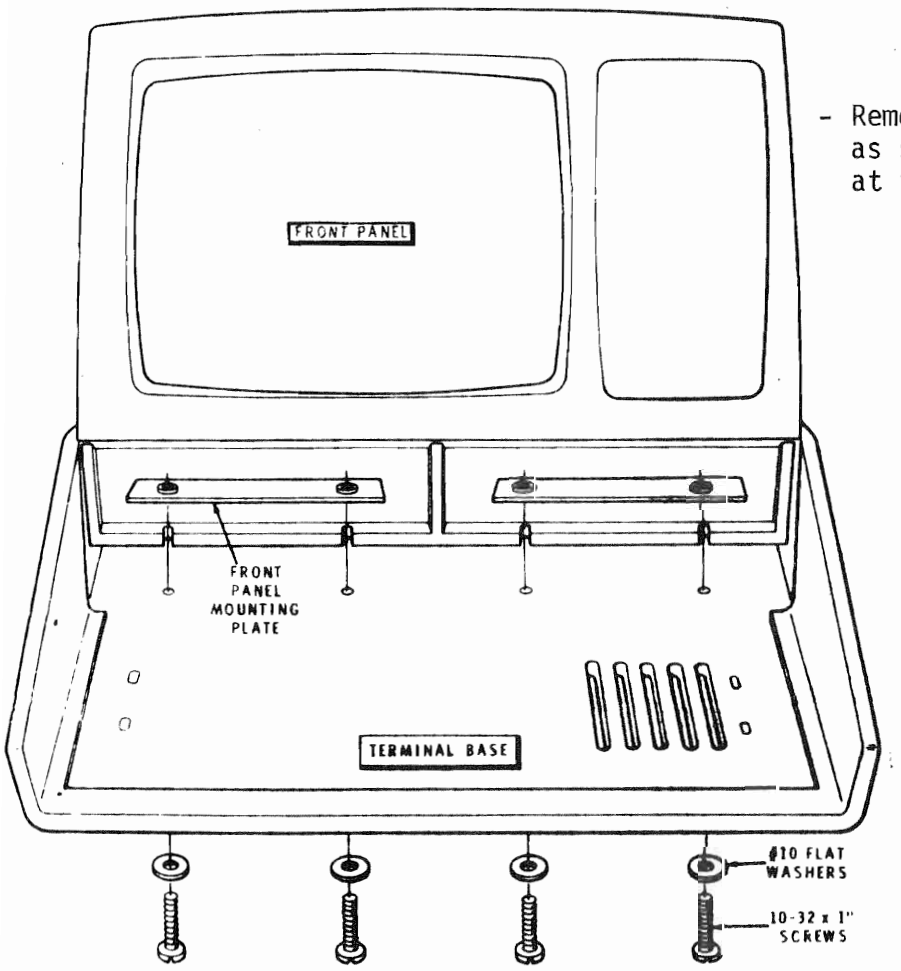
KEYBOARD AND FRONT PANEL REMOVAL

- Set the chassis on its side and remove the indicated 8-32 x 1/2" screws.



- Pull the keyboard and ribbon cable toward the front until it is free of the chassis.

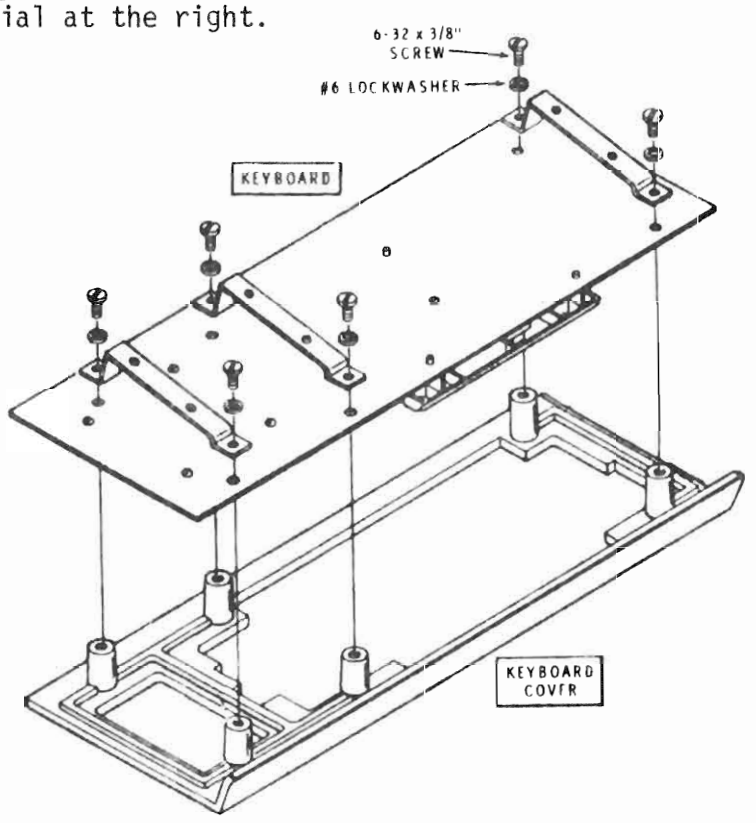




- Remove the front panel as shown in the pictorial at the left.

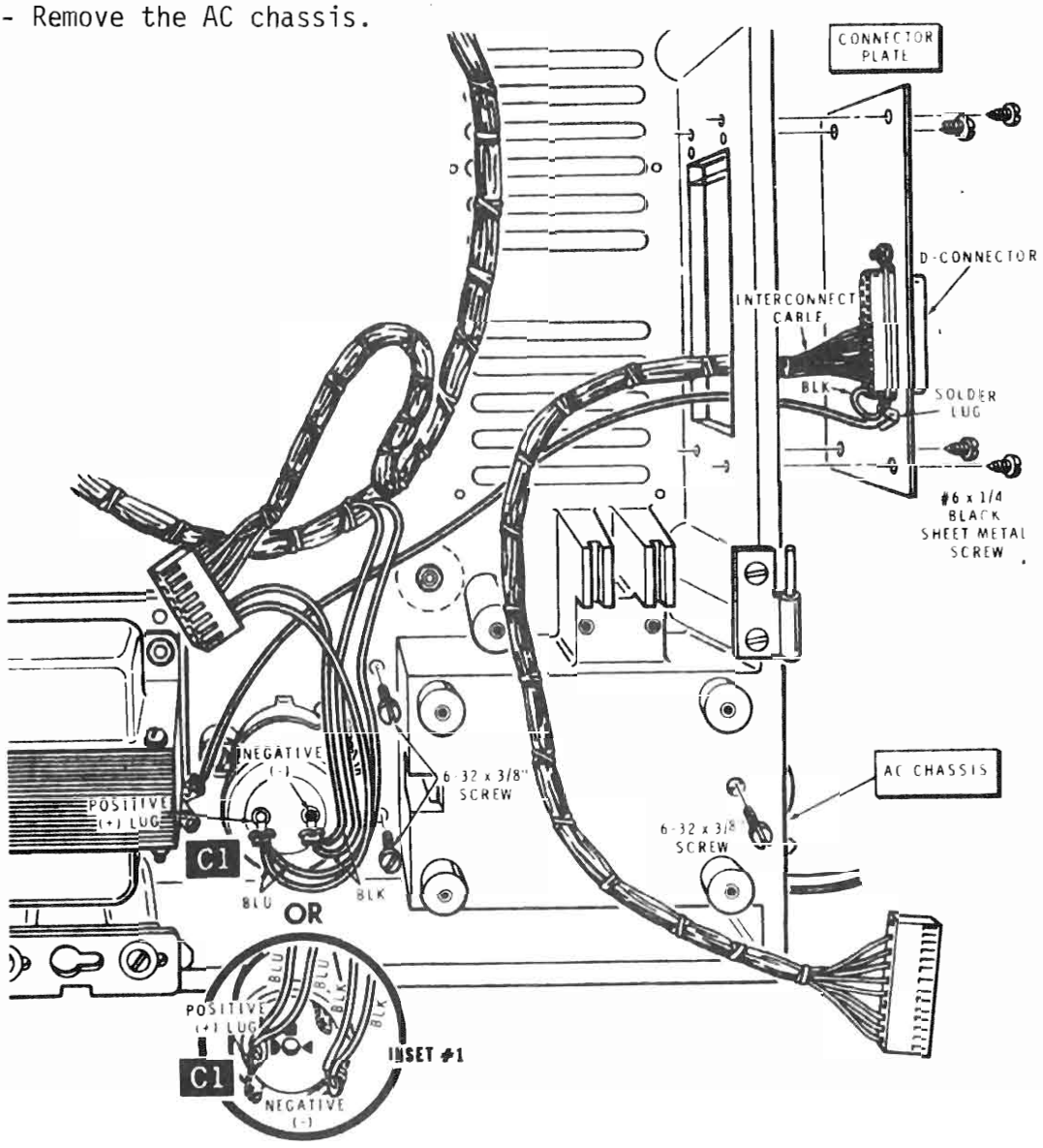
KEYBOARD COVER REMOVAL

- Remove the keyboard cover as shown in the pictorial at the right.



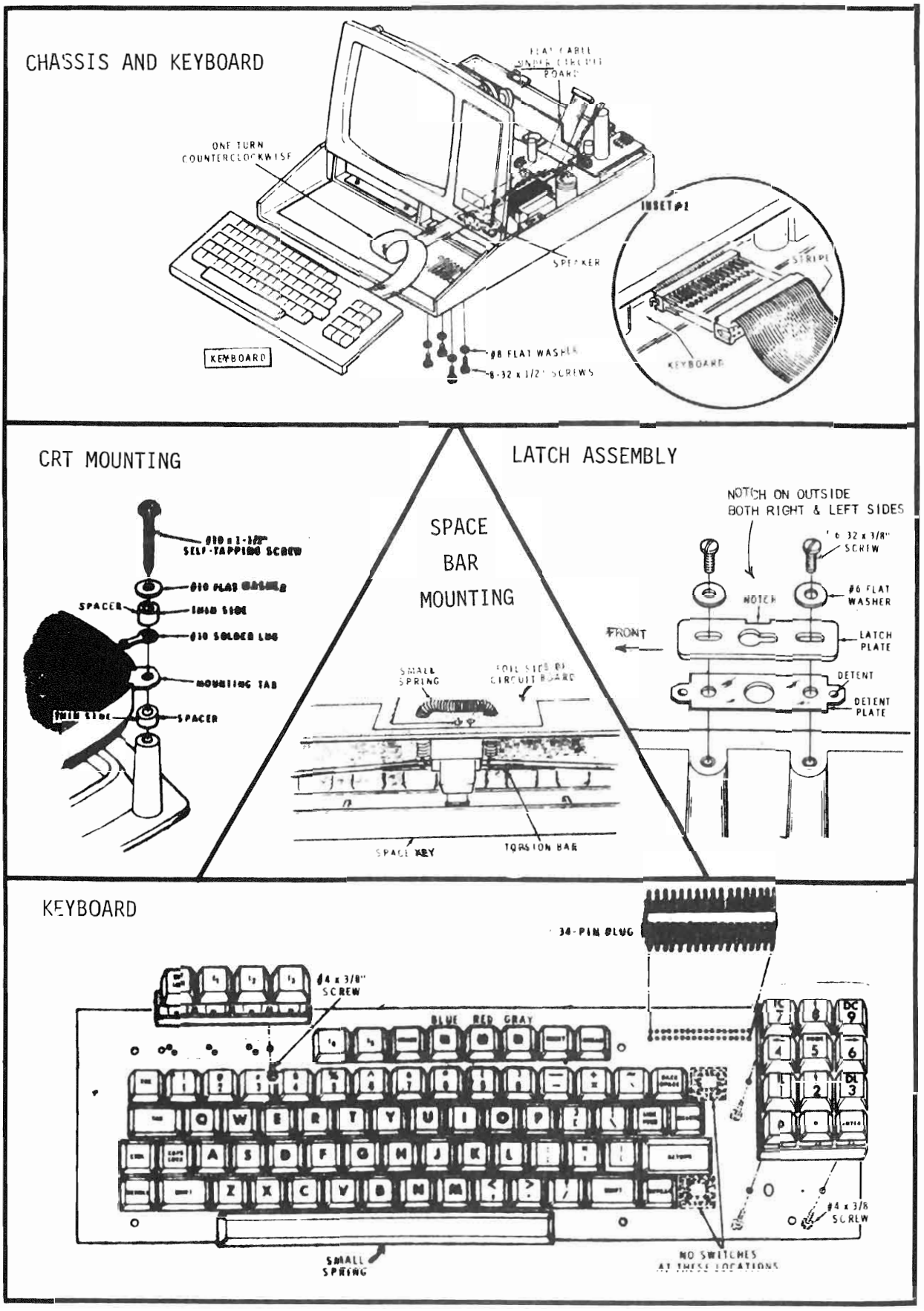
POWER SWITCH AND FUSE HOUSING ASSEMBLY REMOVAL (AC CHASSIS)

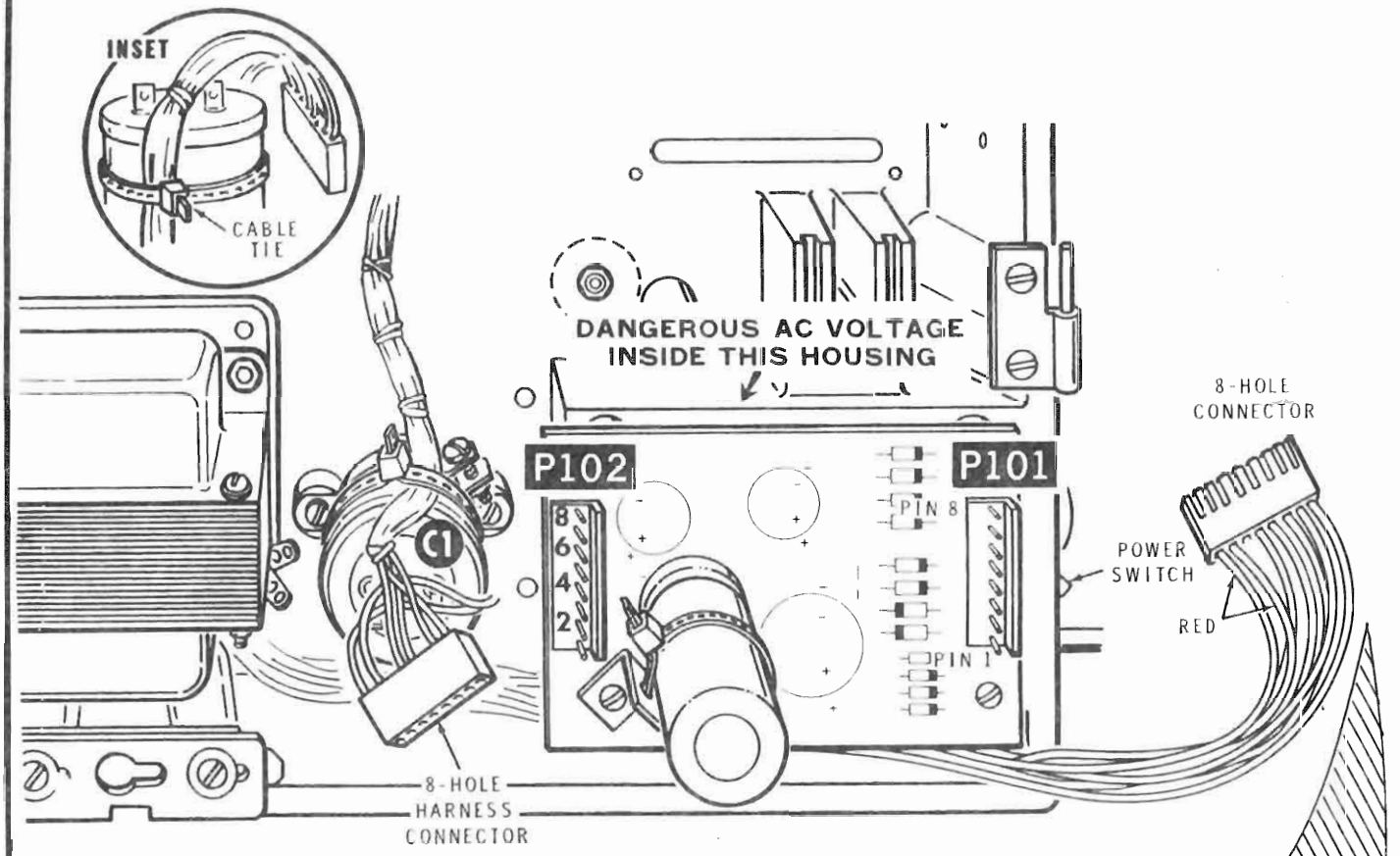
- Remove the four screws holding the Power Supply board.
- Remove the Power Supply board.
- Remove the three 6-32 x 3/8" screws holding the AC chassis.
- Remove the AC chassis.

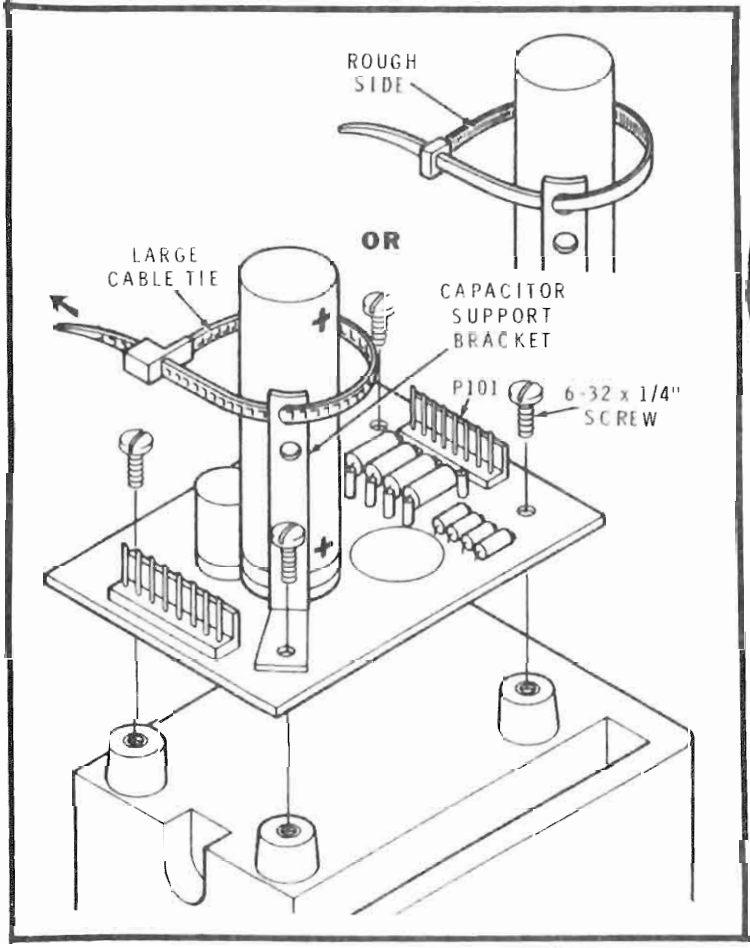


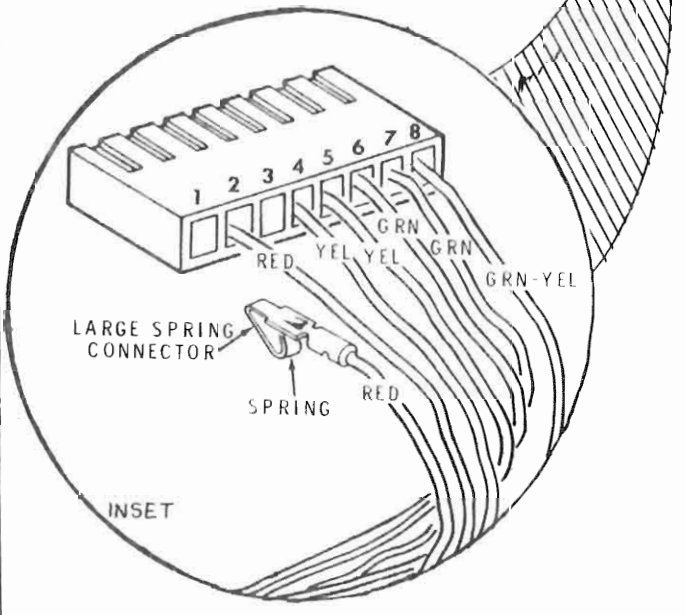
NOTES:

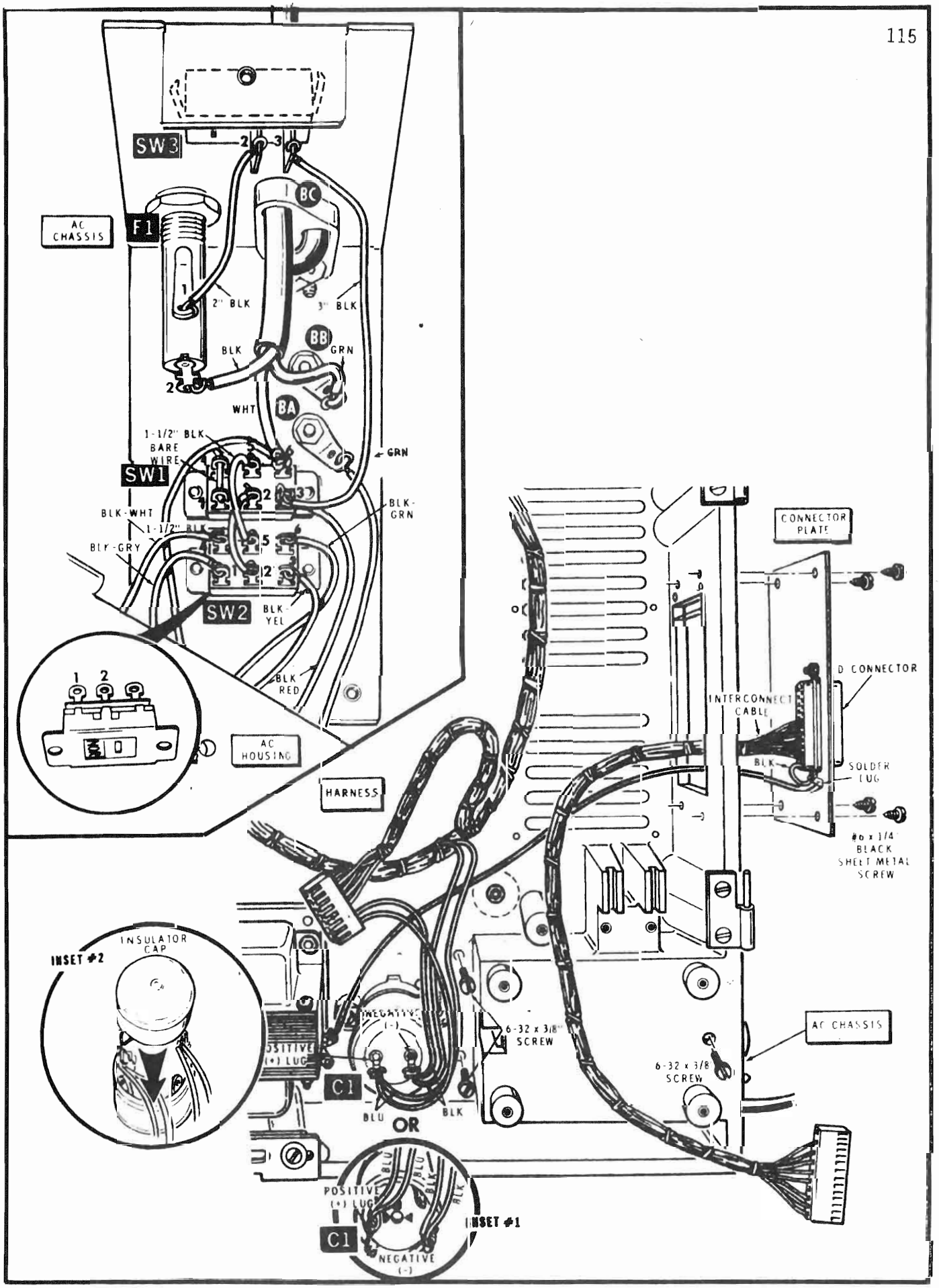
VISUAL CHECKS



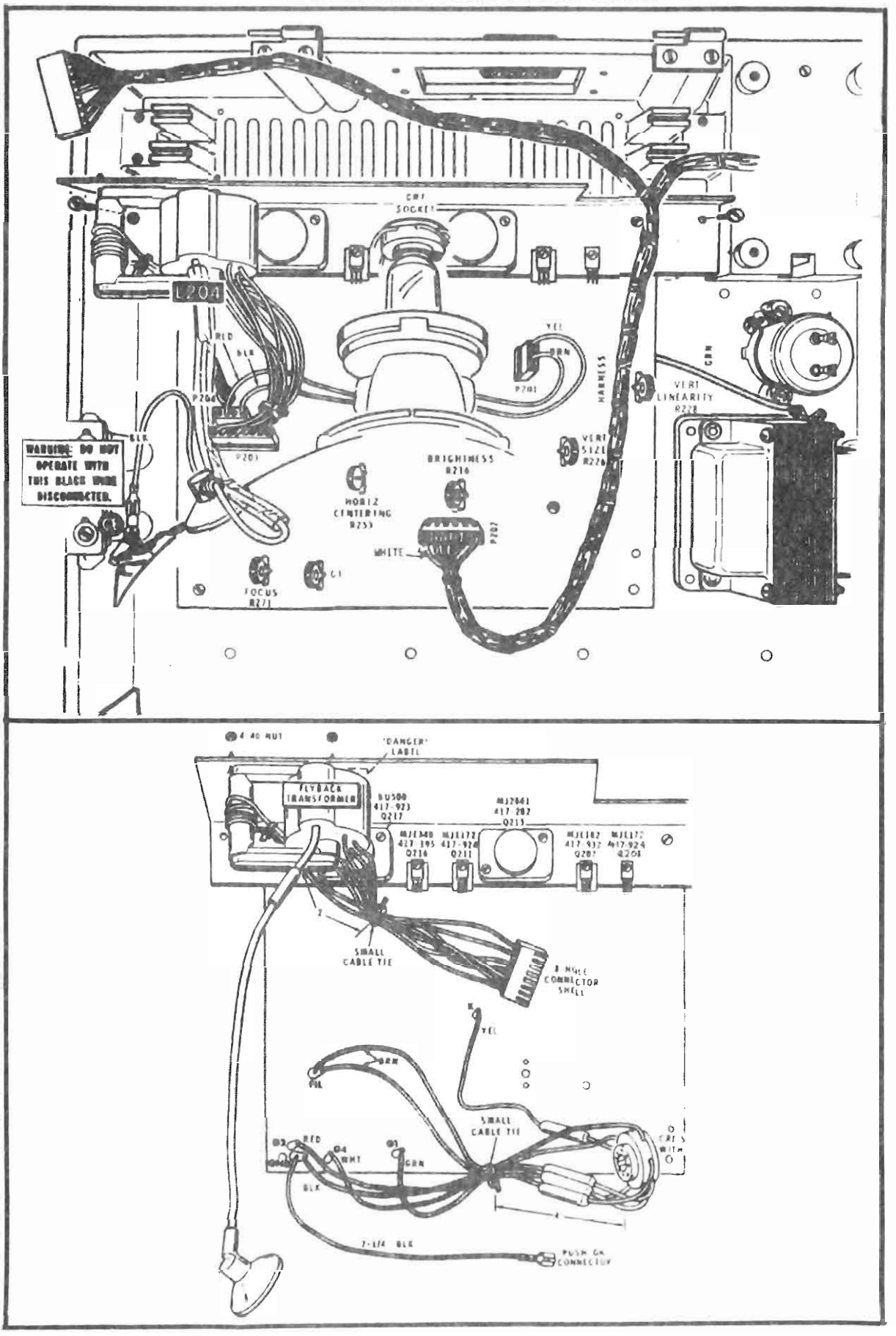

INSET
CABLE TIE
DANGEROUS AC VOLTAGE INSIDE THIS HOUSING
P102
P101
8
6
4
2
PIN 8
PIN 1
C1
8-HOLE CONNECTOR
POWER SWITCH
RED
8-HOLE HARNESS CONNECTOR

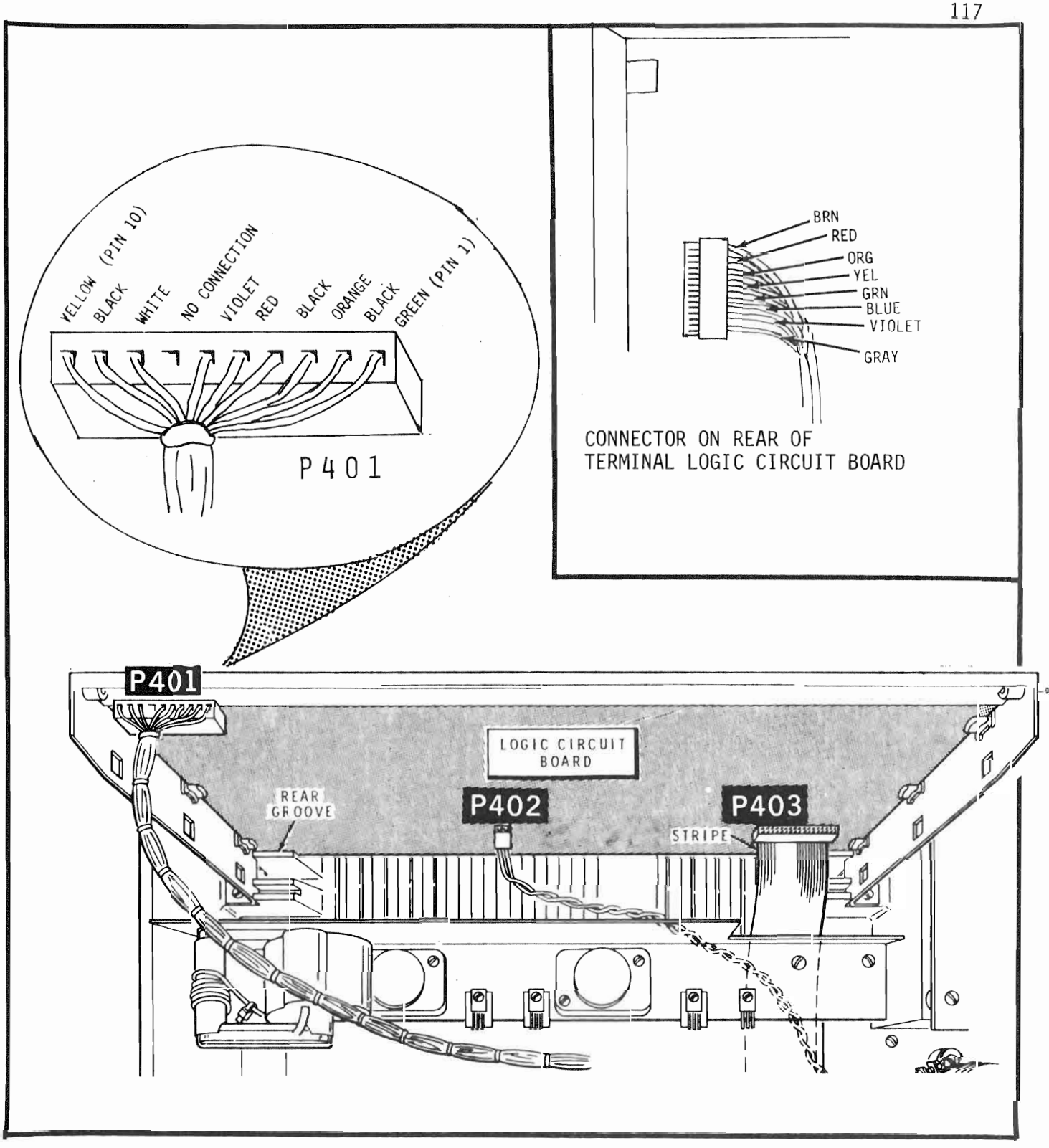

ROUGH SIDE
OR
LARGE CABLE TIE
CAPACITOR SUPPORT BRACKET
P101
6-32 x 1/4" SCREW


1 2 3 4 5 6 7 8
RED
YEL
YEL
GRN
GRN
GRN-YEL
LARGE SPRING CONNECTOR
SPRING
RED
INSET


SW3
2
3
BC
AC CHASSIS
F1
1
2" BLK
3" BLK
BLK
BB
GRN
2
WHT
BA
1-1/2" BLK BARE WIRE
GRN
SW1
2
3
BLK-WHT
1-1/2" BLK
BLK-GRN
BLK-GRY
5
1
2
SW2
BLK-YEL
BLK RED
1
2
3
AC HOUSING
HARNESS
CONNECTOR PLATE
D CONNECTOR
INTERCONNECT CABLE
BLK
SOLDER LUG
#6 x 1/4 BLACK SHEET METAL SCREW
INSET #2
INSULATOR CAP
NEGATIVE (-)
6-32 x 3/8" SCREW
POSITIVE (+) LUG
C1
BLU
BLK
OR
AC CHASSIS
6-32 x 3/8 SCREW
POSITIVE (+) LUG
BLU
BLU
BLK
BLK
C1
NEGATIVE (-)
INSET #1

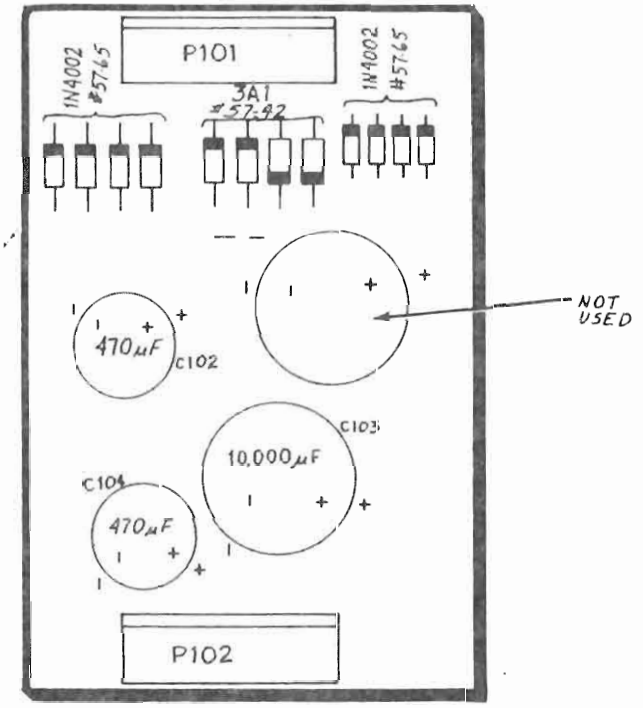
VIDEO CIRCUIT BOARD WIRING CHECKS





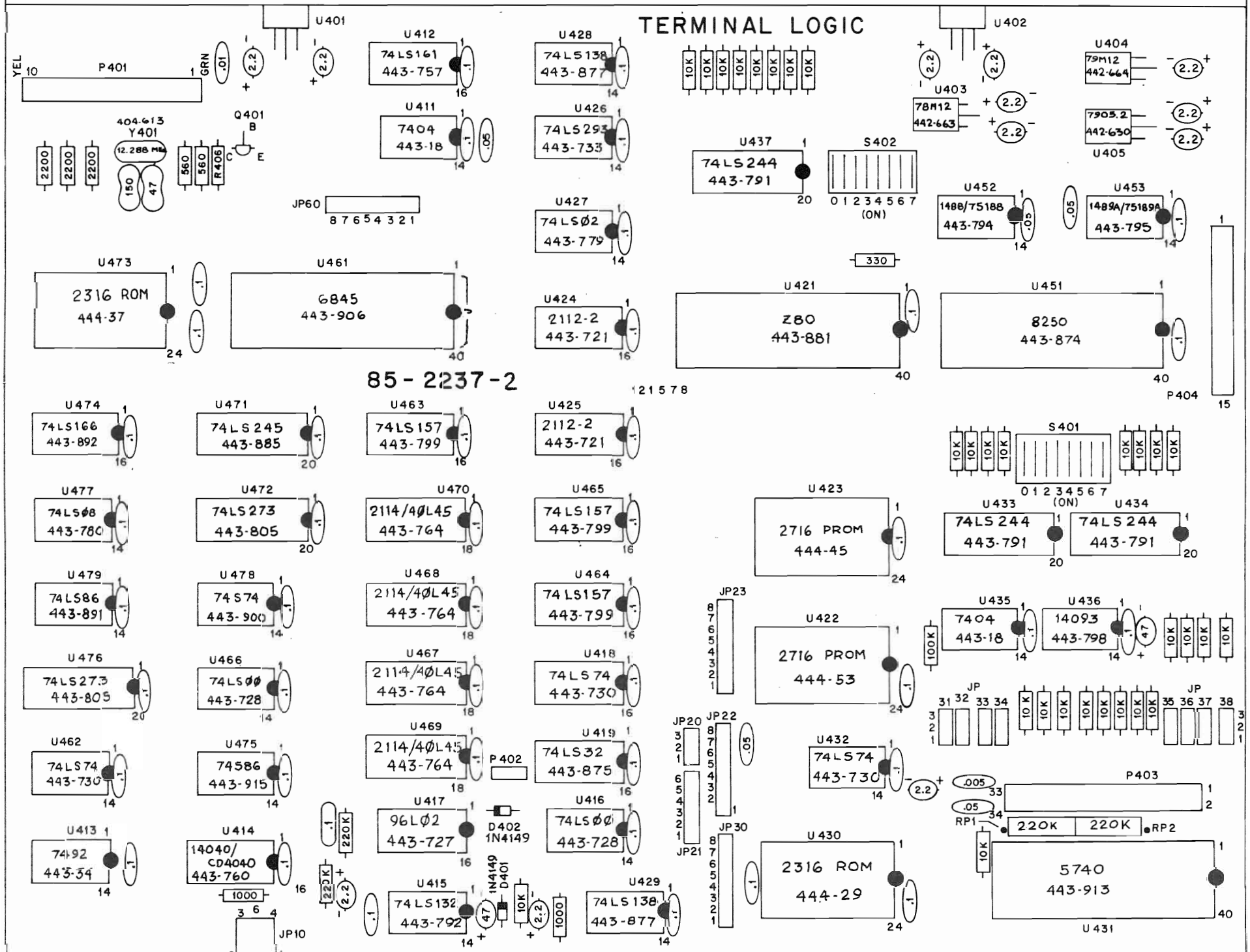
TERMINAL LOGIC CIRCUIT BOARD WIRING CHECKS

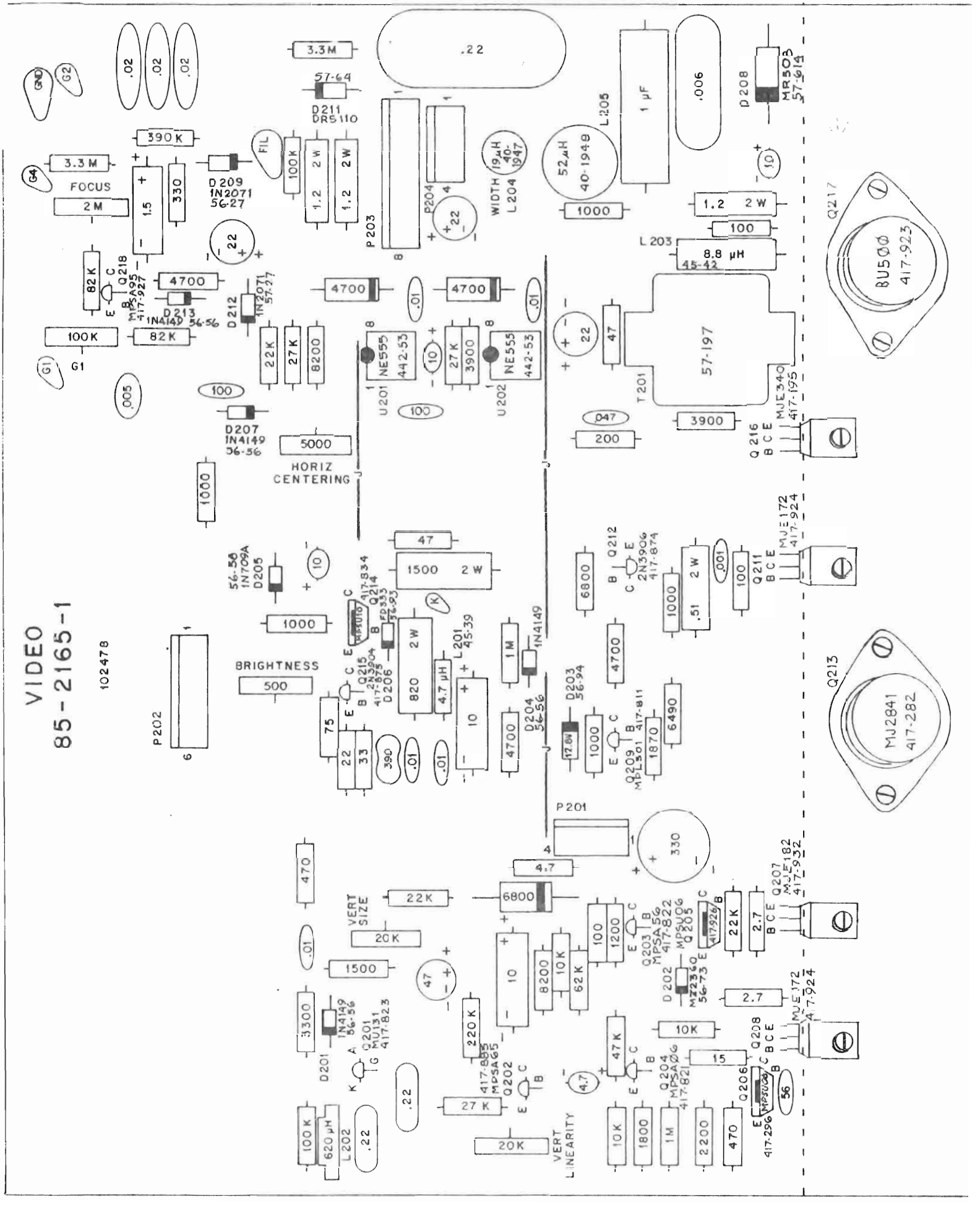
CIRCUIT COMPONENT LOCATIONS AND VALUES



POWER SUPPLY CIRCUIT BOARD

TERMINAL LOGIC



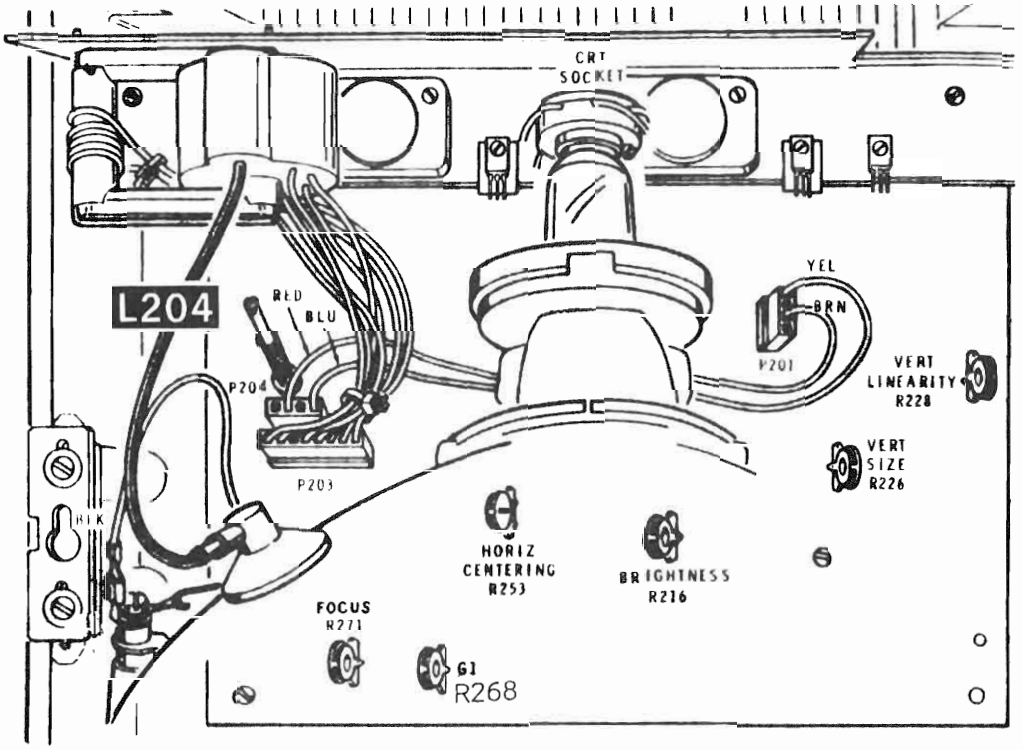

VIDEO
85-2165-1
102478
FOCUS
BRIGHTNESS
HORIZ CENTERING
VERT SIZE
VERT LINEARITY
WIDTH
L204
L205
L203
T201
57-197
U201
U202
NE555
442-53
P201
P202
P203
P204
Q217
BU500
417-923
Q213
MJ2841
417-282
Q216
MJE340
417-195
Q211
MJE172
417-924
Q212
2N3906
417-874
Q207
MJE182
417-932
Q208
MJE172
417-924
Q206
417-296
Q204
MPSA06
417-821
Q203
MPSA56
417-822
Q202
417-885
MPSA65
Q201
MU131
417-823
Q209
MPL501
417-811
Q215
2N3904
417-875
Q214
FD333
56-93
Q218
MPSA95
417-927
D209
1N2071
56-27
D211
DRS110
57-64
D208
MR503
57-614
D212
1N2071
57-27
D213
1N4149
56-56
D207
1N4149
56-56
D205
1N709A
56-56
D206
56-56
D204
56-56
D203
56-94
D202
MZ2360
56-73
D201
1N4149
56-56
L201
45-39
L202
620 µH
L203
8.8 µH
45-42
L204
40-1947
19 µH
L205
40-1949
52 µH
G1
G2
G4
GND

ADJUSTMENTS

No special equipment is needed to adjust the H19 Terminal, other than an alignment tool (#490-1) and a small insulated screwdriver. The direction of rotation of all controls is referenced to the rotor side of the control.

1. Set the OFFLINE and CAPSLOCK keys to their down position.

2. Set section 2 of S402 on the Terminal Logic circuit board to a logic one position (down) to enable the wrap-around function.



3. Set the following controls on the Video circuit board to the center of their rotation: (Refer to pictorial above.)

FOCUS R271
G1 R268
HORIZ CENTERING R253
BRIGHTNESS R216
VERT SIZE R226
VERT LINEARITY R228

4. Apply power to the unit. A cursor or a raster may appear in about 20 to 30 seconds.

5. Adjust the G1 control (R268) CCW until the raster appears.

6. If the display is tilted, loosen the yoke clamp screw and rotate the yoke to correct.

7. Adjust the VERT SIZE control (R226) so the display is approximately 6 inches high.

8. Rotate the ring magnets on the back of the yoke to center the display on the screen.

9. If no cursor is present, adjust the BRIGHTNESS (R216) control CW until the cursor appears.

10. Press the "Z" or "H" key on the keyboard and the repeat key at the same time until the screen is filled with characters.

11. Adjust the HORIZ CENTERING control (R253) to obtain a properly centered display.

12. Adjust the VERT LINEARITY control (R228) so that the top and bottom rows of the characters are of uniform size.

13. Adjust G1 CW until the raster just disappears.

14. If the display width is not approximately 8-1/2 inches, adjust the WIDTH COIL (L204) to correct.

15. With the BRIGHTNESS CONTROL set to a suitable viewing level (which will vary from one person to the next), adjust the FOCUS control (R271) for uniform focus across the screen. The scan lines should be sharply defined.

16. Touch-up the above controls as necessary to obtain a good display.

17. Set section 2 of S402 (on the Terminal Logic circuit board) to its original position.

TROUBLESHOOTING

INTRODUCTION

Due to the large variety of operating modes available through the 156 different "Escape" commands, it is impractical to present a comprehensive "cause and effect" approach to servicing the H19 Terminal. However, by observing the symptoms and knowing how the hardware works, the technician can quickly narrow the problem down to a group of ICs.

To illustrate, if the display is incorrect on power-up (tearing raster, improper sweep frequencies, etc.), then it's likely that the CPU didn't program the CRTC properly. Thus the CPU, clock (U411A), controller ROMs, scratchpad RAMs and address decoders should be checked first. Through substitution and proper test equipment use, the problem can be localized to a specific component.

If the customer should complain of a software-oriented problem that would not normally show up during testing (Transmit 25th Line in the ANSI Mode, for example), the controller ROMs should be suspect. However, first eliminate any hardware problems (improper address decoding, shorted data bus line, etc.) that might cause similar symptoms.

The procedures presented in this section will help narrow the problem down to a particular group of ICs by pressing certain keys on the Terminal and noting their effect.

For example, an ASCII upper case 'U' in binary has the bit pattern '01010101', while the reverse video asterisk (*) is '10101010'. If the H19 can reproduce both these properly, then the data bus and most of the data handling circuits are functioning properly.

Once the problem is narrowed down to a small number of components, use the notes, voltages, and waveforms provided on the schematic supplied with this manual and the recommended test equipment to troubleshoot down to the component.

EQUIPMENT

The test equipment required to perform the steps of the troubleshooting procedure in this manual is:

1 ea	Oscilloscope; dual-trace, DC, 15 MHz (IO-4510 or equivalent)
1 ea	Logic probe (HP-545A or equivalent)
1 ea	High voltage probe (IM-5210 or equivalent)
1 ea	VTVM or DVM (IM-5228 or IM-2202 or equivalent)
1 ea	Variable AC Power Supply (IP-5220 or equivalent)
	Extender cables* for Video circuit board troubleshooting, jumper wires with alligator clips

*See page 139 of this manual for construction detail on the the extender cables.

PROCEDURE

Thoroughly prework the unit, checking for the following problems:

- improperly installed cables,
- components in backwards,
- loose hardware,
- components installed in the wrong place,
- SW2 and SW3 settings (be sure they match the line voltage available at your bench).

Note the switch positions of S401 and S402 on the Terminal Logic circuit board so that they can be returned to their original positions after servicing (assuming that they are in a functional position now).

Set S401 and S402 to the following positions (U = UP; D = DOWN):

S401

SECTION	POSITION
0	U
1	D
2	U
3	D
4	U
5	U
6	U
7	D

S402

SECTION	POSITION
0	U
1	U
2	D
3	U
4	U
5	U
6	U
7	U

Operate the unit to verify the customer's complaint. If the H19 is blowing fuses, isolate the cause with an ohmmeter and power up the Terminal on a variable AC cupply to monitor the primary current.

If there are any reported sweep problems which may damage the CRT phosphor, unplug the CRT socket before powering up.

Upon turn-on, the Terminal should beep once, the CRT filament should glow (if it is connected), and a blinking undersocre cursor should appear in the upper left-hand corner in 20 or 30 seconds. The rest of the screen should be blank.

POWER SUPPLIES CHECK

Video Circuit Board

D204 (anode) = +53 volts DC

D205 (cathode) = +6.2 volts DC

U201, pin 8 = +6 volts DC

U202, pin 8 = +6 volts DC

D1 (cathode) = +15 kilovolts

Terminal Logic Circuit Board

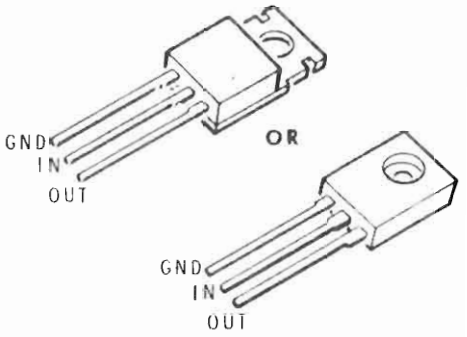
U401 (output pin) = +5 volts DC ($V_{cc}1$)

U402 (output pin) = +5 volts DC ($V_{cc}2$)

U403 (output pin) = +12 volts DC

U404 (output pin) = -12 volts DC

U405 (output pin) = -5.2 volts DC



VIDEO CIRCUIT BOARD ANALYSIS

Observing the CRT and making the measurements in the following list of symptoms can quickly determine if the problem is in the Video circuit board or the Terminal Logic circuit board. If there is a video problem, it can more easily be serviced by using the extender cables. Note that horizontal rows of dots may appear brighter than vertical columns of dots due to the added inductance of the extender cables.

No CRT Filament Glow or Blank Screen

- Check for horizontal sync at P202-1.

  If not present, the problem is in the CRTC or CPU circuits on the Terminal Logic circuit board or the interconnecting cables.

  If sync is present, then check the signal path from R249 to Q217. Note that using a direct voltmeter or oscilloscope probe will load down several test points in the Horizontal circuits and cause unpredictable results. Use a X10 probe with an oscilloscope; use a high-impedance voltmeter such as an SM-5228 to measure voltages.

- Adjust G1 (R268) FCCW (viewed from the rotor).

  If the raster doesn't appear, check for proper high voltage and CRT bias voltages at CRT.

- Adjust the BRIGHTNESS control, R216, FCW (viewed from rotor).

  If no display, check for pulses at P202-4. Use a logic probe; an oscilloscope may not be fast enough to display these pulses. If the pulses are present, check the bias voltages on Q214 and Q215. Otherwise the problem is in the CRTC, CPU, or the interconnecting cable.

Raster Present - No Vertical Sync

- Check for a 60 Hz synchronization pulse at P202-6.

  If it is present, trace the signal path from R221 to R224. Otherwise, check the CRTC on the Terminal Logic circuit board.

No Vertical Deflection

Note: To prevent possible damage to the CRT phosphor, disconnect the CRT socket before applying power.

- Check the DC voltages from Q204 through Q208.

- Check vertical deflection yoke continuity.

- Signal trace the ramp from Q201 to Q202 to the vertical deflection yoke.

No Horizontal Deflection

- Check the series path from C229, the deflection yoke, L204, L205/R273, C233 and D208.

No Horizontal or Vertical Deflection/
Very Dim Spot in Center of Tube

- Check for interchanged horizontal and vertical yoke plugs at P201 and P204.

Poor Vertical Linearity

- Check the adjustment of linearity potentiometer (R228).

- Check the ramp voltage at Q202's base and emitter.

  This is normally slightly concave to account for the curvature of the CRT faceplate. Adjusting R228 from one extreme to another should bring this ramp from a more concave slope to a nearly straight line.

  If not, check the value of R228, R229, C211, C212. Q202 may be slightly leaky also.

- Check the value of R248 and C215.

- Check the vertical yoke and C217.

- Check the bias voltages on Q203 through Q208.

  For silicon transistors, base-emitter values should range from .5 volts to .7 volts. Note however, that a slightly leaky transistor may appear to have normal operating voltages in-circuit and may still cause distortion.

Poor Horizontal Linearity

- Check Q217, D208, L205/R273, C233, L204, the horizontal yoke and C229.

Insufficient Height

- Check the adjustment of the VERTICAL SIZE control, R226.
- Check Q201 and its supporting circuitry.
- Check the base of Q204.

  A ramp approximately 3.6 volts P-P will cause a 30 V P-P signal at the junction of R246 and R247.

Improper Width

- Check for proper adjustment of width coil, L204.
- Check the voltage at the collector of Q217. Do not use a direct probe as the loading will introduce noise into the system and may produce unpredictable results.
- Check for leakage in D208.
- Check the series string of components C229, C233, L205/R273, L204, and the deflection yoke.

TERMINAL LOGIC CIRCUIT BOARD OPERATIONAL CHECKOUT

This checkout procedure should be performed in sequential order. This will permit the verification of all circuitry on the Terminal Logic circuit board. When an IC or circuit is completely checked by an operation or step a "(100%)" indication will appear after the IC number or circuit name.

For example, "Secondary Address Bus (100%)" indicates the bus has been completely checked at that point in the procedure.

When a step indicates two or more keys are to be pressed, the step will show, for example, "ESC p". This indicates the Escape key and the lower-case "p" are pressed.

- Press the OFF LINE key so that it latches in its down position (off line).

- Press the SHIFT key and the letter U.

  A capital U should be displayed and a click should be heard at the same time. This verifies:

  - the data bus,
  - the keyboard circuits,
  - Interrupt circuits: U427C, U428A, and U428B
  - Decoder circuits: U418 and U419
  - CRTC circuits: U461, U462A, U426B, and U466C
  - Character Generator circuits: U472, U473, U474, U475A, U475B, U477D (100%), U478A (100%), and U479A (100%),
  - a large portion of the CPU hardware support and controlling firmware:
    - Power Up/Reset circuits,
    - Decoder circuits for the controlling firmware,
    - Scratchpad RAM
    - Clock and $\overline{\text{WAIT}}$ circuits (U426 and U427A, B),
    - U417, U416C, and U415C (verified when the click was heard when the U was pressed).

- Press the ESC p

  The speaker should click with each entry and p should not appear on the screen.

  • This verifies that the firmware is capable of detecting an Escape function.

- Press the SHIFT 8 at the same time.

  A reverse-video asterisk (*) should appear to the right of the U. This verifies:

  • The Secondary (Refresh) Data Bus (100%)

  • The Data Bus Gate: U471

  • Reverse Video Circuits: U472 (100%), U478B, U477A (100%), U476H (100%), and U475B (100%)

  • CPU controlling firmware and scratchpad locations that masks the ASCII character for reverse-video format prior to writing it into the Display Memories: U422, U423, U424, and U425.

  The cursor should now be to the right of the reverse-video asterisk, or three character positions from the left-hand margin. This verifies:

  • The CRTC cursor positioning circuits: U461

  • Cursor Delay and processing circuits: U476F (100%), U476G (100%), and U475A (100%)

  • CPU controlling firmware and scratchpad locations that update the cursor position during vertical retrace.

- Release the OFF LINE key (up) and press any printable character key. No character should be displayed.

  If the character is displayed, check:

  The Scratchpad RAMS: U424 and U425,

  Section 7 of S401,

  Buffers: U434 and U433,

  The OFF LINE key.

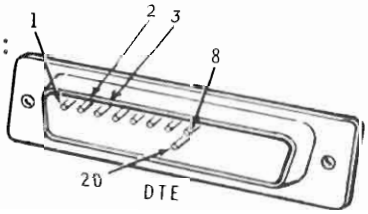
- With a jumper wire, short together pin 2 and pin 3 of the serial I/O connector (P1) located on the rear panel. Again press a displayable character key.

  If the character appears on the CRT, this verifies:

  • I/O decoder: U418, pin 13

  • Interrupt circuits: U427C

  • Serial I/O port: U451, U452, and U453



- Press the CAPS LOCK key so that it latches down.

- Press the RIGHT SHIFT key and the RESET key simultaneously to bring the Terminal to the original power-up mode.

- Hold the letter U and REPEAT key down until all 24 lines are filled with upper case U's.

  This verifies:

  - The Main and Secondary Address Bus Lines
  - Address Bus Multiplexers: U463, U464, U465
  - Memory Address Decoders: U466A, U466B
  - Read/Write Gate: U429C
  - Display RAMs: U467 to U470
  - CAPS LOCK key

- Press RIGHT SHIFT and RESET keys at the same time to restore the H19 Terminal to the original power-up mode.

- Press the ESC p keys for reverse video.

- Hold down the SHIFT and 8 key and the REPEAT key until the screen is filled with reverse video asterisks (*).

  This verifies:

  - All display Ram locations except that reserved for the 25th line: U467 through U470.

- Enter the following Escape sequence: ESC x 1

  This will enable the 25th line.

- Enter ESC Y 8

- Press the SPACE bar.

  This will place the cursor on the first character position in the 25th line. This verifies:

  - The Direct Cursor Addressing Escape sequence in firmware, scratchpad, RAM, and most of the CRTCs (U461) internal registers.
  - The 25th Line Enable Escape function.

- Using the REPEAT key, fill the 25th line with reverse video asterisks.

  This verifies:

  • The Secondary Address Bus (100%),

  • The Address Bus Multiplexers (100%), U463 through U465.

- Press the RETURN key.

- Enter the following Escape sequence: ESC q

  This restores the direct video mode.

- Using the REPEAT key, fill the 25th line with upper case U

  This verifies:

  • RETURN processing firmware,

  • Exit Reverse Video Escape processing,

  • Display RAMs (100%): U467 through U470.

- Press the SHIFT and RESET keys to restore the original operating mode.

- Press ESC F

  You will now be in the graphics mode.

- Using the ASCII Chart on page 16, enter each graphics character at least once.

  This verifies:

  • Operating firmware for the graphics function,

  • Portions of the scratchpad RAM,

  • Character generator, U473.

- Press the SHIFT and RESET keys.

- Enter all displayable characters (shift and unshift) at least once.

  This verifies:

  • Character generator: U473 (100%),

  • Keyboard circuits: U430 and U431,

- Latch the OFF LINE key to its down position.

- Enter ESC #

  This will initiate the transmit page function.

  One to three seconds later, the bell should sound once. Any characters prsent may be interrupted by intermittent blanking. This verifies:

  • Transmit page software in the Controller ROM and scratchpad.

- Release the OFF LINE key (up).

  The jumper wire should still be installed from pin 2 to pin 3 at the serial I/O connector on the back panel.

- Again initiate the transmit page function by entering ESC #

  The bell should sound continuously for about 3 seconds. This verifies:

  • Buffer Overflow Software in the Controller ROM and scratchpad.

Power-Up Logic Switch Test

- Test the functions of the Power-Up Logic Configuring switch, S402. Set the eight switch positions to "UP". Now reset the Terminal (Right Shift/RESET).

  The function shown to the left of the slash (/) mark in the table below should be operative.

Section	Description	Notes
0	Underscore Cursor/Block Cursor	
1	Key click/ No key click	
2	Discard End of Line/Wrap Around	
3	No Auto LF on CR/Auto LF on CR	
4	No Auto CR on LF/Auto CR on LF	
5	Heath Mode/ANSI Mode	A quick test of the ANSI mode is to enter: ESC [p The Terminal should transmit page.

6	Keypad Normal/Keypad Shifted	The KEYPAD NORMAL can be quickly checked by pressing any of the keys on the keypad. Pressing any of the double-entry keys will cause the symbol on the lower portion of the key to be printed. KEYPAD SHIFTED will allow cursor positioning or character and line manipulation without pressing the SHIFT key at the same time.
7	60 Hz/50 Hz Refresh	Any displayed character will jitter when in the 50 Hz Refresh mode when running the Terminal off a 60 Hz power line.

- Now place the switch positions of S402 in the DOWN position; reset the Terminal (Shift/Reset), and test for operation of the function on the right of the slash mark in the previous table.

  This verifies:

  - S402,
  - U437,
  - U422,
  - U423.

- Return S402 switches to the following positions:

Section	Position
0	up
1	up
2	down
3	up
4	up
5	up
6	up
7	up

- Reset the Terminal (R shift/RESET).

Baud Rate Switch Test

To check the baud rate:

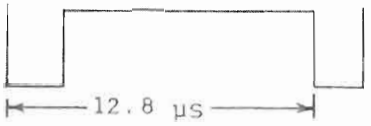
- Set S401 to 4800 baud as follows:

S401	Section	0	1	2	3	4	5	6	7
	Position	U	D	U	D	U	U	U	D

- Reset the Terminal (R shift/reset).

- Connect an oscilloscope to U451, pin 9 or pin 15.

  The period of the signal at U451, pin 9, should measure approximately 12.8 µs.

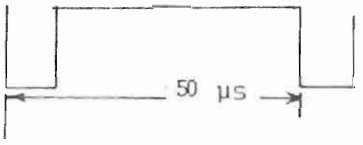


- Set S401 to 1200 baud as follows:

S401	Section	0	1	2	3	4	5	6	7
	Position	D	U	D	U	U	U	U	D

- Reset the Terminal (R shift/RESET).

  The period of the signal at U451, pin 9 should measure approximately 50 µs.



This verifies:

- S401
- U433
- ROMs: U422 and U423
- RAMs: U424 and U425
- ACE: U451

TEST JIG EXTENDER CABLES

In order to more efficiently service the Video circuit board, it should be placed outside the chassis so that both sides can be reached. Since only one cable is long enough to reach from the chassis to the Video circuit board, some extender cables will have to be built.

Parts Required

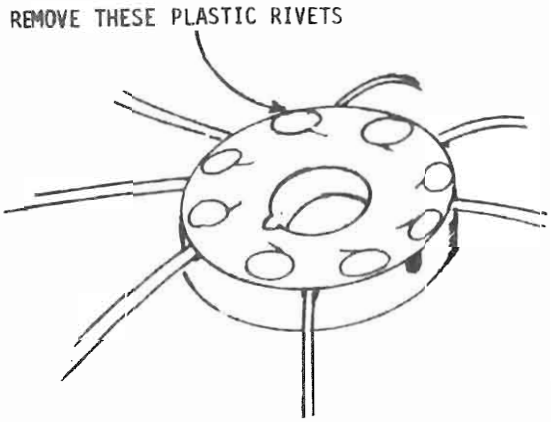
Qty	Description	Heath Part No.
3-1/2'	Green stranded wire	344-155
1'	Heat-shrink tubing	346-66
1	Epoxy	351-6
1	8-pin plug	432-122
4	Spring connectors	432-753
2	4-pin plug	432-827
2	4-pin socket shell	432-954
2	CRT socket	434-235

Procedure

1. Locate the 8-pin plug (#432-122) and remove the pins with a pair of long-nose pliers. Discard the base.

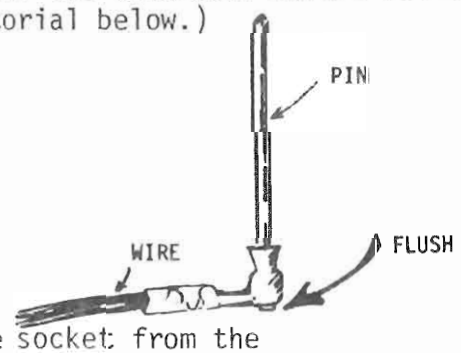
2. Insert the pins that were removed in the above step into the socket holes of one of the CRT sockets (#434-235). Leave pin 6 empty. Be sure the inserted pins are snug.

3. With a sharp knife or diagonal pliers, cut off the plastic rivets which hold on the back of the socket and remove the back of the socket. (See pictorial at right.)



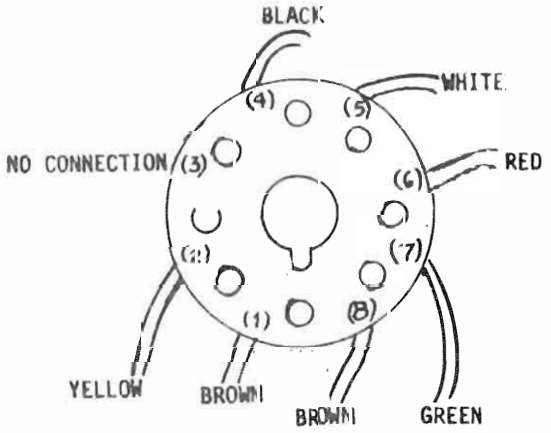
4. Remove the female connectors from the CRT socket. The pins should remain inserted.

5. Position the pin in each connector so that it is flush with the rear of the connector before soldering it. (Refer to pictorial below.)



6. Looking at the socket from the rear (rivet side), reinstall the connectors in the following order:

Pin	Color
8	Brown
7	Green
6	Red
5	White
4	Black
3	No Connection
2	Yellow
1	Brown

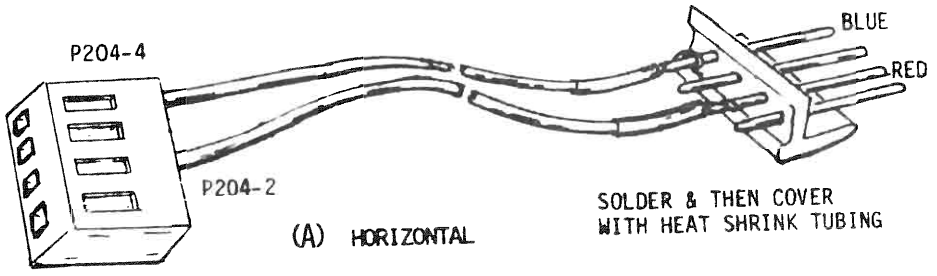


7. Replace the back cover with the epoxy (#351-6) applied sparingly around the outer rim of the socket. Hold this in place with rubber bands overnight to allow the epoxy to properly harden.

8. Cut seven one-inch lengths of heat-shrink tubing (#346-66) and slide over the wires of one of the CRT socket assemblies.

9. Solder together the two CRT socket assemblies, matching the wire color codes, and finish construction by sliding the heat-shrink tubing over the connections and heating.

HORIZONTAL AND VERTICAL DEFLECTION YOKE EXTENDER CABLES



(A) HORIZONTAL



(B) VERTICAL

1. Cut the stranded wire (#344-155) into four 10-inch lengths.

2. Install a spring connector (#432-753) on one end of each wire/

3. Insert two spring connectors at pins 2 and 4 of the horizontal 4-pin socket shell (#432-954) and the other two in pins 1 and 3 of the vertical shell. (Refer to pictorial.)

4. Slide shrink tubing over the other end of each wire.

5. Solder the other ends of the wires to pins 2 and 4 of the one 4-pin plug (#432-827) for the horizontal and pins 1 and 3 for the vertical plug.

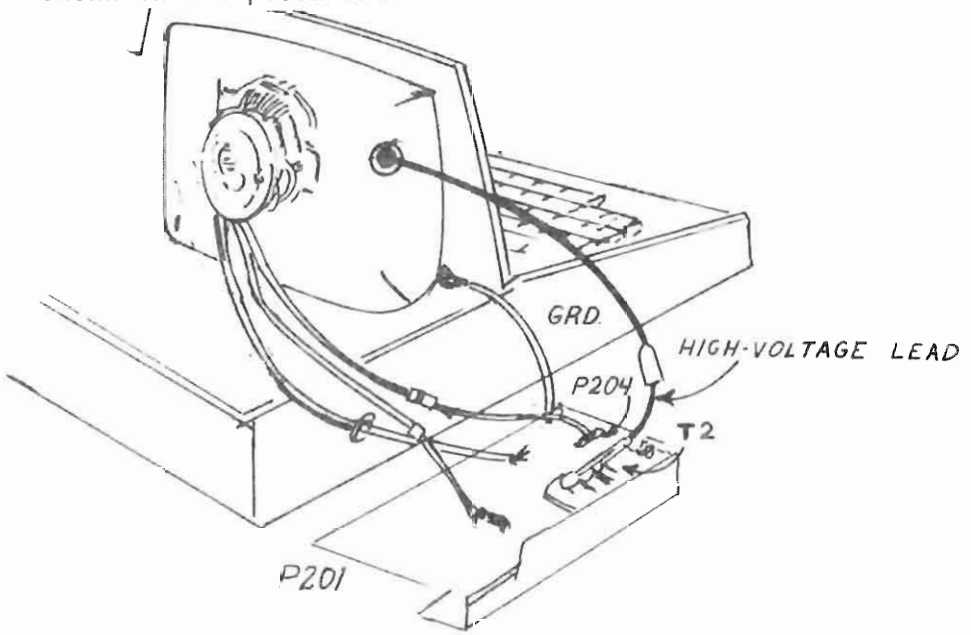
6. Slide the shrink tubing over the connections and heat.

7. For ease of identification, mark an H and V on the connector shells with a marking pen.

TEST JIG INSTALLATION

1. Remove the Horizontal and Video circuit boards as described in the Disassembly section of this manual.

2. Position the Vertical board as shown in the pictorial.



3. Connect the three extender cables as shown.

   The blue/red yoke wires are the horizontal and go to P204.

4. Reconnect the CRT ground wire and high voltage lead.

5. Reconnect P202.

6. Reinstall the circuit board brackets and the Terminal Logic circuit board.

7. Reconnect the Terminal Logic board plugs.

The H19 Terminal is ready to test. Note that the added inductance of the CRT extender cable may cause the horizontal and vertical portions of the displayed character to be of unequal brightness.

FINAL CHECKS

The following Physical and Functional Checks must be made to each unit before it is returned to the customer.

PHYSICAL CHECKS

- All plugs properly installed (double-check the speaker plug, P402 on the Terminal Logic circuit board--it's easy to overlook).
- All hardware installed and tightened.
- CRT faceplate clean.
- Cabinet clean and free of nicks and scratches.
- Correct fuse installed.
- Normal-Low switch in the Normal position.
- Line voltage switch set to the voltage range at which the H19 Terminal will be operated.
- S401 and S402 set to the Heath-recommended operating mode or to the mode specified by the customer.
- I/O cable (if supplied) in good working order (no bent connector pins or broken wires).
- Line cord is not nicked, frayed or burned. Replace the line cord if the grounding pin has been removed from the plug.
- The high-voltage lead positioned away from the front panel bracket and excess slack looped and tied with a cable tie.
- The cables to P101 on the Power Supply circuit board positioned so they will not be pinched when the cabinet shell is closed.
- The cabinet-shell latches function properly.
- Paperwork in order.

FUNCTIONAL CHECKS

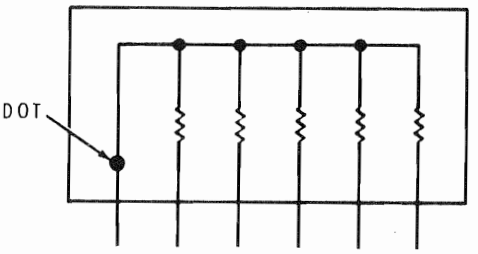
- Unit beeps once on turn-on.
- Blinking cursor appears in the upper left-hand corner, the rest of the CRT is blank.
- Keys click when pressed. Control "G" rings the bell.
- All keys function properly.
- All major special functions work properly:
  - Reverse video,
  - Graphics,
  - Direct cursor positioning,
  - 25th line.
- Unit functions properly "on-line." If a computer isn't available, short pins 2 and 3 of the rear DTE connector to check.

IC DATA

SEMICONDUCTOR IDENTIFICATION CHARTS

RESISTOR PACK

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION
9-98		220 kΩ resistor network



LEAD CONFIGURATION (TOP VIEW)

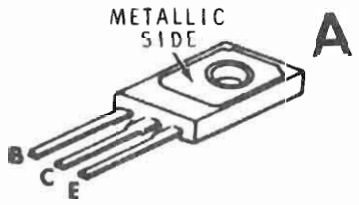
DIODES

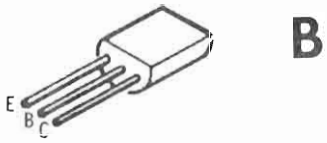
56-56	1N4149	10 mA, 75 V
56-58	1N709A	Zener, 6.2 V, 25 mA
56-73	MZ2360	Compensation
56-93	FD333	225 mA, 125 V
56-94		Zener, 12.8 V, 12 mA
57-27	1N2071	SI Rectl 1 A, 600 V
57-42	3A1	SI rect 3A, 100 V
57-64	DRS-110	SI Rectl 1A, 1000 V
57-65	1N4002	SI Rect 1A, 100 V
57-614	MR-508	SI Rect 3A, 800 V

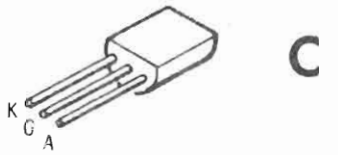
TRANSISTORS

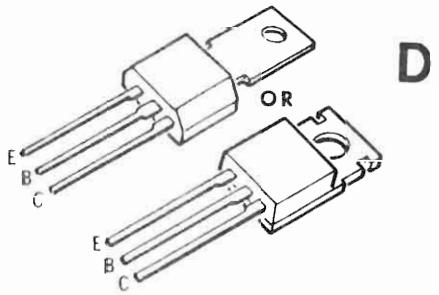
HEATH PART NUMBER	MAY BE REPLACED WITH	BASING DIAGRAM
417-195	MJE340	A
417-282	MJ2841	E
417-811	MPSL01	B
417-821	MPSA06	B
417-822	MPSA56	B
417-823	MPU131	C
417-834	MPSU10	D
417-874	2N3906	B
417-875	2N3904	B
417-885	MPSA65	B
417-923	BU500	E
417-924	MJE172	A
417-926	MPSU06	D
417-927	MPSA93	B
417-932	MJE182	A

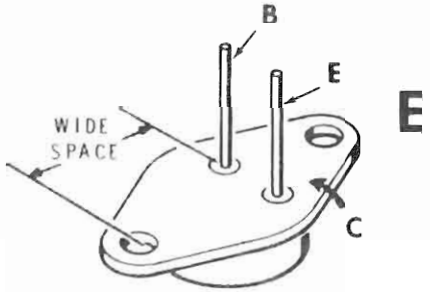
LEAD CONFIGURATION



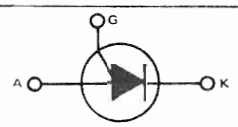








#417-823
MPU131



SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor trigger, oscillator, pulse and timing circuits. The MPU131, MPU132 and MPU133 may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 5.0 nA Maximum
- High Peak Output Voltage - 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

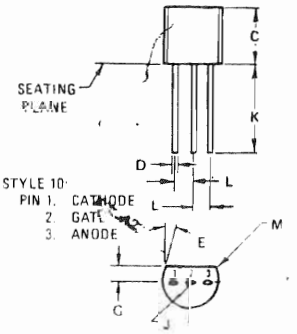
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	±20	mA
Repetitive Peak Forward Current 100 µs Pulse Width, 1.0% Duty Cycle 20 µs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non Repetitive Peak Forward Current 10 µs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

40 VOLTS
375 mW





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
C	4.450	4.700	0.175	0.185
D	0.407	0.483	0.016	0.019
E	5° NOM		5° NOM	
G	1.150	1.390	0.045	0.055
J	2.160	2.420	0.085	0.095
K	12.700	–	0.500	
L	1.270 TP		0.050 TP	
M	0.076	0.330	0.003	0.013

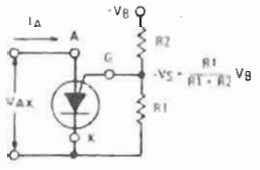
CASE 29-01

#417-823
MPU131 (cont)

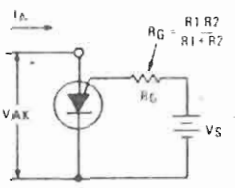
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current	MPU131	2,9-14	I_P	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			–	0.19	0.30	
	MPU133			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			–	4.0	5.0	
	MPU132			–	1.20	2.0	
	MPU133			–	0.70	1.0	
Offset Voltage	MPU131	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			0.2	0.50	0.6	
	MPU133			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms) (All Types)				0.2	0.35	0.6	
Valley Current		1,4,5,	i_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131, 132			–	18	50	
	MPU133			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			70	270	–	
	MPU132, 133			50	270	–	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

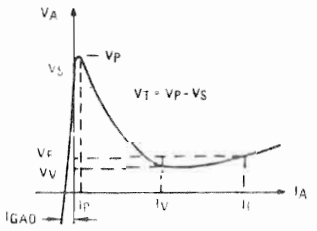
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2



1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)



1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

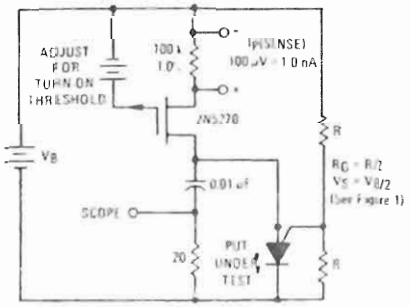
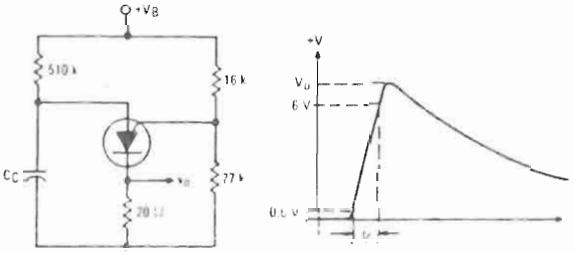


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

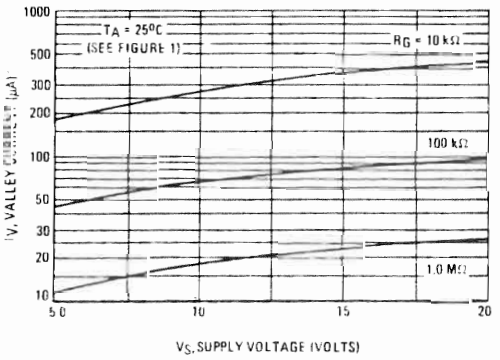


FIGURE 5 – EFFECT OF TEMPERATURE

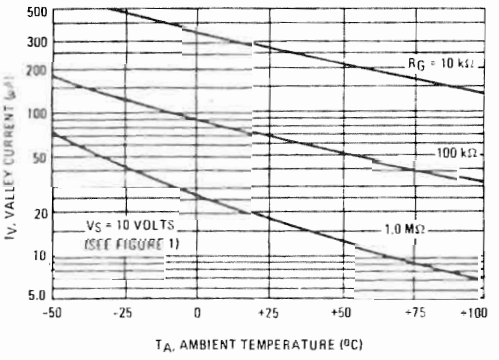


FIGURE 6 – FORWARD VOLTAGE

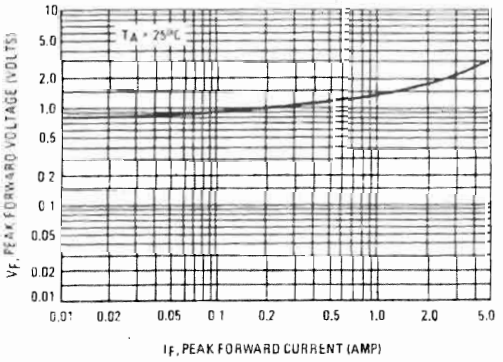


FIGURE 7 – PEAK OUTPUT VOLTAGE

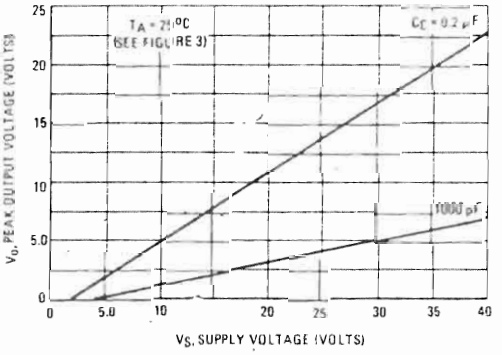
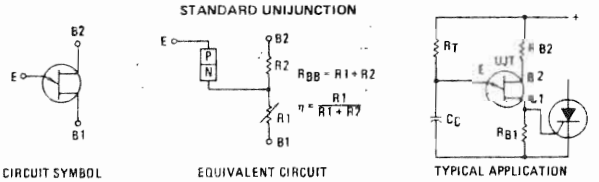
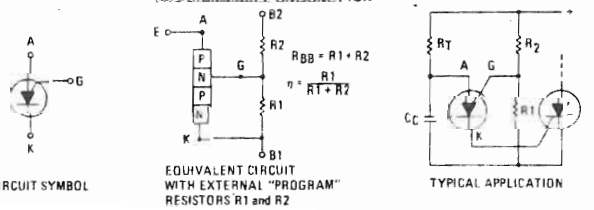


FIGURE 8 – STANDARD UNIJUNCTION
COMPARED TO PROGRAMMABLE UNIJUNCTION

STANDARD UNIJUNCTION



PROGRAMMABLE UNIJUNCTION



#417-823
MPU131 (cont)

TYPICAL PEAK CURRENT BEHAVIOR

MPU131

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

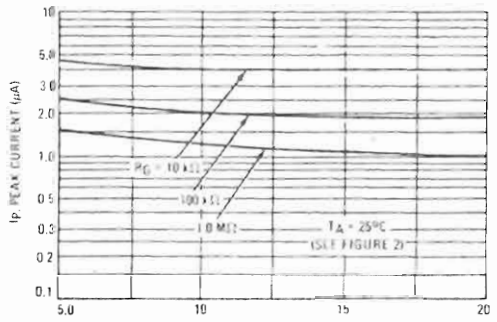
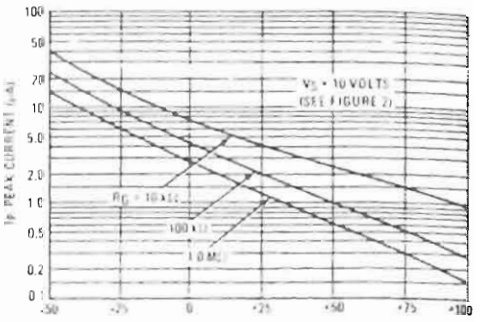


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



MPU132

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

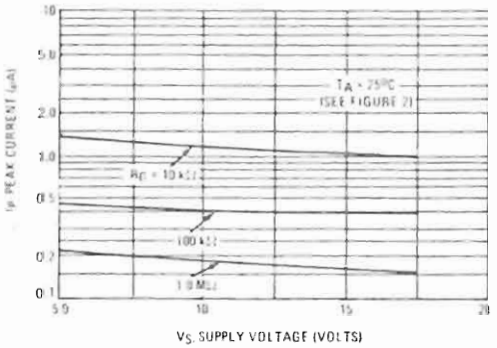
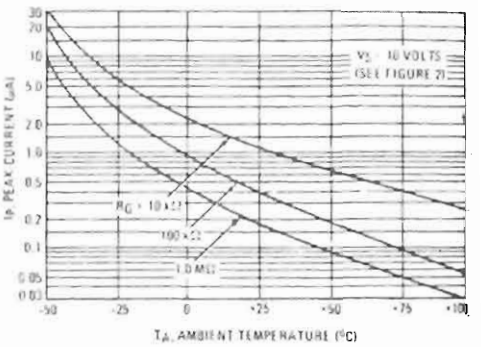


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



MPU133

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

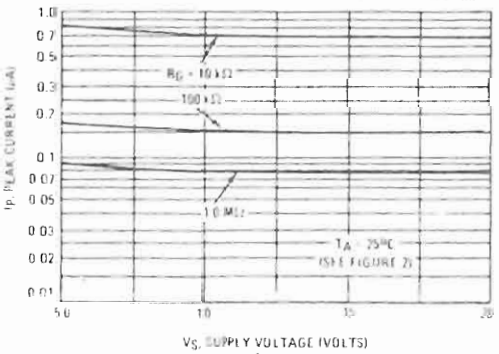
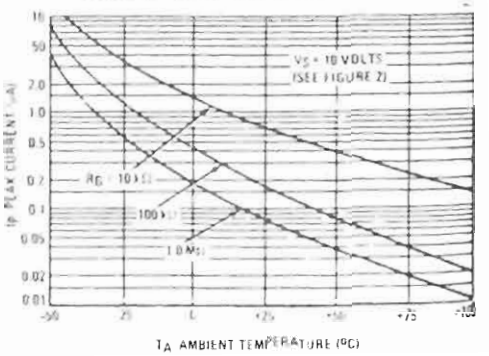


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



signetics

555

442-53

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

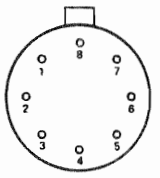
FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER ^{o}C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

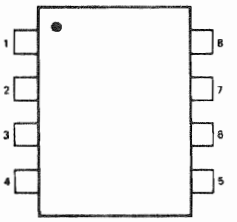
PIN CONFIGURATIONS



T PACKAGE
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T



V PACKAGE
(Top View)

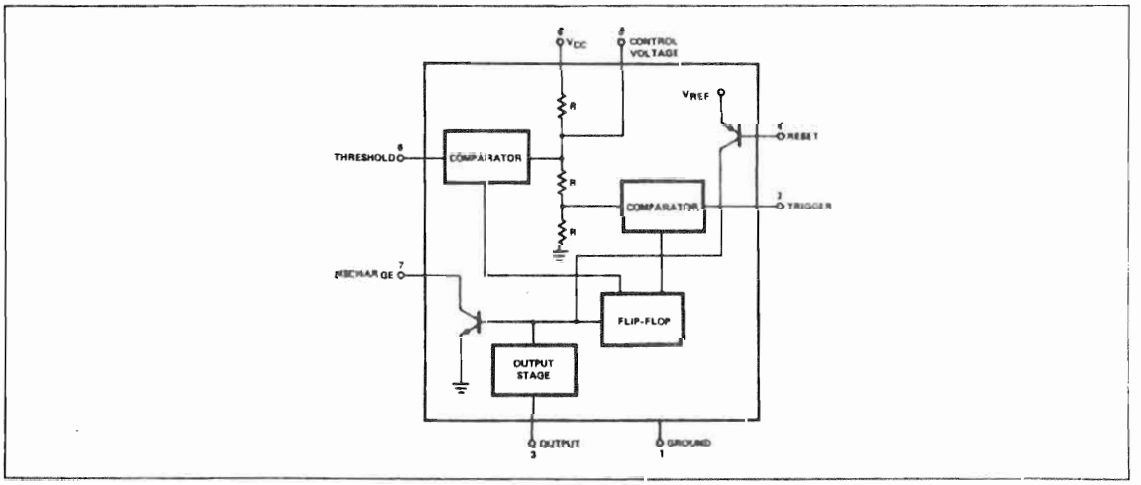
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

BLOCK DIAGRAM



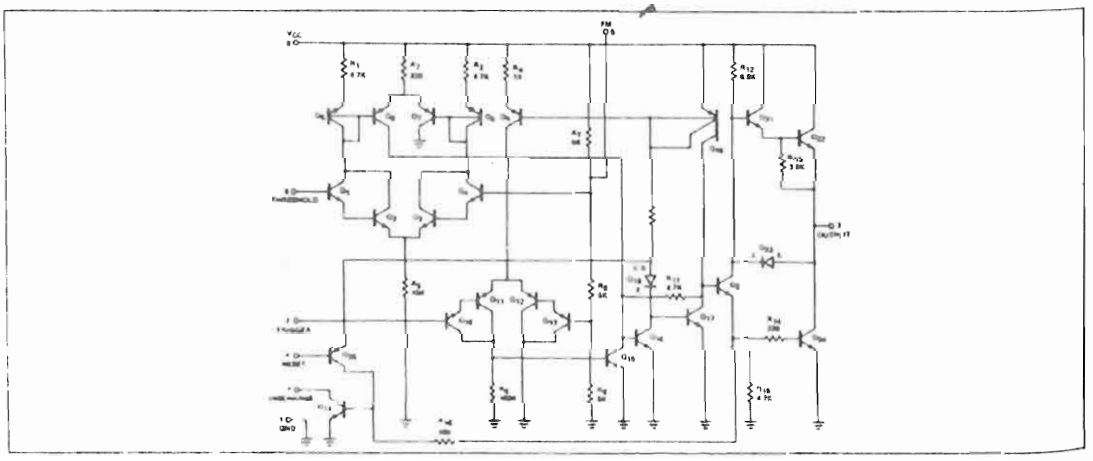
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 μF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					25	.35	
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA V_{CC} = 15V		12.5			12.5		
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

NOTES:

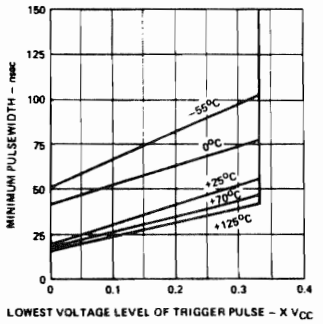
1. Supply Current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

EQUIVALENT CIRCUIT

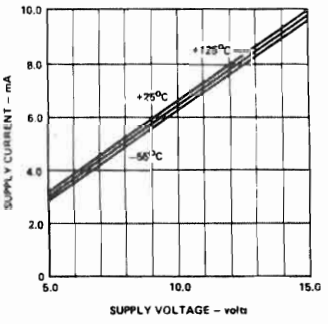


Typical Characteristics

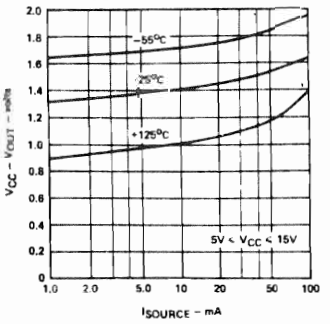
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



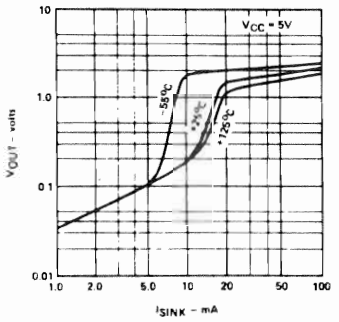
SUPPLY CURRENT vs SUPPLY VOLTAGE



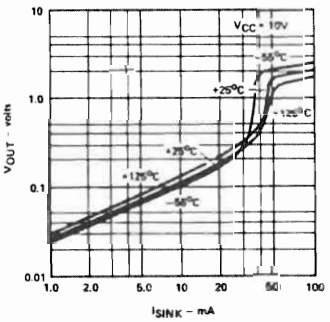
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



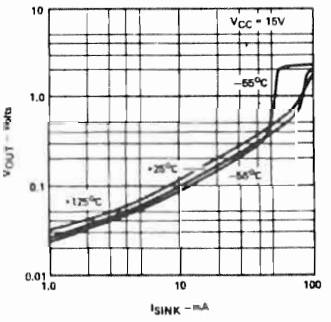
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



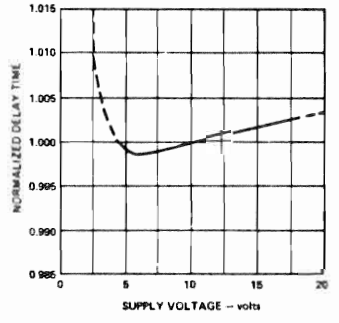
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



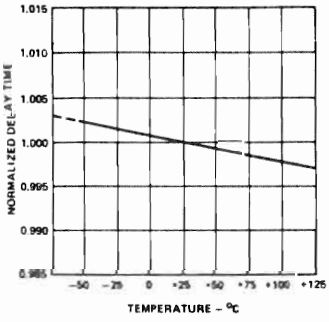
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



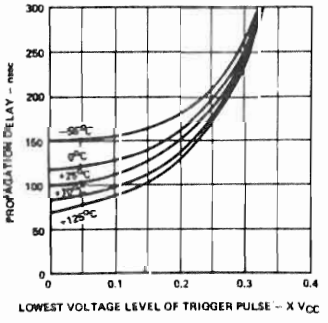
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

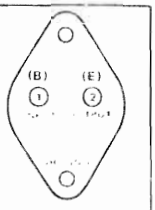
The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0 to 24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation – making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT[1] or TO-220)
  Or Hermetic TO-3 Type Metal Power Package (Case 11)

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



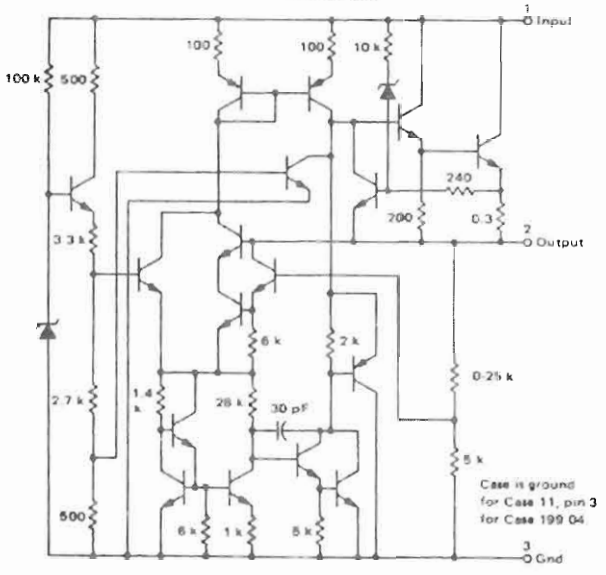


K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)

bottom view

Pins 1 and 2 electrically isolated from case
Case is third electrical connection

SCHEMATIC DIAGRAM



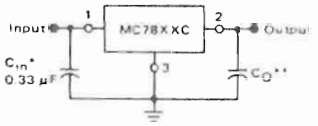
P SUFFIX
PLASTIC PACKAGE
CASE 199-04



Pin 1 Input (Base)
Pin 2 Output (Emitter)
Pin 3 Ground (Collector)

Heat sink surface connected to pin 3.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

See Packaging Information Section for outline dimensions.

[1]Trademark of Raoto Corporation of America

7805

442-54

ELECTRICAL CHARACTERISTICS (V_{IN} = 10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	50	mV
			8 V ≤ V_{IN} ≤ 12 V		1	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	50	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	25	mV
Output Voltage		8.0 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.65		5.35	V
Quiescent Current		T_J = 25°C			4.2	6.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Long Term Stability						20	mV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		68	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short Circuit Current		T_J = 25°C			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.1		mV/°C

7805C

ELECTRICAL CHARACTERISTICS (V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	100	mV
			8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.2	8.0	mA
Quiescent Current Change	with line	7 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Long Term Stability						20	mV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		62	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short Circuit Current		T_J = 25°C			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.1		mV/°C

NOTE 1: Thermal resistance of the packages (without a heat sink)

Junction to Case

TO-3 Package . . . . . 4°C/W
TO-220 Package . . . . . 2°C/W

Junction to Ambient

TO-3 Package . . . . . 35°C/W
TO-220 Package . . . . . 50°C/W

NOTE 2: Operating Ambient Temperature Range

7800 −55°C to +125°C
7800C 0°C to 85°C

MC7805
442-54

MC7805C ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc (T_J = +25°C, I_O = 500 mA) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{in}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	4.75	–	5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_B	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	750	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$	TCV_O	 –	 -1.0	 –	mV/°C

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

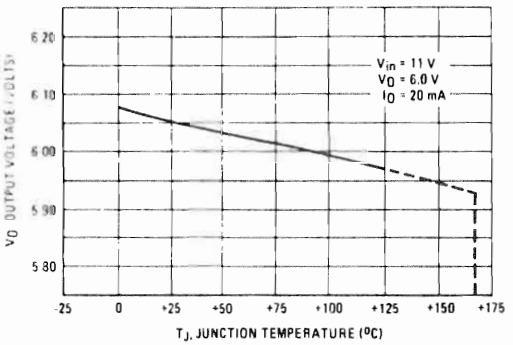


FIGURE 8 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

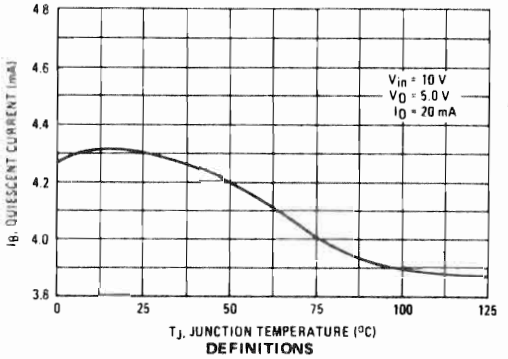
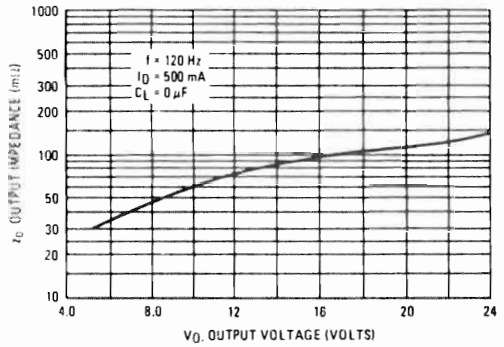


FIGURE 9 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (CASE 199-04)

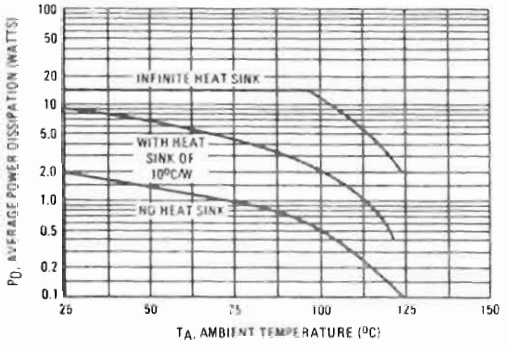


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 PACKAGE)

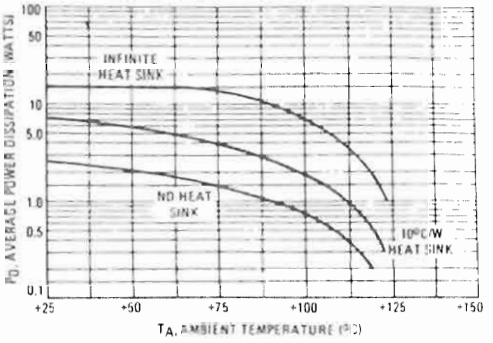


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE

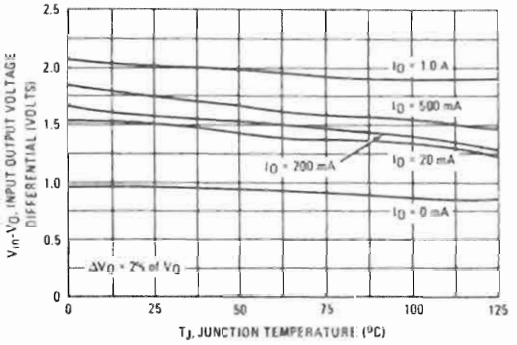


FIGURE 4 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

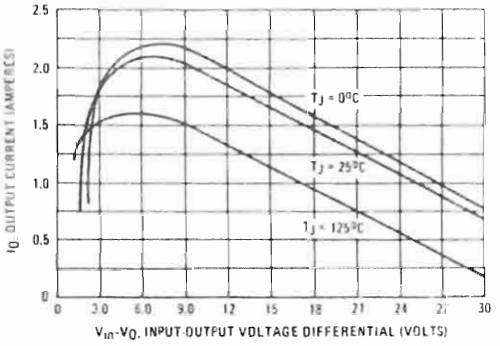


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

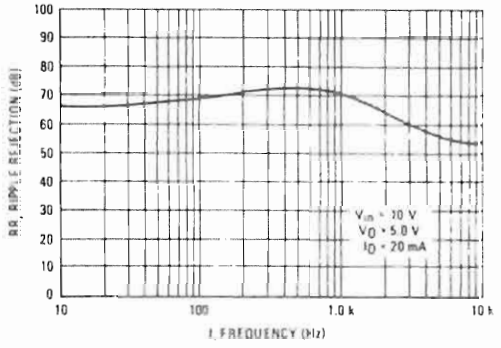
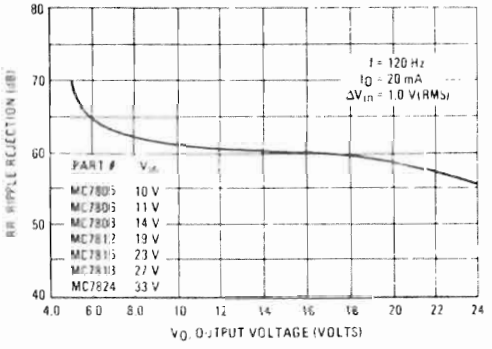


FIGURE 6 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



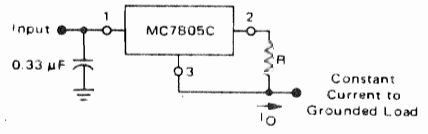
APPLICATIONS INFORMATION

Design Considerations

The MC7800C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. If an aluminum electrolytic capacitor is used, its value should be 10 μF or larger. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 10 – CURRENT REGULATOR



The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

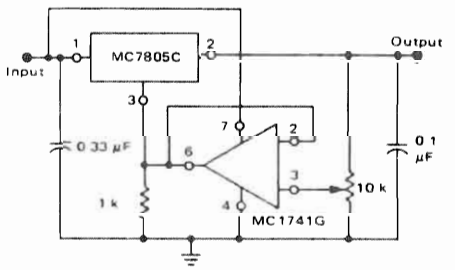
$$I_O = \frac{5\ V}{R} + I_Q$$

I_Q = 8.0 mA Max

ΔI_Q = 1.5 mA over line and load changes

For example, a 1 ampere current source would require R to be a 5 ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 11 – ADJUSTABLE OUTPUT REGULATOR

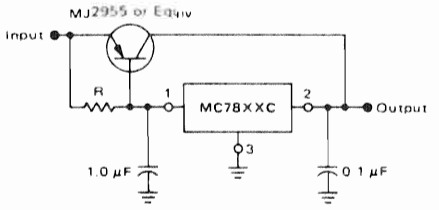


V_O = 7.0 V to 25 V

V_{IN} $V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

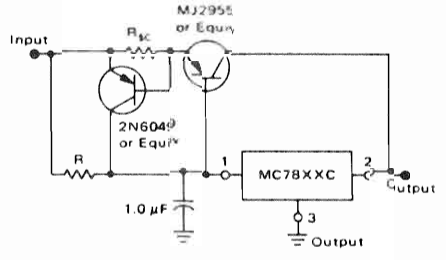
FIGURE 12 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 13 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 12 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, a four ampere plastic power transistor is specified.

#442-630

μA7905

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

GENERAL DESCRIPTION – The μA7900 series of monolithic 3-Terminal Negative Regulators is manufactured using the Fairchild Planar® epitaxial process. These negative regulators are intended as complements to the popular μA7800 series of positive voltage regulators, and they are available in the same voltage options from −5 to −24 V. The 7900s employ internal current limiting, safe-area protection, and thermal shutdown, making them virtually indestructible.

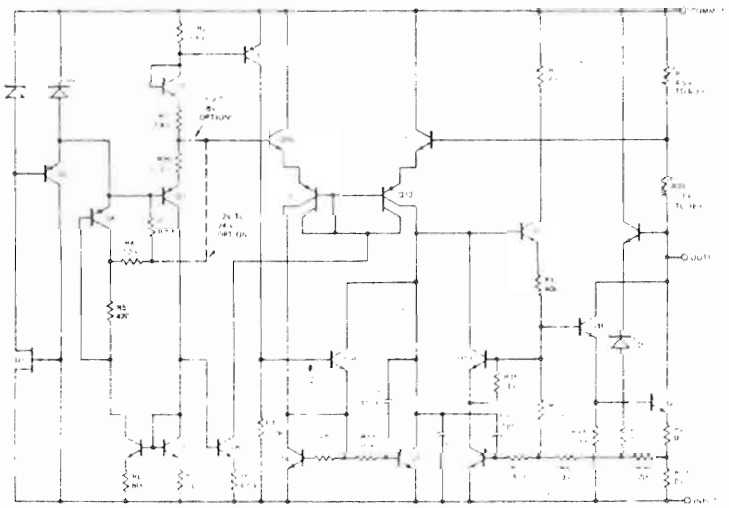
- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE AREA COMPENSATION**
- **AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE**
- **OUTPUT VOLTAGES ARE 5, 6, 8, 12, 15, 18 AND 24 V**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(5 V through 18 V)	−35 V
(24 V)	−40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-3 (Al or Steel)	−65°C to +150°C
TO-220	−55°C to +150°C
Operating Junction Temperature Range	
Military (μA7900)	−55°C to +150°C
Commercial (μA7900C)	0°C to +150°C
Lead Temperature	
TO-3 (Soldering, 60 s)	300°C
TO-220 (Soldering, 10 s)	230°C

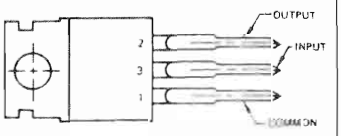
NOTE: The convention for Negative Regulators is the Algebraic value, thus −15 is less than −10 V.

EQUIVALENT CIRCUIT



Resistor values in Ω unless otherwise noted.

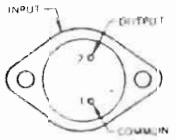
CONNECTION DIAGRAMS
TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
−5 V	μA7905C	μA7905UC
−6 V	μA7906C	μA7906UC
−8 V	μA7908C	μA7908UC
−12 V	μA7912C	μA7912UC
−15 V	μA7915C	μA7915UC
−18 V	μA7918C	μA7918UC
−24 V	μA7924C	μA7924UC

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
−5 V	μA7905	μA7905KM
−6 V	μA7906	μA7906KM
−8 V	μA7908	μA7908KM
−12 V	μA7912	μA7912KM
−15 V	μA7915	μA7915KM
−18 V	μA7918	μA7918KM
−24 V	μA7924	μA7924KM
−5 V	μA7905C	μA7905KC
−6 V	μA7906C	μA7906KC
−8 V	μA7908C	μA7908KC
−12 V	μA7912C	μA7912KC
−15 V	μA7915C	μA7915KC
−18 V	μA7918C	μA7918KC
−24 V	μA7924C	μA7924KC

#442-630
μA7905 (cont)

μA7905

ELECTRICAL CHARACTERISTICS (V_{IN} = −10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−4.8	−5.0	−5.2	V
Line Regulation		T_J = 25°C	−7 V ≤ V_{IN} ≤ −25 V		3	50	mV
			−8 V ≤ V_{IN} ≤ −12 V		1	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	50	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	25	mV
Output Voltage		−8.0 V ≤ V_{IN} ≤ −20 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−4.70		−5.30	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−8 V ≤ V_{IN} ≤ −25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		f = 120 Hz, −8 V ≤ V_{IN} ≤ −18 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.4		mV/°C

μA7905C

ELECTRICAL CHARACTERISTICS (V_{IN} = −10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−4.8	−5.0	−5.2	V
Line Regulation		T_J = 25°C	−7 V ≤ V_{IN} ≤ −25 V		3.0	100	mV
			−8 V ≤ V_{IN} ≤ −12 V		1.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5.0	50	mV
Output Voltage		−7 V ≤ V_{IN} ≤ −20 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−4.75		−5.25	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−7 V ≤ V_{IN} ≤ −25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		f = 120 Hz, −8 V ≤ V_{IN} ≤ −18 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.4		mV/°C

#442-630
μA7905 (cont)

The μA7900 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 7900, 125°C for 7900C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JC}	MAX θ_{JA}
TO-3	3.5°C/W	5.5°C/W	40°C/W	45°C/W
TO-220	3.0°C/W	5.0°C/W	60°C/W	65°C/W

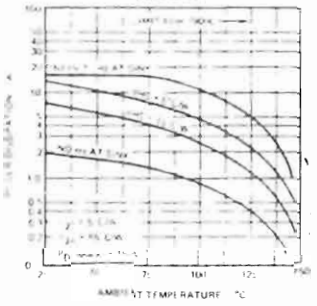
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)}\ T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

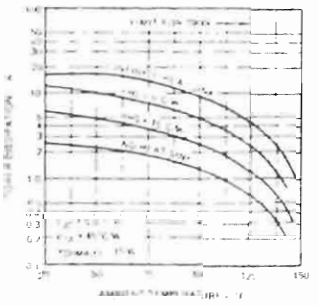
Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
θ_{CA} = Case to Ambient Thermal Resistance
θ_{CS} = Case to Heat Sink Resistance
θ_{SA} = Heat Sink to Ambient Thermal Resistance

WORST CASE POWER DISSIPATION
AS A FUNCTION OF
AMBIENT TEMPERATURE
(TO-220)



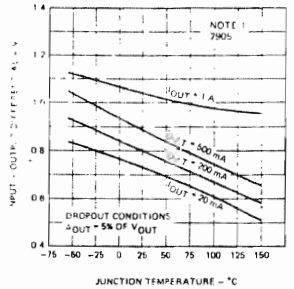
WORST CASE POWER DISSIPATION
AS A FUNCTION OF
AMBIENT TEMPERATURE
(TO-3)



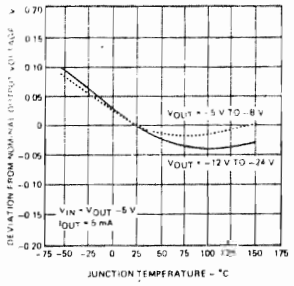
#442-630

μA7905 (cont)

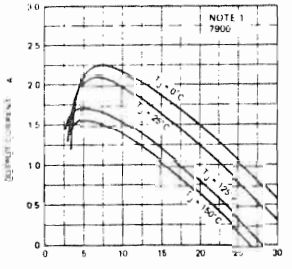
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



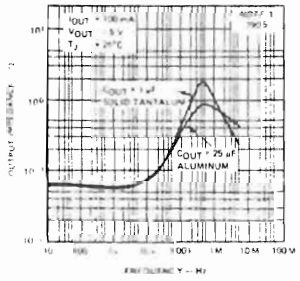
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



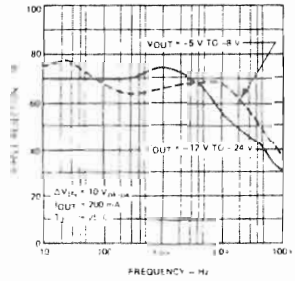
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



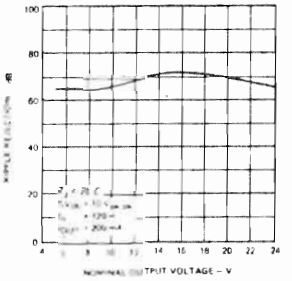
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



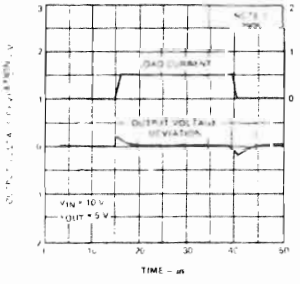
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



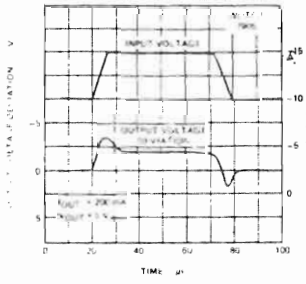
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



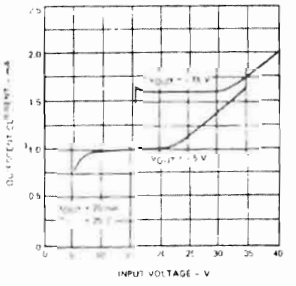
LOAD TRANSIENT RESPONSE



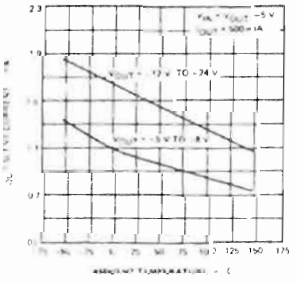
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



NOTE 1: The other μA7900 series devices have similar performance curves.

#442-663

μA78M12

3-TERMINAL POSITIVE VOLTAGE REGULATORS

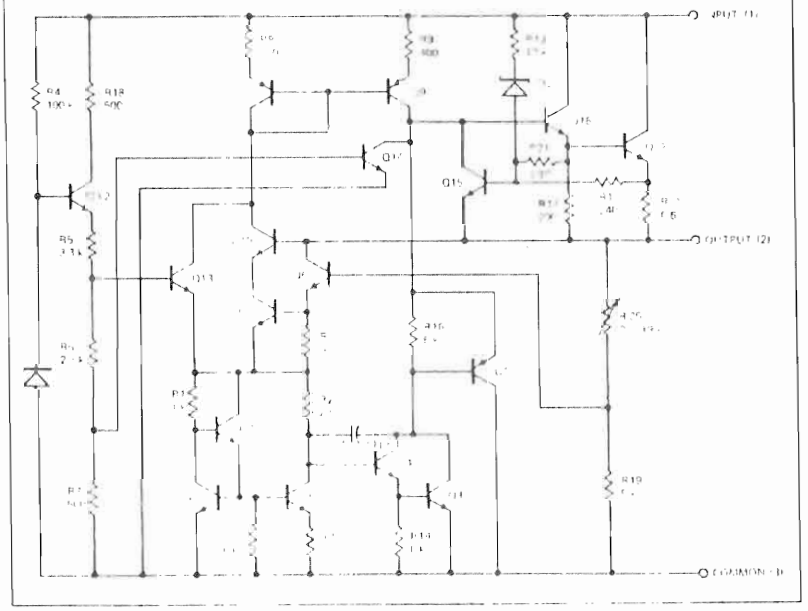
GENERAL DESCRIPTION – The μA78M00 series of 3-Terminal Medium Current Positive Voltage Regulators is constructed using the Fairchild Planar™ epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver in excess of 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- OUTPUT CURRENT IN EXCESS OF 0.5 A
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE AREA COMPENSATION
- AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES
- OUTPUT VOLTAGES OF 5 V, 6 V, 8 V, 12 V, 15 V, 20 V AND 24 V
- MILITARY AND COMMERCIAL TEMPERATURE RANGE

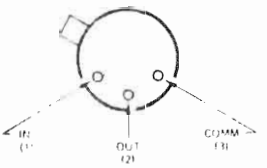
ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(5 V through 15 V)	35 V
(20 V, 24 V)	40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-39	−65°C to +150°C
TO-220	−55°C to +150°C
Operating Junction Temperature Range	
μA78M00	−55°C to +150°C
μA78M00C	0°C to +150°C
Lead Temperatures (Soldering, 60 s time limit) TO-39	300°C
(Soldering, 10 s time limit) TO-220	230°C

EQUIVALENT CIRCUIT



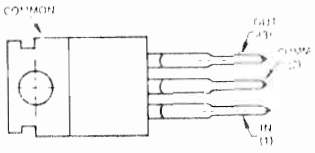
CONNECTION DIAGRAM
TO-39 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE BF
PACKAGE CODE H



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA78M05	μA78M05HM
6 V	μA78M06	μA78M06HM
8 V	μA78M08	μA78M08HM
12 V	μA78M12	μA78M12HM
15 V	μA78M15	μA78M15HM
20 V	μA78M20	μA78M20HM
24 V	μA78M24	μA78M24HM
5 V	μA78M05C	μA78M05HC
6 V	μA78M06C	μA78M06HC
8 V	μA78M08C	μA78M08HC
12 V	μA78M12C	μA78M12HC
15 V	μA78M15C	μA78M15HC
20 V	μA78M20C	μA78M20HC
24 V	μA78M24C	μA78M24HC

TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA78M05C	μA78M05UC
6 V	μA78M06C	μA78M06UC
8 V	μA78M08C	μA78M08UC
12 V	μA78M12C	μA78M12UC
15 V	μA78M15C	μA78M15UC
20 V	μA78M20C	μA78M20UC
24 V	μA78M24C	μA78M24UC

#442-663
μA78M12 (cont)

μA78M12

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	60	mV
			16 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		2.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	120	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	60	mV
Output Voltage		15.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	15 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M12C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	100	mV
			16 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		2.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	240	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	120	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

#442-663
µA78M12 (cont)

DESIGN CONSIDERATIONS

The µA78M00 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 78M00, 125°C for 78M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JA}	MAX θ_{JA}
TO-39	18	25	120	185
TO 220	3	5	62	70

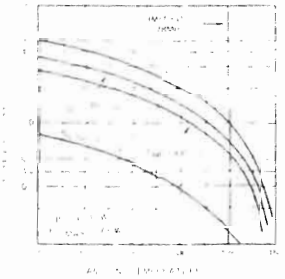
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

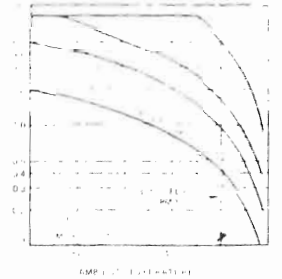
Solving for T_J: $T_J = T_A + P_D(\theta_{JC}+\theta_{CA})$ or $T_A = P_D \theta_{JA}$ (Without a heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to Case thermal resistance
θ_{CA} = Case to Ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to Ambient thermal resistance

WORST CASE POWER DISSIPATION
VERSUS AMBIENT TEMPERATURE
TO 39



WORST CASE POWER DISSIPATION
VERSUS AMBIENT TEMPERATURE
TO 220

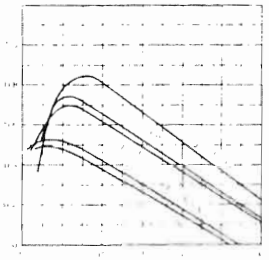


#442-663

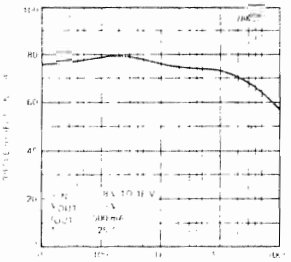
μA78M12 (cont)

ELECTRICAL PERFORMANCE CURVES

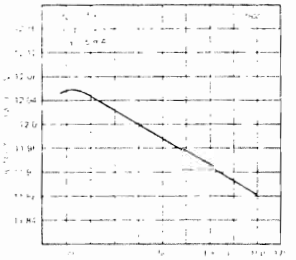
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT OUTPUT DIFFERENTIAL VOLTAGE



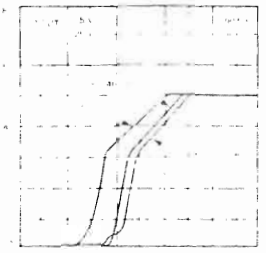
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



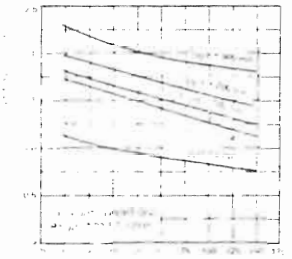
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



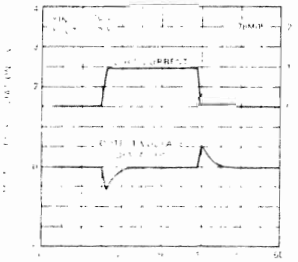
DROPOUT CHARACTERISTICS



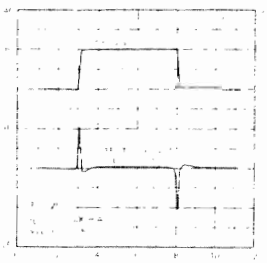
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



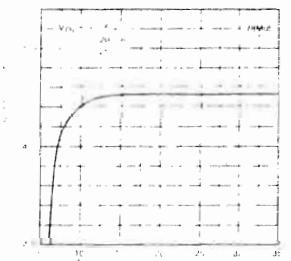
LOAD TRANSIENT RESPONSE



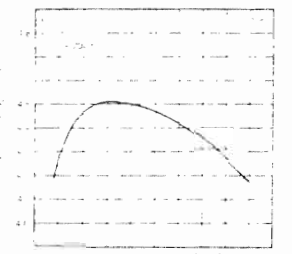
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

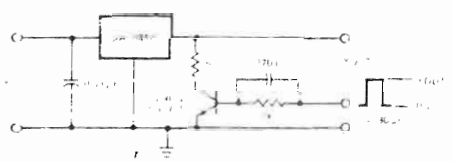


QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

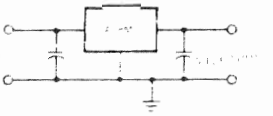


NOTE: Other μA78M00 Series devices have similar curves

TEST CIRCUITS



LOAD REGULATION TEST CIRCUIT



DC PARAMETER TEST CIRCUIT

#442-664

79M12

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

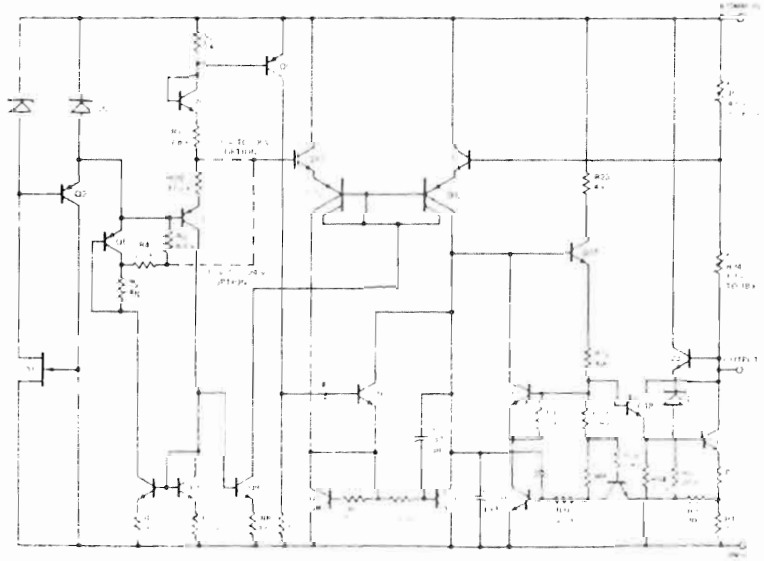
GENERAL DESCRIPTION – The μA79M00 series of 3-Terminal Medium Current Negative Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- OUTPUT CURRENT IN EXCESS OF 0.5 A
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE AREA COMPENSATION
- AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES
- OUTPUT VOLTAGES OF –5 V, –6 V, –8 V, –12 V, –15 V, –20 V AND –24 V

ABSOLUTE MAXIMUM RATINGS

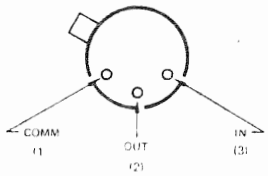
Input Voltage		
(–5 V through –15 V)		–35 V
(–20 V, –24 V)		–40 V
Internal Power Dissipation		Internally Limited
Storage Temperature Range		
TO-39		–65°C to +150°C
TO-220		–55°C to +125°C
Operating Junction Temperature Range		
TO-39	Military (μA79M00)	–55°C to +150°C
	Commercial (μA79M00C)	0°C to +150°C
TO-220	Commercial (μA79M00C)	0°C to +150°C
Lead Temperature (Soldering, 60 s) TO-39		300°C
(Soldering, 10 s) TO-220		230°C

EQUIVALENT CIRCUIT



Resistor values in kΩ unless otherwise noted

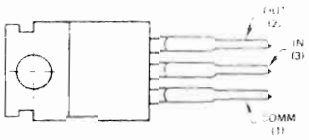
CONNECTION DIAGRAMS
TO-39 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE BF
PACKAGE CODE H



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.	PART NO.
–5 V	μA 79M05HM	μA 79M05AHC
–6 V	μA 79M06HM	μA 79M06AHC
–8 V	μA 79M08HM	μA 79M08AHC
–12 V	μA 79M12HM	μA 79M12AHC
–15 V	μA 79M15HM	μA 79M15AHC
–20 V	μA 79M20HM	μA 79M20AHC
–24 V	μA 79M24HM	μA 79M24AHC

TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
–5 V	μA 79M05AUC
–6 V	μA 79M06AUC
–8 V	μA 79M08AUC
–12 V	μA 79M12AUC
–15 V	μA 79M15AUC
–20 V	μA 79M20AUC
–24 V	μA 79M24AUC

NOTE
Product previously specified as HC or UC has been deleted

#442-664
79M12 (cont)

μA79M12HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −19 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−12.5	−12	−11.5	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −14.5 V		9.0	80	mV
			−25 V ≤ V_{IN} ≤ −15 V		5.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −14.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−12.6		−11.4	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −14.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		−25 V ≤ V_{IN} ≤ −15 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.8		mV/°C

μA79M12AHC AND μA79M12AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −19 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−12.5	−12	−11.5	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −14.5 V		9.0	80	mV
			−25 V ≤ V_{IN} ≤ −15 V		5.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −14.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−12.6		−11.4	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −14.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		−25 V ≤ V_{IN} ≤ −15 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.8		mV/°C

*P_D ≤ 4 W

#442-664
79M12 (cont)

DESIGN CONSIDERATIONS

The μA79M00 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 79M00, 125°C for 79M00AC and 79M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	TYP	MAX	TYP	MAX
PACKAGE	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
TO-39	18.0	25	120	185
TO-220	3.0	5.0	62	70

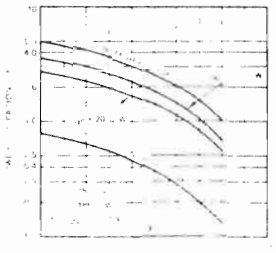
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$\theta_{CA} \quad \theta_{CS} + \theta_{SA}$

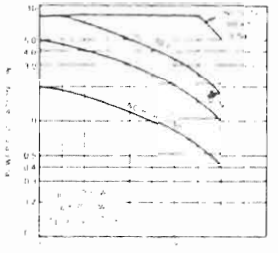
Solving for T_J: $T_J = T_A + P_D(\theta_{JC}+\theta_{CA})$ or $T_A + P_D\,\theta_{JA}$ (Without a heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to ambient thermal resistance

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-39



WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-220

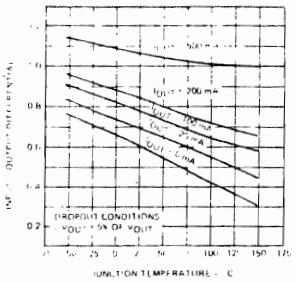


#442-664

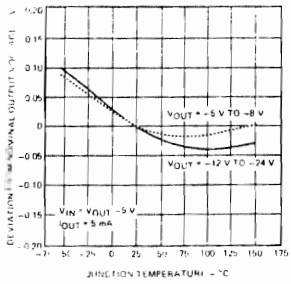
79M12 (cont)

TYPICAL PERFORMANCE CURVES

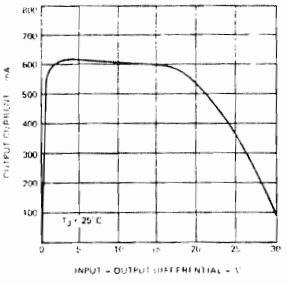
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



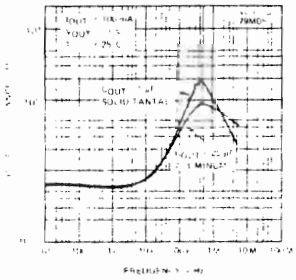
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



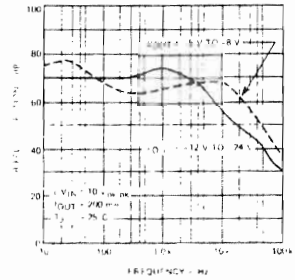
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



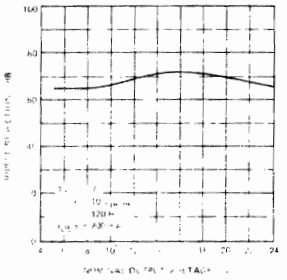
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



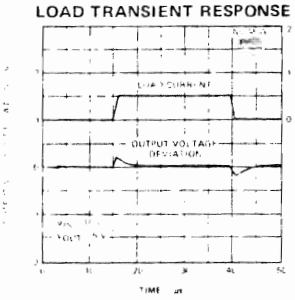
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



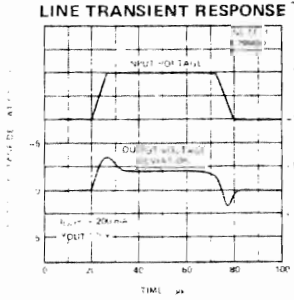
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



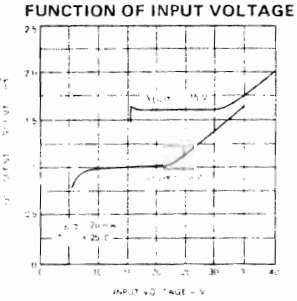
LOAD TRANSIENT RESPONSE



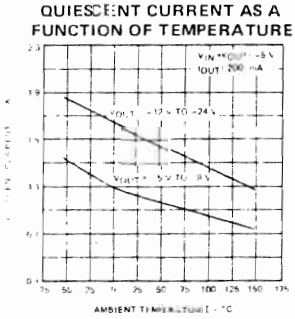
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



NOTE 3: The other µA79M00 voltage series devices have similar performance curves.

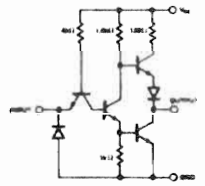
443-18
7404

HEX INVERTER | S5404 N7404

S5404–A,F,W • N7404–A,F

DIGITAL 54/74 TTL SERIES

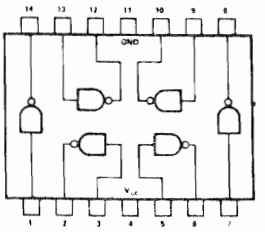
SCHEMATIC (each inverter)



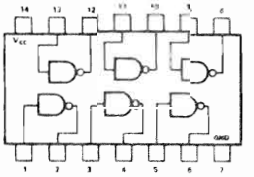
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5404 Circuits	4.5	5	5.5	V
N7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A: S5404 Circuits	-55	25	125	°C
N7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current	V_{CC} = MAX		S5404	-20		-55	mA
				N7404	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		6	12	mA

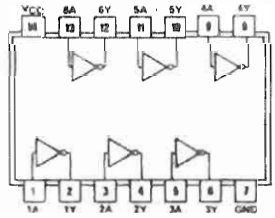
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

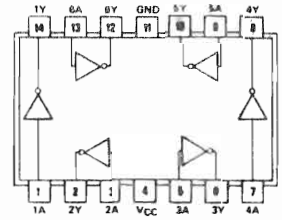
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

HEX INVERTERS

positive logic:
$Y = \overline{A}$



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			400			1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.7			0.8	V
				74 Family			0.8			0.8			0.7			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §*				−1.5			−1.5						1.5			1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V, LS30												−0.4				
				V_{IL} = 0.4 V, Others			−1.6			−2						−0.36				
				V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current¶	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−3		−15	6		−40	−40		−100	mA
				74 Family	−18		−55	−40		−100	−3		−15	5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
¶Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts date-coded 7332 or higher.

MOS RAMs

MM2112, MM2112-2 1024-bit (256 × 4) static MOS RAM with common data I/O

general description

The National MM2112 is a 256 by 4 static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

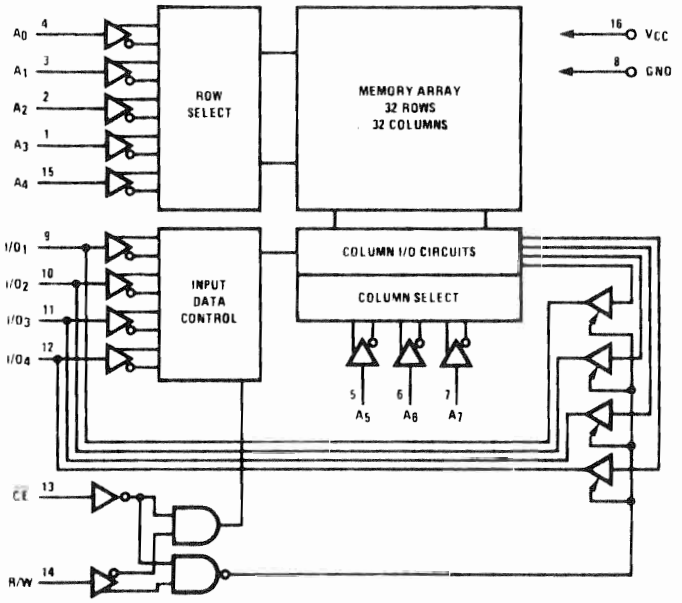
The MM2112 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The Chip-enable allows easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

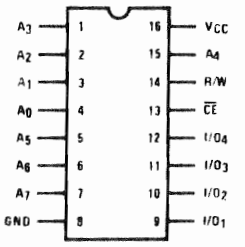
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 0.65 to 1 μs Max.
- Simple Memory Expansion – Chip Enable Input
- Low Cost Packaging – 16 Pin Epoxy B Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Tri-State ® Output – OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0 A_7	ADDRESS INPUTS
R/W	READ WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1 I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2112D or MM2112-2D
See Package 3

Order Number MM2112N or MM2112-2N
See Package 15

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics

T_A = 0°C to +70°C, V_{CC} = 5 V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25 V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2 V, $V_{I/O}$ = 4.0 V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}$ = 2.2 V, $V_{I/O}$ = 0.45 V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25 V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25 V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

Note 1: Typical values are for T_A = 25°C and nominal supply voltage.

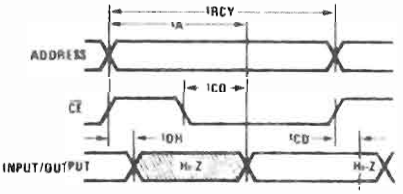
capacitance

T_A = 25°C, f = 1 MHz

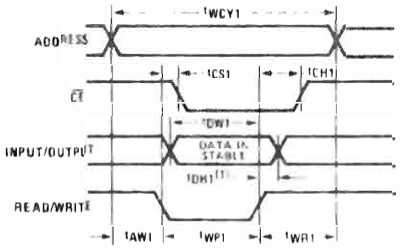
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0 V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0 V	10	18

switching time waveforms

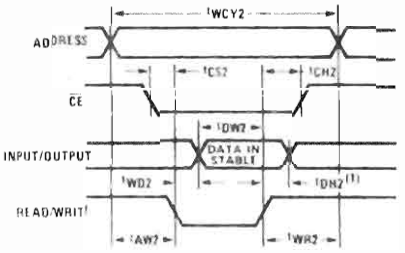
READ CYCLE (R/W = "1")



WRITE CYCLE #1



WRITE CYCLE #2



Note 1: Data Hold Time (t_{DH}) is referenced to the trailing edge of CHIP ENABLE ($\overline{CE}$) or READ/WRITE (R/W) whichever comes first.

ac electrical characteristics T_A = 0°C to +70°C, V_{CC} = 5 V ± 5% unless otherwise specified.

MM2112

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			1,000	ns	Input Pulse Rise and Fall Times: 20 ns
t_{CO}	Chip Enable to Output Time			800	ns	Timing Measurement Reference Level: 1.5 V
t_{CD}	Chip Enable to Output Disable Time	0		200	ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{OH}	Previous Read Data Valid After Change of Address	50			ns	
WRITE CYCLE #1						
t_{WCY1}	Write Cycle	850			ns	
t_{AW1}	Address to Write Setup Time	150			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW1}	Write Setup Time	650			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WP1}	Write Pulse Width	650			ns	Timing Measurement Reference Level: 1.5 V
t_{CS1}	Chip Enable Setup Time	0		100	ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	100			ns	
WRITE CYCLE #2						
t_{WCY2}	Write Cycle	1,050			ns	
t_{AW2}	Address to Write Setup Time	150			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW2}	Write Setup Time	650			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WD2}	Write to Output Disable Time	200			ns	Timing Measurement Reference Level: 1.5 V
t_{CS2}	Chip Enable Setup Time	0			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	100			ns	

MM2112-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			650	ns	Input Pulse Rise and Fall Times: 20 ns
t_{CO}	Chip Enable to Output Time			500	ns	Timing Measurement Reference Level: 1.5 V
t_{CD}	Chip Enable to Output Disable Time	0		150	ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{OH}	Previous Read Data Valid After Change of Address	50			ns	
WRITE CYCLE #1						
t_{WCY1}	Write Cycle	500			ns	
t_{AW1}	Address to Write Setup Time	100			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW1}	Write Setup Time	350			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WO1}	Write Pulse Width	350			ns	Timing Measurement Reference Level: 1.5 V
t_{CS1}	Chip Enable Setup Time	0		50	ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	50			ns	
WRITE CYCLE #2						
t_{WCY2}	Write Cycle	700			ns	
t_{AW2}	Address to Write Setup Time	100			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW2}	Write Setup Time	350			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WD2}	Write to Output Disable Time	200			ns	Timing Measurement Reference Level: 1.5 V
t_{CS2}	Chip Enable Setup Time	0			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	50			ns	

443-727

LPTTL/MONOSTABLE 96L02

LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 96L02 is a low power Dual Retriggerable, Resettable Monostable Multivibrator which provides andoutput pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

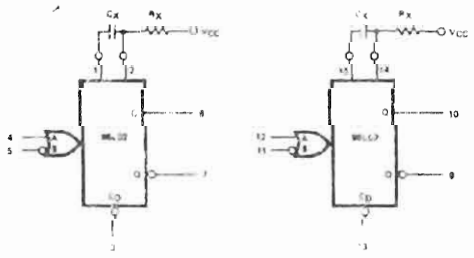
- TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT
- 50 ns TYPICAL PROPAGATION DELAY
- RETRIGGERABLE 0 TO 100 % DUTY CYCLE
- TTL INPUT GATING – LEADING OR TRAILING EDGE-TRIGGERING
- COMPLEMENTARY TTL OUTPUTS
- OPTIONAL RETRIGGER LOCK-OUT CAPABILITY
- PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS
- RESETTABLE

PIN NAMES

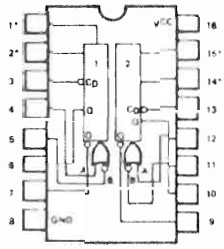
		LOADING HIGH	LOADING LOW
B	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
$\overline{C}_D$	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
$\overline{Q}$	Output (Active LOW)	9.0	3.0

1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

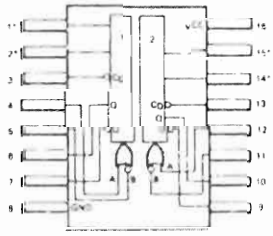


CONNECTION DIAGRAM DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)



*Pins for external timing.

FUNCTIONAL DESCRIPTION – The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset lead to a logic LOW. Active pull ups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active LOW input or the Q output to the active HIGH input.

OPERATION RULES

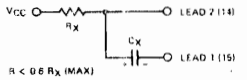
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Symbol.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for −55 to 125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse width (t) is defined as follows:

$$t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right] \text{ (for } C_X > 10^3 \text{ pF)}$$

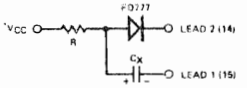
Where R_X is in kΩ, C_X is in pF, t is in ns. For $C_X < 10^3$ pF, see Fig. 1

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

   A. Use with low leakage capacitors.
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 μA, and the inverse capacitor leakage at 1.0 V is less than 1.6 μA over the operational temperature range and Rule 3 above is satisfied.

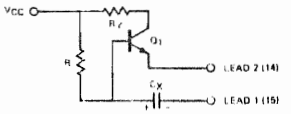


   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



$$t \approx 0.3\ RC_X$$

   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



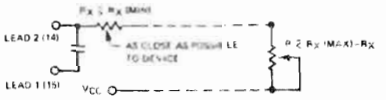
$R < R_X\,(0.7)\,(h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
R_X (min) $< R_Y < R_X$ (max)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\ RC_X$$

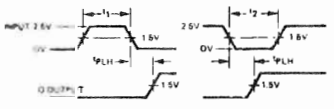
This configuration is not recommended with retriggerable operation.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

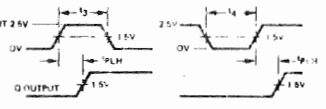


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pick up.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

Input to Lead 5 (11)
Lead 4 (12) = LOW
Lead 3 (13) = HIGH
t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
t_2, t_4 = Min. Negative Input Pulse Width > 60 ns



Input to Lead 4 (12)
Lead 5 (11) = HIGH
Lead 3 (13) = HIGH



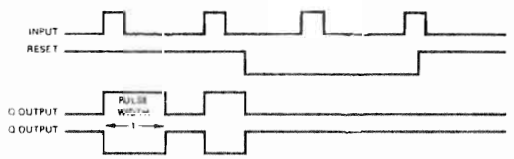
9. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.33\ R_X C_X \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t.
Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation – An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interfliction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC}
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
96L02XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 4)	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	V	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	V	V_{CC} = MIN, I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.3 V
I_{SC} I_{OS}	Output Short Circuit Current (Note 5)	−2.0		−13	mA	V_{CC} = MAX, V_{OUT} = 1.0 V
I_{CC}	Supply Current		10	16	mA	V_{CC} = MAX

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
96L02XM						
t_{PLH}	Turn Off Delay, Negative Trigger Input to True Output		55	75	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Turn On Delay, Negative Trigger Input to Complement Output		45	62	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	μs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	$R_X = 39$ kΩ, $C_X = 1000$ pF
96L02XC						
t_{PLH}	Turn Off Delay, Negative Trigger Input to True Output		55	80	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Turn On Delay, Negative Trigger Input to Complement Output		45	65	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	μs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	$R_X = 39$ kΩ, $C_X = 1000$ pF

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X (C_X < 1000 pF)
(FOR C_X > 1000 pF SEE OPERATION RULES 4 AND 5.)

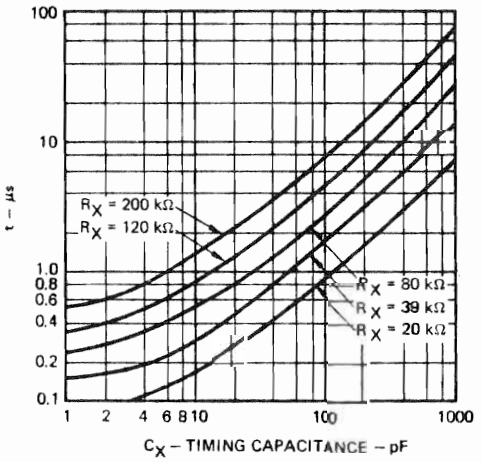
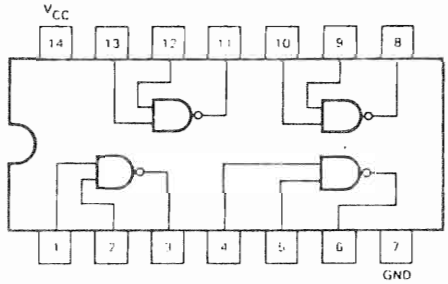


Fig. 1

#443-728

FAIRCHILD • 9LS00 (54LS/74LS00)

QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS00XM / 54LS00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS00XC / 74LS00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type: F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

signetics

DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

S5492 N7492

S5492–A,F,W • N7492–A,F

443-34

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5492/N7492 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

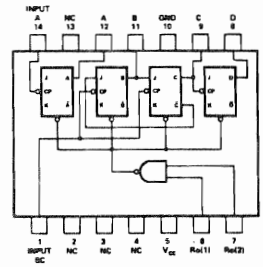
1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

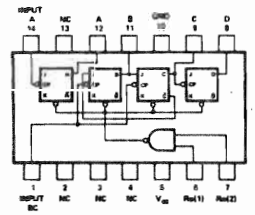
The S5492/N7492 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 155mW.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



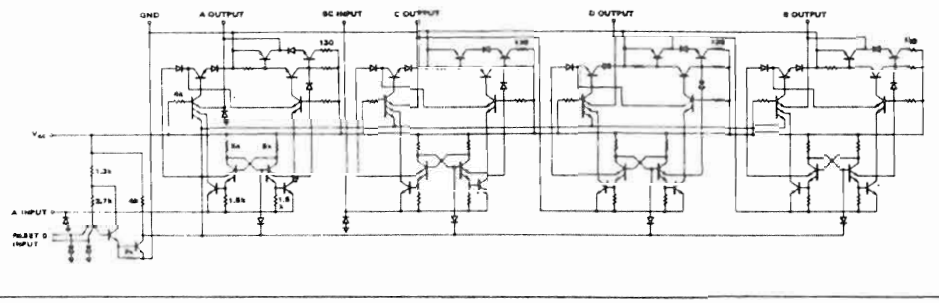
TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5492 Circuits		4.5	5	5.5	V
N7492 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5492 Circuits	-55	25	125	°C
	N7492 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	V_{CC} = MAX,	V_{in} = 2.4V				160	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	V_{CC} = MAX,	V_{ir} = 0.4V				-6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5492	-20		-57	mA
				N7492	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5492		31	44	mA
				N7492		31	51	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

#443-731
AND
#443-733

9LS290 (54LS/74LS290)
DECADE COUNTER
9LS293 (54LS/74LS293)
4-BIT BINARY COUNTER

DESCRIPTION — The 9LS290 (54LS/74LS290) and 9LS293 (54LS/74LS293) are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (9LS290) or divide-by-eight (9LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the 9LS290 also has a 2-input gated Master Set (Preset 9).

- CORNER POWER PIN VERSIONS OF THE 9LS90 and 9LS93
- LOW POWER CONSUMPTION . . . . TYPICALLY 45 mW
- HIGH COUNT RATES . . . . TYPICALLY 50 MHz
- CHOICE OF COUNTING MODES . . . . BCD, BI-QUINARY, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

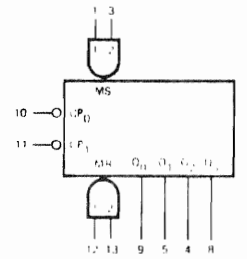
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷ 2 Section.	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 5 Section (9LS290).	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 8 Section (9LS293).	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, 9LS290) Inputs	0.5 U.L.	0.25 U.L.
O_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. The O_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

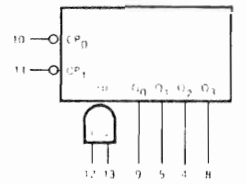
LOGIC SYMBOL

9LS290



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

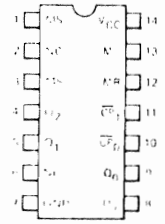
9LS293



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

CONNECTION DIAGRAM
DIP (TOP VIEW)

9LS290

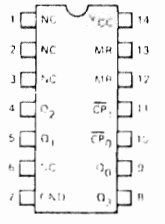


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC – No Internal Connection

CONNECTION DIAGRAM
DIP (TOP VIEW)

9LS293



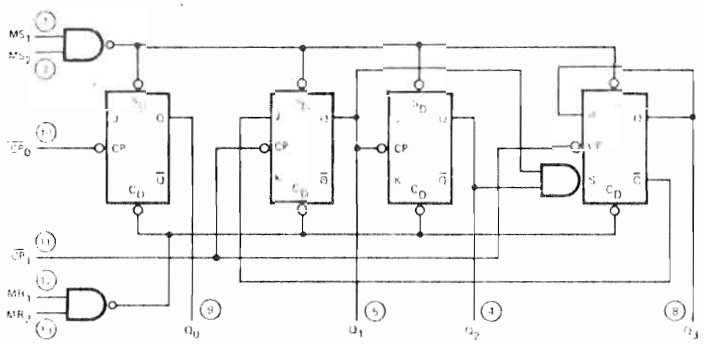
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC – No internal connection

FAIRCHILD • 9LS290 • 9LS293

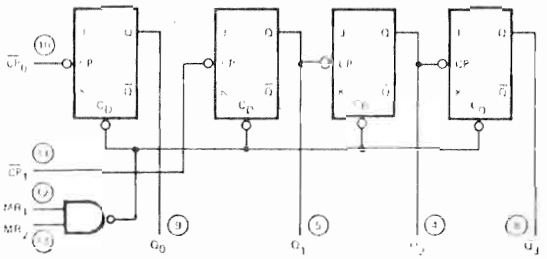
LOGIC DIAGRAMS

9LS290



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

9LS293



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

FUNCTIONAL DESCRIPTION – The 9LS290 and 9LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (9LS290) or divide-by-eight (9LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the 9LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

9LS290

A. BCD Decade (8421) Counter – the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

9LS293

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

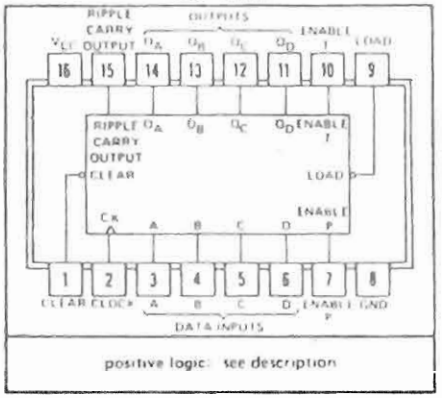
B. 3 Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS160 thru 'LS163	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160, 'LS162, and 'S162 are decade counters and the '161, '163, 'LS161, 'LS163, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160 thru 'LS163, or 'S162 and 'S163. The clear function for the '160, '161, 'LS160, and 'LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162, 'LS163, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

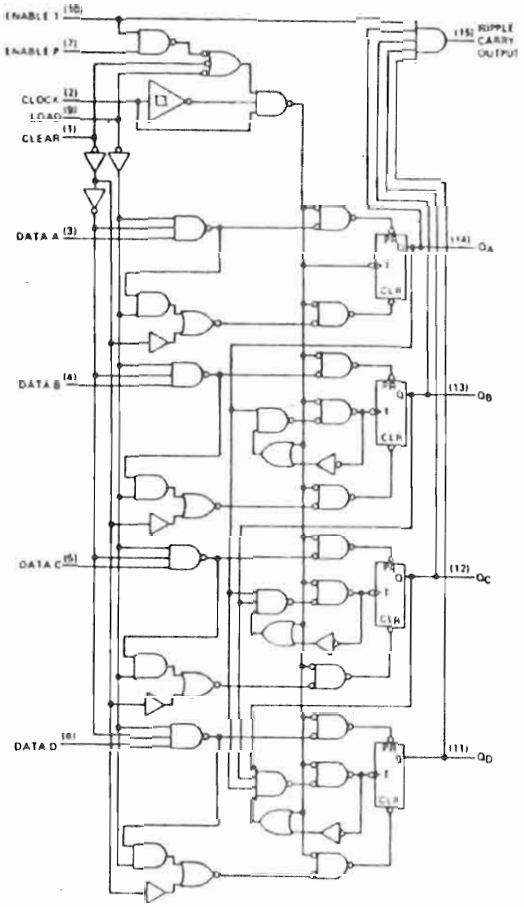
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160 thru 'LS163 or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160 thru 'LS163, 'S162 and 'S163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, Series 74LS, and Series 74S circuits are characterized for operation from 0°C to 70°C.

SN54LS163, SN74LS163 SYNCHRONOUS BINARY COUNTERS

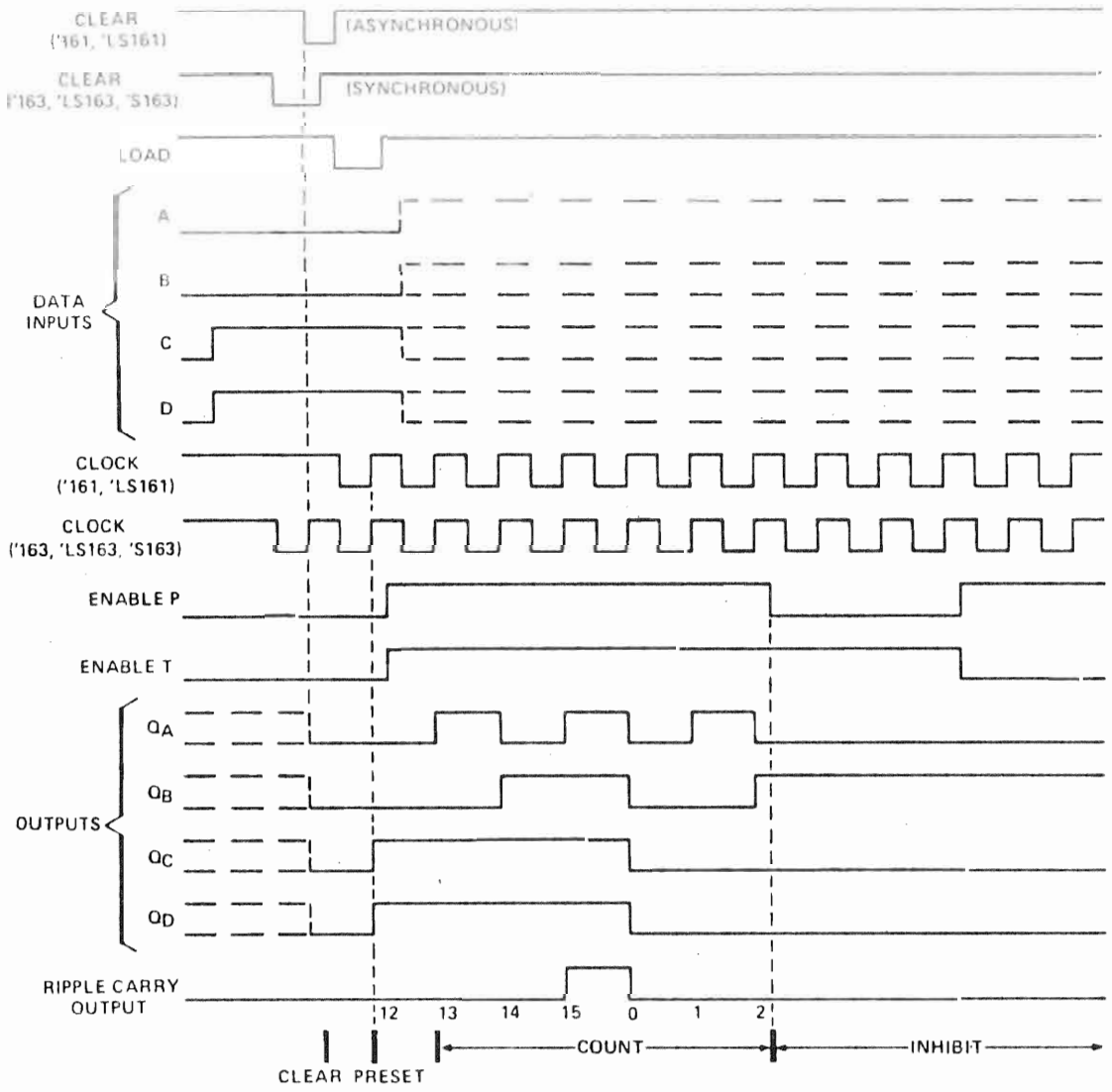
SN54LS161, SN74LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160, SN74LS160 decade counters at left.



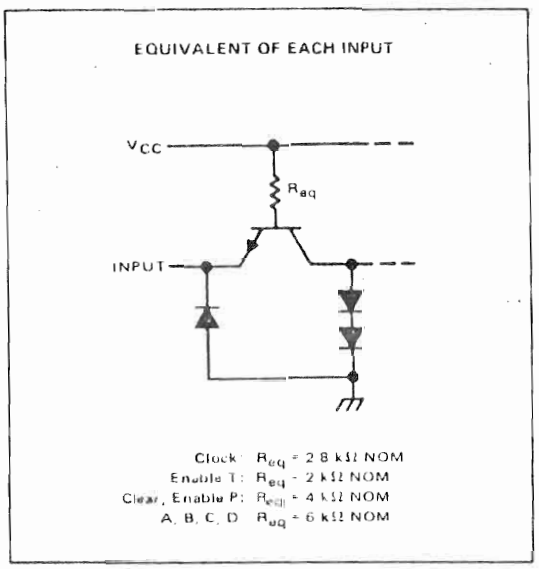
typical clear, preset, count, and inhibit sequences

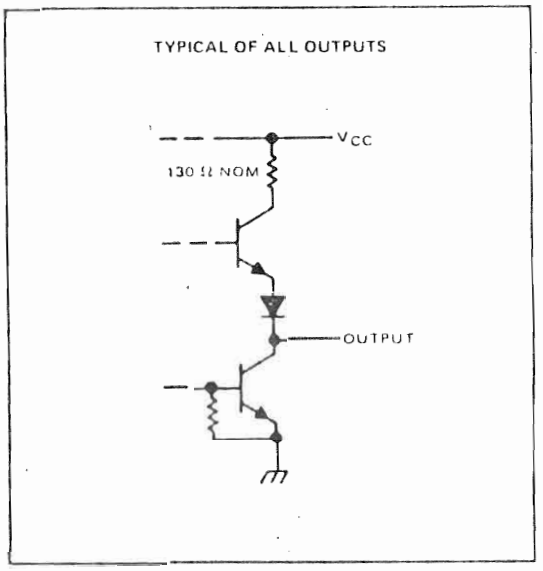
Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (*see* Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

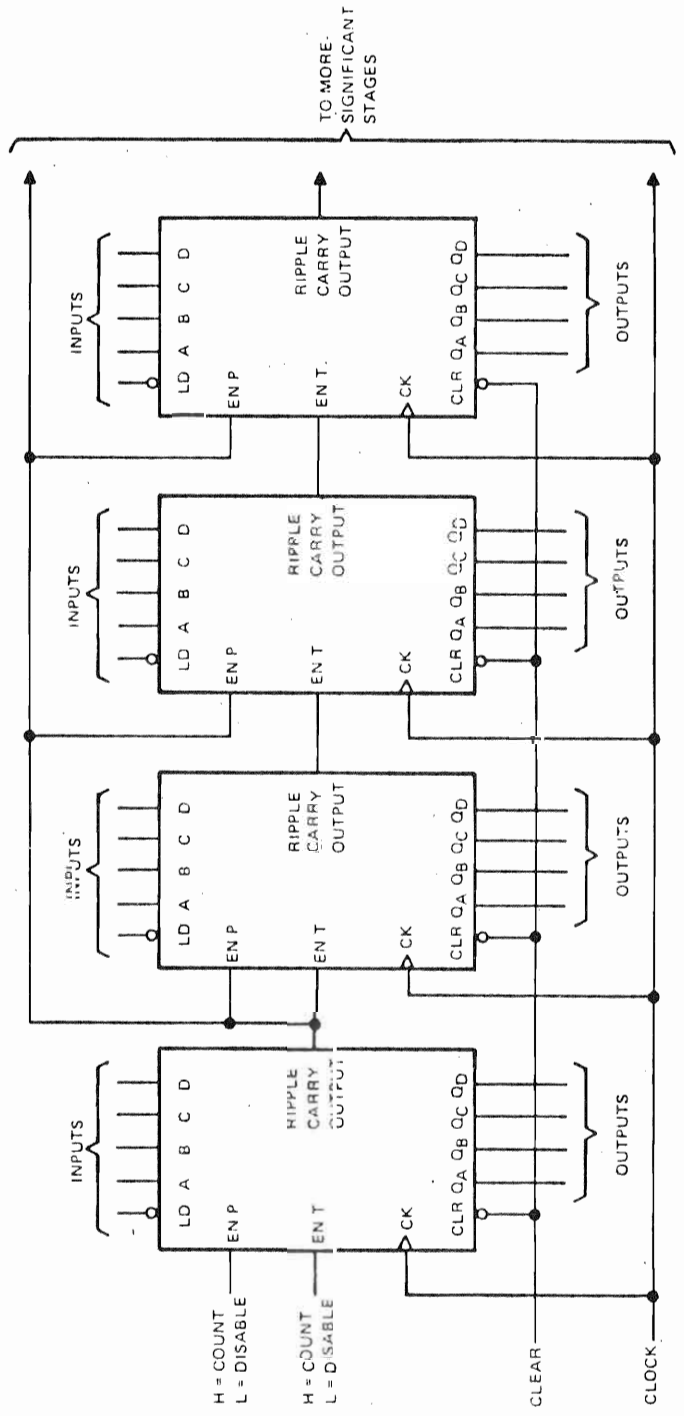
		SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	Enable P	20			20			
	Load	25			25			
	Clear[1]	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

[1] This applies only for '162 and '163, which have synchronous clear inputs.

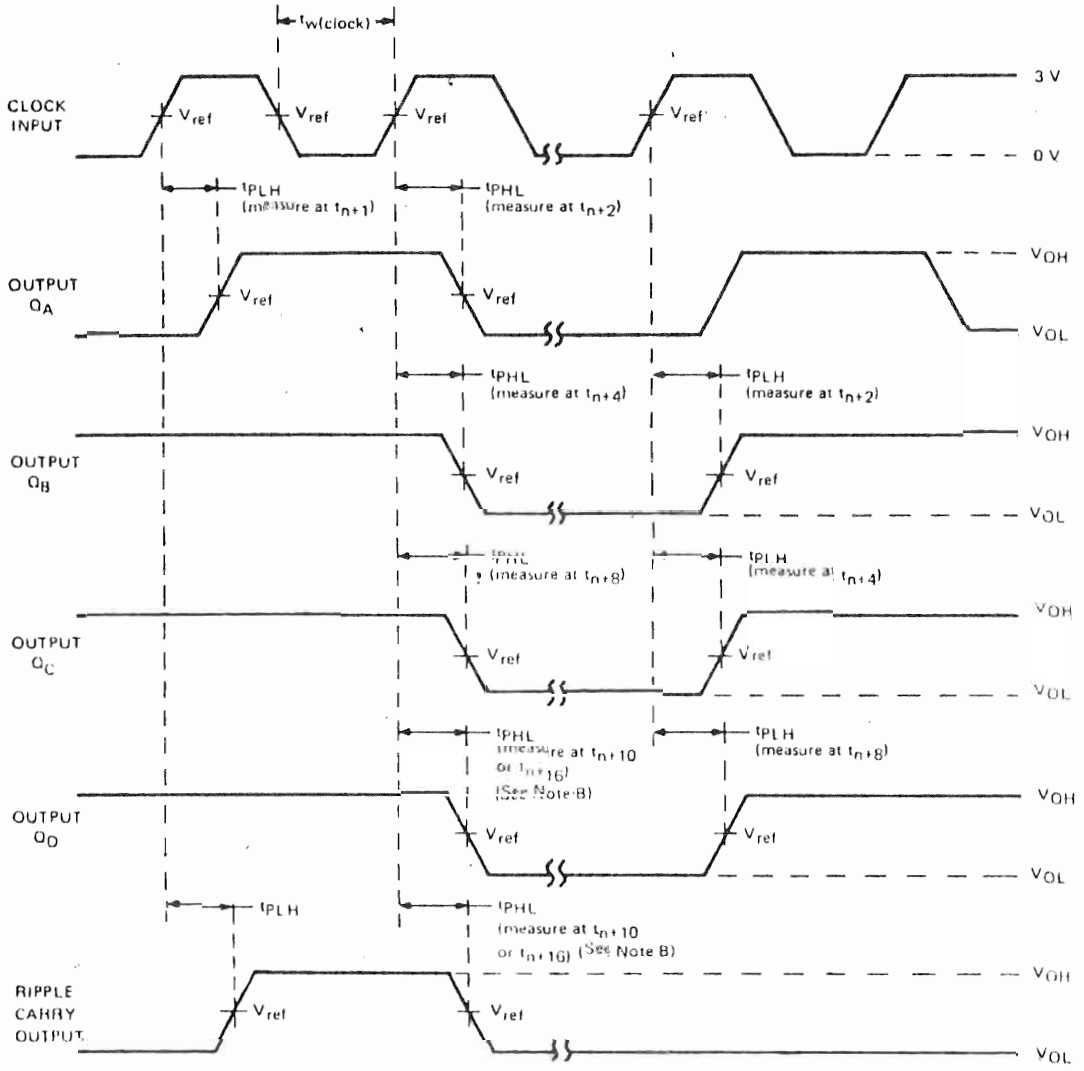
TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160, 'LS162, or 'S162 will count in BCD and the '161, '163, 'LS161, 'LS163, or 'S163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



PARAMETER MEASUREMENT INFORMATION



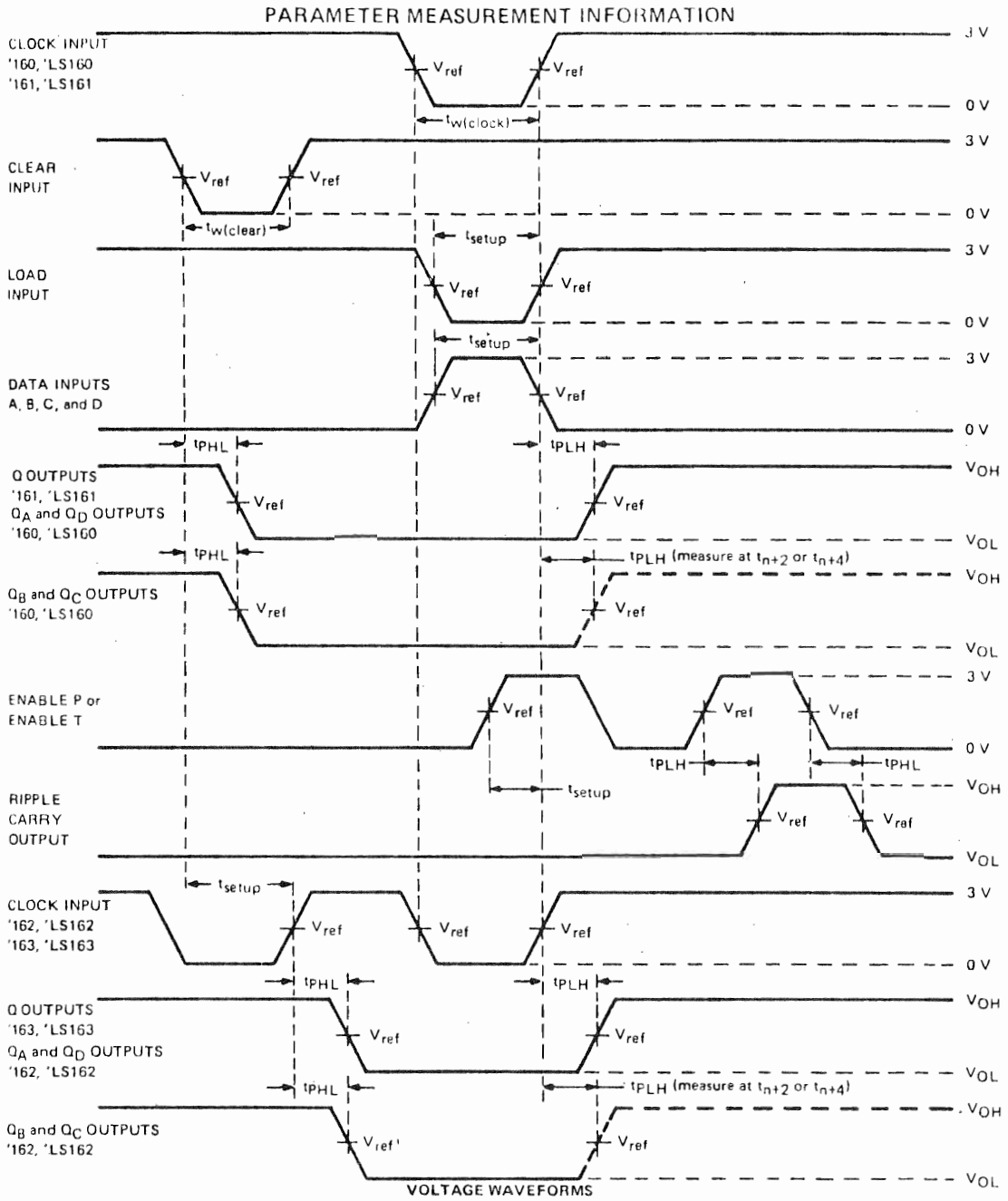
VOLTAGE WAVEFORMS

NOTES A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160, 'LS162 and 'S162, and at t_{n+16} for '161, '163, 'LS161, 'LS163, and 'S163, where t_n is the bit time when all outputs are low.

C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160 thru 'LS163, $V_{ref} = 1.3$ V.

FIGURE 1–SWITCHING TIMES



NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160 thru 'LS163, $V_{ref} = 1.3$ V.

FIGURE 2--SWITCHING TIMES

443-757
74LS161 (cont)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_I Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	Data or enable P	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
	Load, clock, or enable T					0.2			0.2	
	Clear ('LS160, 'LS161)					0.1			0.1	
	Clear ('LS162, 'LS163)					0.2			0.2	
I_{IH} High-level input current	Data or enable P	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
	Load, clock, or enable T					40			40	
	Clear ('LS160, 'LS161)					20			20	
	Clear ('LS162, 'LS163)					40			40	
I_{IL} Low-level input current	Data or enable P	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	Load, clock, or enable T					−0.8			−0.8	
	Clear ('LS160, 'LS161)					−0.4			0.4	
	Clear ('LS162, 'LS163)					−0.8			−0.8	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CCH} Supply current, all outputs high		V_{CC} = MAX,	See Note 3		18	31		18	31	mA
I_{CCL} Supply current, all outputs low		V_{CC} = MAX,	See Note 4		19	32		19	32	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2 and Notes 8 and 9	25	32		MHz
t_{PLH}	Clock	Ripple carry			23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock (load input high)	Any Q			16	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			17	25	ns
t_{PHL}					19	29	
t_{PLH}	Enable T	Ripple carry			15	23	ns
t_{PHL}					15	23	
t_{PHL}	Clear	Any Q			26	38	ns

¶f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low to high level output
t_{PHL} = propagation delay time, high to low level output
NOTES: 8. Load circuit is shown on page S-88.
9. Propagation delay for clearing is measured from the clear input for the 'LS160 and 'LS161 or from the clock input transition for the 'LS162 and 'LS163.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High level input voltage			2			2			V
V_{IL}	Low level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

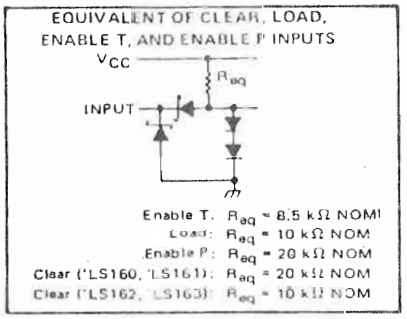
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

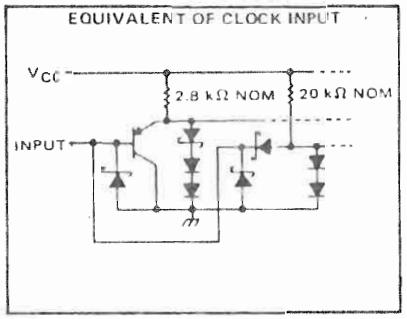
switching characteristics, V_{CC} = 5 V, T_A = 25°C

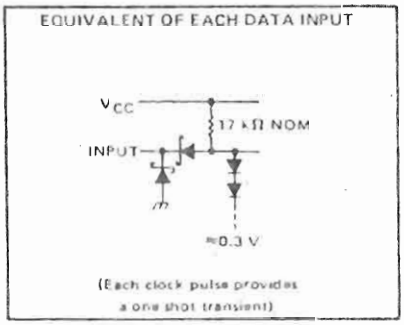
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2 and Notes 5 and 6	25	32		ns
t_{PLH}	Clock	Ripple carry			23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock (load input high)	Any Q			13	20	ns
t_{PHL}					15	23	
t_{PLH}	Clock (load input low)	Any Q			17	25	ns
t_{PHL}					19	29	
t_{PLH}	Enable T	Ripple carry			11	16	ns
t_{PHL}					11	16	
t_{PHL}	Clear	Any Q			26	38	ns

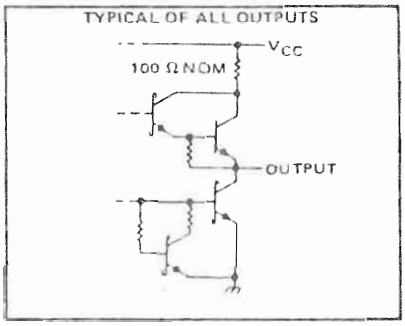
¶f_{max} Maximum clock frequency
t_{PLH} propagation delay time, low to high level output
t_{PHL} propagation delay time, high to low level output
NOTES: 5. Load circuit is shown on page S 87.
6. Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

schematics of inputs and outputs









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS' Circuits	−55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	0			0			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear[◊]	20			20			
Hold time at any input, t_{hold}		25¶			25¶			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

◊ This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

¶ The minimum hold time is 25 ns or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

12-BIT BINARY COUNTER

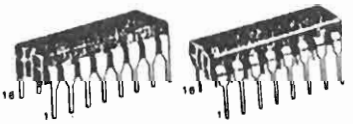
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

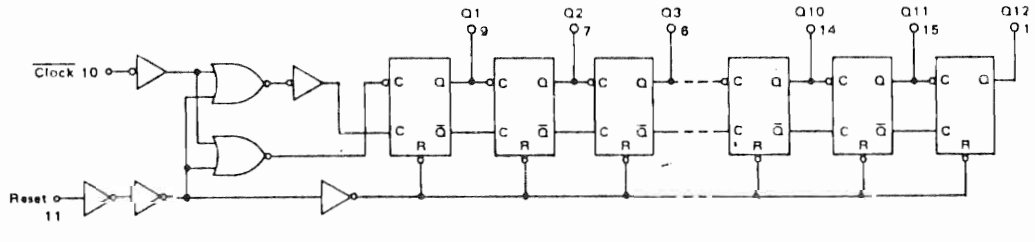
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↓	0	No Change
↓	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4 V_{DD} = Pin 16
Q5 = Pin 3 Q8 = Pin 13 V_{SS} = Pin 8
Q6 = Pin 2 Q9 = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

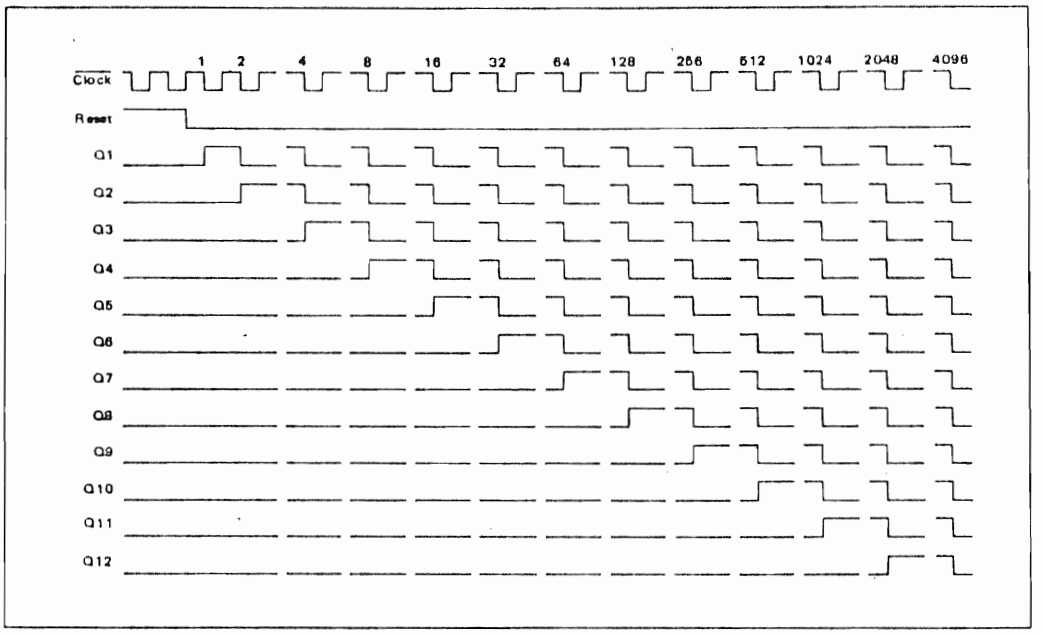
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

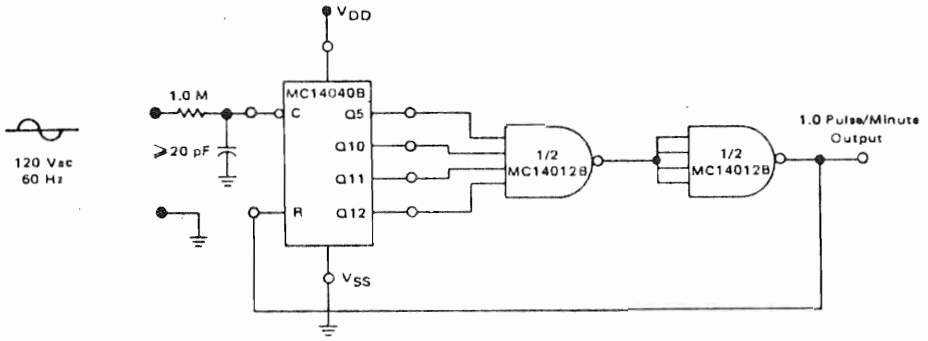
FIGURE 3 – TIMING DIAGRAM



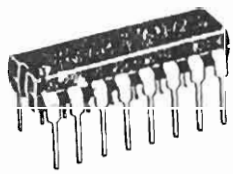
APPLICATIONS INFORMATION

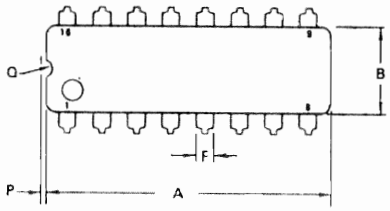
TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14040B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

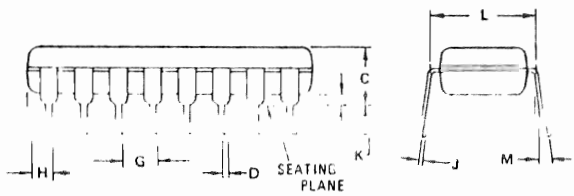


P SUFFIX
PLASTIC PACKAGE
CASE 648





NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 648-03

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_r = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Q1	t_{PHL}							
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L +315 ns		5.0	–	–	400	700	1050	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L +137 ns		10	–	–	170	280	420	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L +95 ns		15	–	–	120	210	320	
Clock to Q12								µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L +2415 ns		5.0	–	–	2.5	5.0	7.5	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L +867 ns		10	–	–	0.9	1.8	2.7	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L +475 ns		15	–	–	0.5	1.4	2.1	
Propagation Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.7 ns/pF) C_L +485 ns		5.0	–	–	570	1080	1620	
t_{PHL} = (0.66 ns/pF) C_L +182 ns		10	–	–	215	400	600	
t_{PHL} = (0.5 ns/pF) C_L +145 ns		15	–	–	170	300	450	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	250	385	ns
		10	–	–	55	100	150	
		15	–	–	38	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.5	–	–	MHz
		10	5.0	3.5	9.0	–	–	
		15	6.5	4.5	13	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–			
Minimum Reset Pulse Width	PW_R	5.0	–	–	320	640	960	ns
		10	–	–	120	240	360	
		15	–	–	80	180	270	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

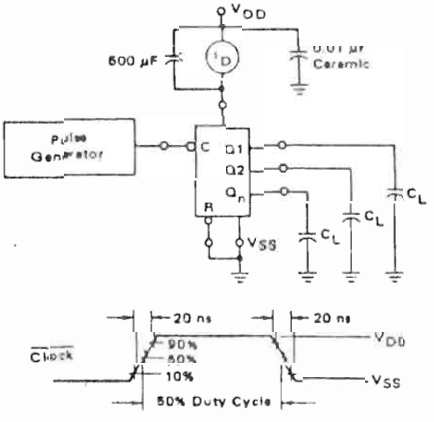
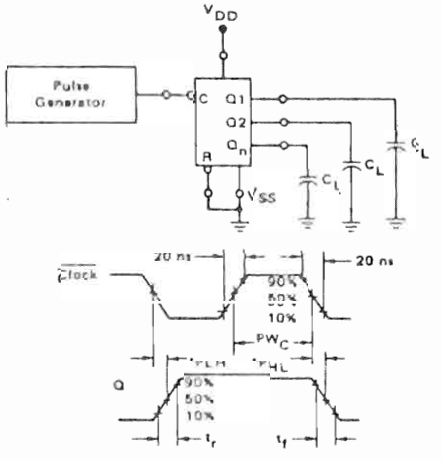


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



#443-764
2114/40L45

4K (1024 x 4 BIT) STATIC RAM

	2114-2	2114-3	2114
Max. Access Time (ns)	200	300	450

- High Density 18 Pin Package
- Access Time Selections From 200 - 450 ns
- Identical Cycle and Access Times
- Low Operating Power Dissipation .1 mW/Bit Typical
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Directly TTL Compatible: All Inputs and Outputs
- Common Data Input and Output Using Three-State Outputs
- Pin-Out Compatible with 3605 Bipolar PROM

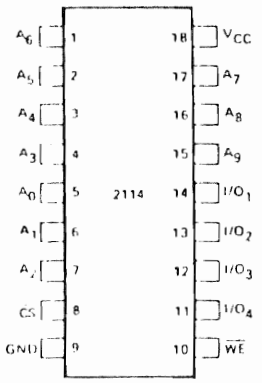
The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

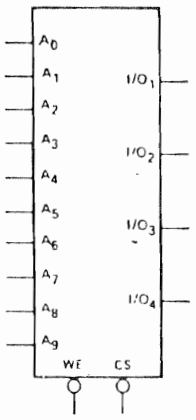
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

PIN CONFIGURATION



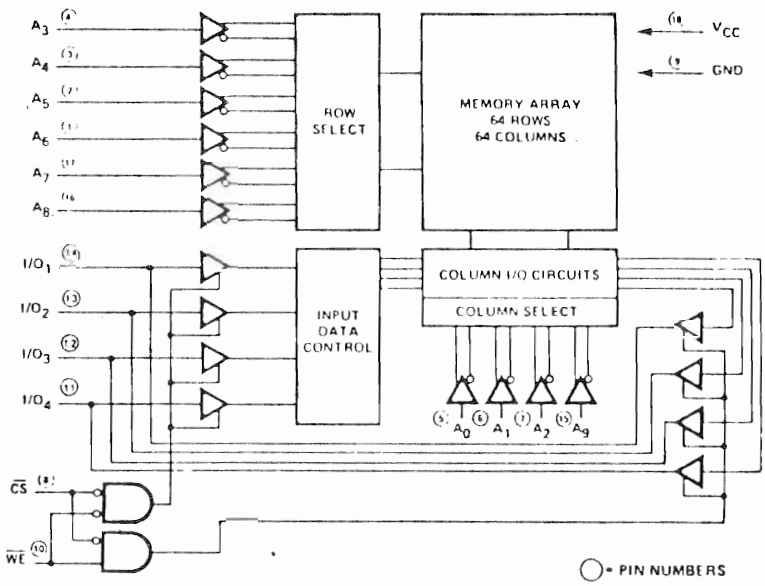
LOGIC SYMBOL



PIN NAMES

A_0 - A_9 ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$ WRITE ENABLE	GND GROUND
$\overline{CS}$ CHIP SELECT	
I/O_1 - I/O_4 DATA INPUT/OUTPUT	

BLOCK DIAGRAM



#443-764
2114/40L45 (cont)

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2 NOMINAL OPERATING LIMITS	2114-3 NOMINAL OPERATING LIMITS	2114 NOMINAL OPERATING LIMITS	UNIT
t_{RC}	Read Cycle Time	200	300	450	ns
t_A	Access Time	200	300	450	ns
t_{CO}	Chip Selection to Output Valid	TBD	TBD	150	ns
t_{CX}	Chip Selection to Output Active	0	0	0	ns
t_{OTD}	Output 3-state from Deselection	TBD TBD	TBD TBD	TBD 150	ns
t_{OHA}	Output Hold from Address Change	TBD	TBD	50	ns

WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2 NOMINAL OPERATING LIMITS	2114-3 NOMINAL OPERATING LIMITS	2114 NOMINAL OPERATING LIMITS	UNIT
t_{WC}	Write Cycle Time	200	300	450	ns
t_W	Write Time	TBD	TBD	250	ns
t_{WR}	Write Release Time	TBD	TBD	50	ns
t_{OTW}	Output 3-state from Write	TBD TBD	TBD TBD	TBD 150	ns
t_{DW}	Data to Write Time Overlap	TBD	TBD	250	ns
t_{DH}	Data Hold From Write Time	0	0	0	ns

A. C. CONDITIONS OF TEST

Input Pulse Levels . . . . . 0.8 Volt to 2.4 Volt
Input Rise and Fall Times . . . . . 10 nsec
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 50 pF

CAPACITANCE [3]

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	8	pF	V_{IN} = 0V

NOTES: 1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. This parameter is periodically sampled and not 100% tested.

NOMINAL OPERATING LIMITS

The nominal operating limits are provided in order to assure functional operation only. Guaranteed minimum and maximum operating limits will be specified in the final Data Sheet.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation 1.0W

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

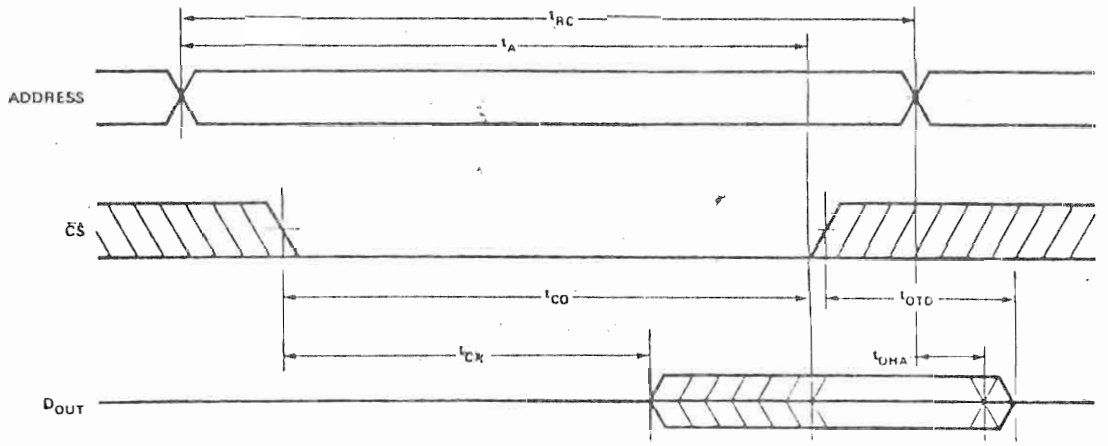
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	NOMINAL OPERATING LIMITS			UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10	µA	$\overline{CE}$ = 2.4V, $V_{I/O}$ = 0.45V to 4.0V
I_{CC1}	Power Supply Current		TBD	TBD	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current		TBD	TBD	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = - 1.0 mA

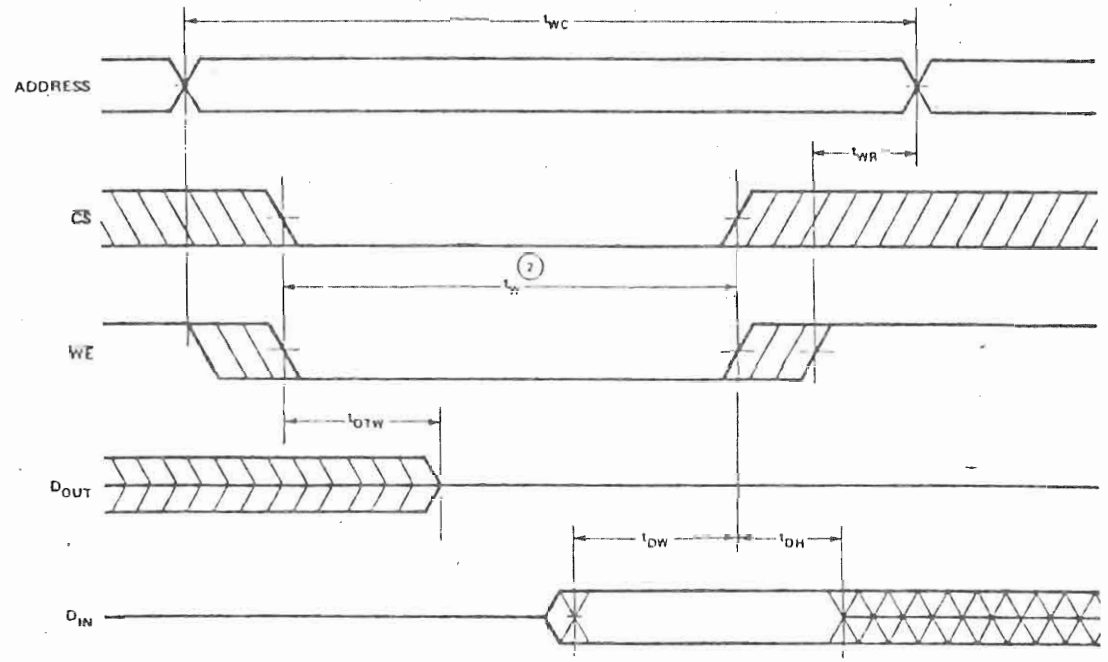
Waveforms

#443-764
2114/40L45 (cont)

READ CYCLE ①



WRITE CYCLE



NOTES:
① $\overline{WE}$ is high for a Read Cycle.
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the address, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be affected by $\overline{WE}$, the addresses, nor the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself — or in conjunction with the other — can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time — defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays on the 2114 are established such that address decoding propagates ahead of data inputs (keyed by the Write time). Therefore, it is permissable to establish the addresses coincident to the selection of a Write time, but no later. If the Write time precedes the addresses, the data in the previously addressed locations, or some other location, may be inadvertently changed.

While it is important that the addresses remain stable for the entire Write cycle, the data inputs are not required to remain stable. Appropriate voltage levels will be written into the cells as long as the data is stable for t_{DW} at the end of the Write time.

#443-778

4093

CD4093BM/CD4093BC quad 2-input NAND Schmitt trigger

general description

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

features

- Wide supply voltage range 3V to 15V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input) $T_A = 25°C$

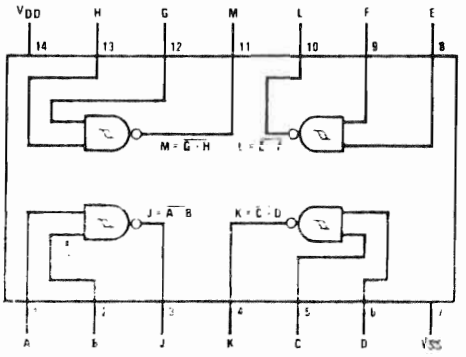
Typical	$V_{DD} = 5V$	$V_H = 1.5V$
	$V_{DD} = 10V$	$V_H = 2.2V$
	$V_{DD} = 15V$	$V_H = 2.7V$
Guaranteed		$V_H = 0.1\ V_{DD}$

applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

connection diagram

Dual-In-Line Package



#443-778
4093 (cont)

absolute maximum ratings

(Notes 1 and 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	500 mW
Lead Temperature (Soldering, 10 seconds) (T_L)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4093BM	−55°C to +125°C
CD4093BC	−40°C to +85°C

dc electrical characteristics CD4093BM (Note 2)

	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15.0	μA
		V_{DD} = 15V		1.0			1.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\|$ < 1μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\|$ < 1μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_T	Negative-Going Threshold Voltage (Any Input)	$\|I_O\|$ < 1μA								
		V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage (Any Input)	$\|I_O\|$ < 1μA								
		V_{DD} = 5V, V_O = 0.5V	3.5	3.65	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	7.0	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	10.5	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis (V_{T+} − V_T) (Any Input)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
		V_{DD} = 10V	1.0	4.30	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.30	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified

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4093 (cont)

dc electrical characteristics CD4093BC (Note 2)

PARAMETER		CONDITIONS	-40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15.0	μA
		V_{DD} = 15V		4.0			4.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.30	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	3.5	3.6	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	7.0	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	10.5	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis (V_{T+} - V_{T-})	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
		V_{DD} = 5V, V_O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V_{DD} = 15V, V_O = 13.5V	-3.6		-8.0	-8.8		-2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

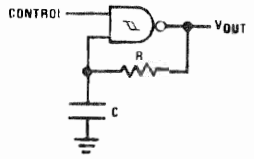
ac electrical characteristics T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200k, unless otherwise specified.

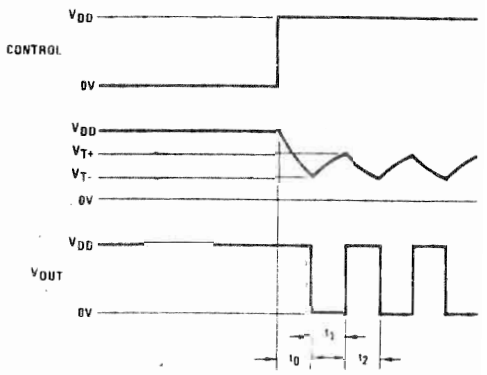
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	300	ns
		V_{DD} = 15V		80	240	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		90	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance			5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance			24		pF

#443-778
4093 (cont)

typical applications

Gated Oscillator





Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC \ln [V_{DD}/V_{T-}]$

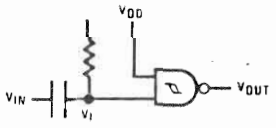
$t_1 = RC \ln [(V_{DD} - V_{T-})/(V_{DD} + V_{T+})]$

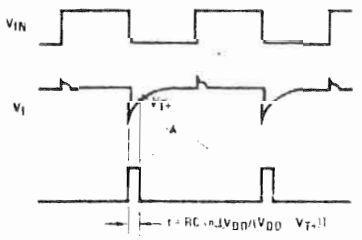
$t_2 = RC \ln [V_{T+}/V_{T-}]$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC \ln \dfrac{(V_{T+})(V_{DD} - V_{T-})}{(V_{T-})(V_{DD} - V_{T+})}}$$

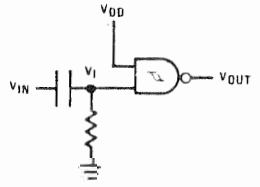
Gated One-Shot

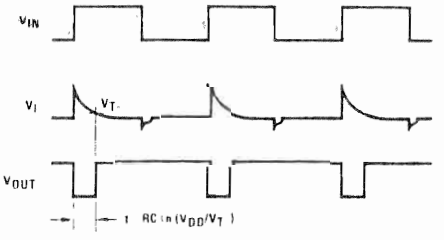
(a) Negative-Edge Triggered





(b) Positive-Edge Triggered



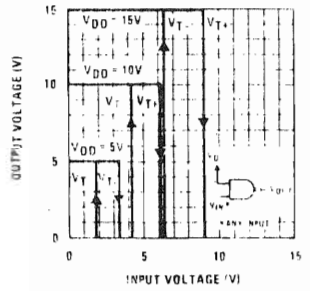


#443-778

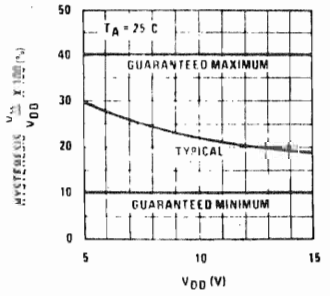
4093 (cont)

typical performance characteristics

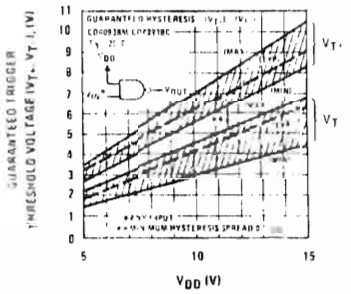
Typical Transfer Characteristics



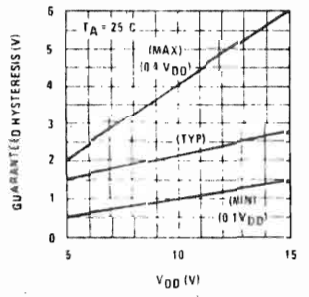
Guaranteed Hysteresis vs V_{DD}



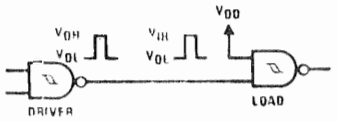
Guaranteed Trigger Threshold Voltage vs V_{DD}

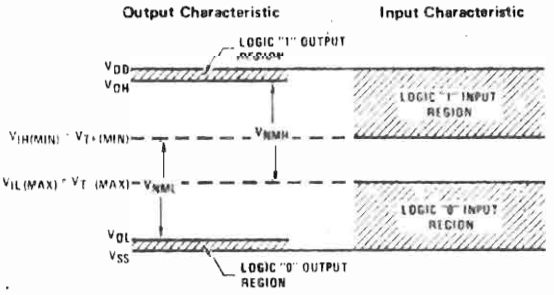


Guaranteed Hysteresis vs V_{DD}



input and output characteristics

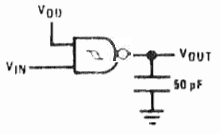


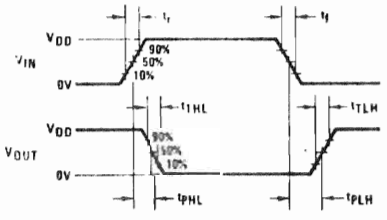


$V_{NML} = V_{IH(MIN)} - V_{OL} = V_{IH(MIN)} = V_{T+(MIN)}$

$V_{NMH} = V_{OH} - V_{IL(MAX)} = V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T-(MAX)}$

ac test circuits and switching time waveforms





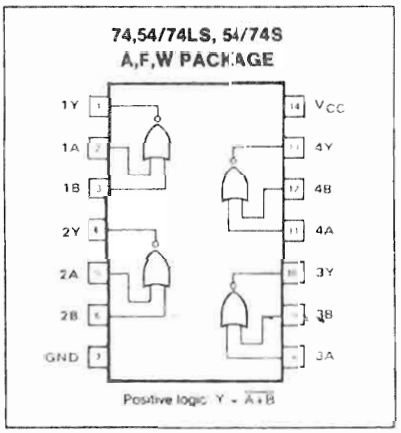
#443-779

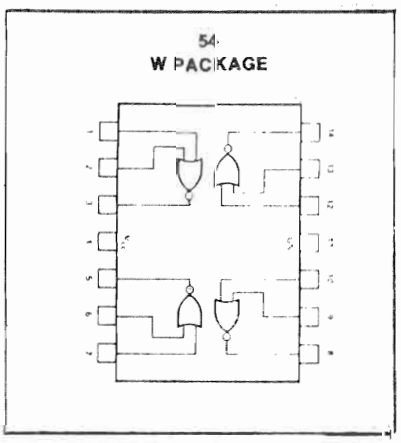
QUAD 2-INPUT NOR GATE 54/7402

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION





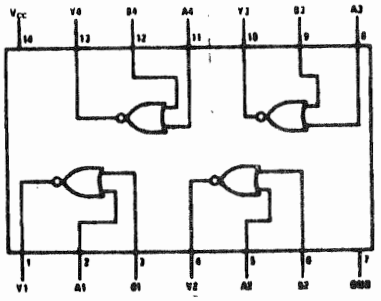
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time										
t_{PLH} Low-to-high		12	22		8	15		3.5	5.5	ns
t_{PHL} High-to-low		8	15		8	15		3.5	5.5	ns

Load circuit and typical waveforms are shown at the front of section.

Quad 2-Input NOR Gates

$Y = \overline{A+B}$



S402/7402(J), (N); S4L02/74L02(J), (N); S4LS02/74LS02(J), (N), (W); 7[illegible]

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			CONDITIONS			DM54/74 02, 25, 27			DM54L/74L L02			DM54LS/74LS L502, L527			[illegible] [illegible]			UNITS
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage					2			2			2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7			0.7			N/A	V
					DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5			N/A							V
				I_I = −18 mA							N/A			−1.5			−1.2	
I_{OH}	High Level Output Current				25, 27			−800										μA
					Others			−400			−200			−400			−1000	
V_{OH}	High Level Output Voltage		V_{CC} = Min	LS27								2.4						V
			V_{IL} = Max	Others	DM54	2.4	3.4		2.4	3.3		2.5	3.4		N/A			
			I_{OH} = Max		DM74	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			2			4			N/A	mA
					DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
			V_{IH} = 2V		DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	DM74									0.4				
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max	V_I = 5.5V				1			0.1						1	mA
				V_I = 7V										0.1				
I_{IH}	High Level Input Current	Data Inputs	V_{CC} = Max	V_I = 2.4V				40			10							μA
		Strobe of 25						160			N/A							
		All Inputs		V_I = 2.7V										20			60	
I_{IL}	Low Level Input Current	All Inputs	V_{CC} = Max	V_I = 0.3V							−0.18							mA
		Data Inputs		V_I = 0.4V				−1.6						−0.36				
		Strobe of 25						−6.4						N/A				
		All Inputs		V_I = 0.5V													−2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max (2)		DM54	−20		−55	−3		−15	−30		−130			N/A	mA
					DM74	−18		−55	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current		V_{CC} = Max			See Table												

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) National Semiconductor temporarily reserves the right to ship DM54/DM74LS02, L527 devices which have a minimum I_{OS} = 5.0 mA.

#443-779 74LS02

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
02	8	16	14	27
25	8	16	10	19
27	10	16	16	26
L02	0.8	1.6	1.4	2.6
LS02	1.6	3.2	2.8	5.4
LS27	2.0	4	3.4	6.8
S02	17	29	20	45
S260	17	29	26	45

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
02	C_L = 15 pF, R_L = 400Ω		12	22		8	15
25			13	22		8	15
27			7	11		10	15
L02	C_L = 50 pF, R_L = 4 kΩ		31	60		35	60
LS02, LS27	C_L = 15 pF, R_L = 2 kΩ		10	15		10	15
S02	C_L = 15 pF, R_L = 280Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280Ω		5	7.5		5	7.5
S260	C_L = 15 pF, R_L = 280Ω		4	5.5		4	6

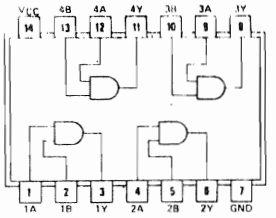
443-780

74LS08

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

positive logic:
Y = AB



SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			'08,			'H11, 'H21			'LS08, 'LS11, 'LS21			'S11			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−500			−400			−1000	μA
Low-level output current, I_{OL}		54 Family			16			20			4			20	mA
		74 Family			16			20			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
					'08			'H11, 'H21			'LS08, 'LS11, 'LS21			'S11			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.8	V
				74 Family			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §			*	−1.5		*	−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50							μA
				V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6			−2			−0.36				mA
				V_{IL} = 0.5 V												−2	
I_{OS}	Short circuit output current◆	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−6		−40	−40		−100	mA
				74 Family	−18		−55	−40		−100	−5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = 12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
◆Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of output short circuit should not exceed one second.
*The input clamp voltage specification is effective for Series 54/74, 54H, 74H part types shipped after 31 July 1973.

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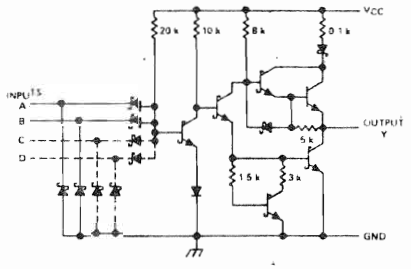
(cont)

74LS08

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'H11	18	30	30	48	8
'H21	12	20	20	32	8
'LS08	2.4	4.4	6.8	8.8	0.85
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S11	13.5	24	24	42	6.25

¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.



'LS08,

switching characteristics at V_{CC} = 5 V, T_A = 25°C

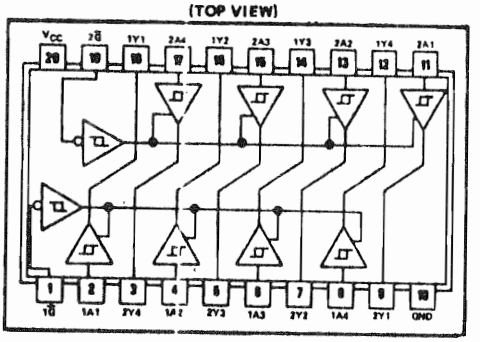
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
'H11, 'H21	C_L = 25 pF, R_L = 280 Ω		7.6	12		8.8	12
'LS08, 'LS11 'LS21	C_L = 15 pF, R_L = 2 kΩ		12	24		12	24
'S11	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5	7.5
	C_L = 50 pF, R_L = 280 Ω		6			7.5	

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)

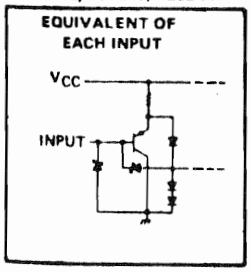


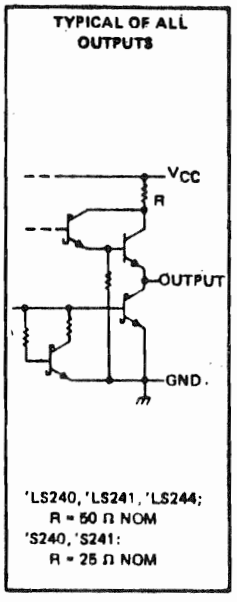
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

schematics of inputs and outputs

'LS240, 'LS241, 'LS244





recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs high	All		13	23		13	23	mA
		Outputs low	'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
		Outputs open	'LS240		29	50		29	50	
		All outputs disabled	'LS241, 'LS244		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18		12	18	ns
t_{PZL}	Output enable time to low level				20	30		20	30	ns
t_{PZH}	Output enable time to high level				15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		15	25	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

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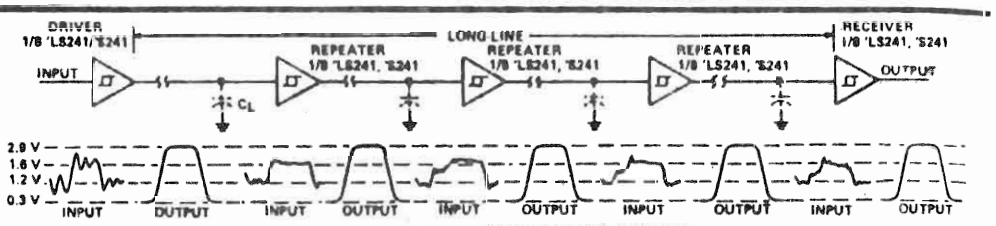
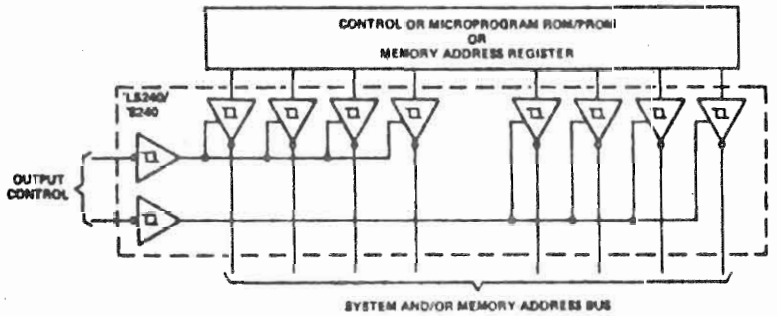
74LS244
(cont)

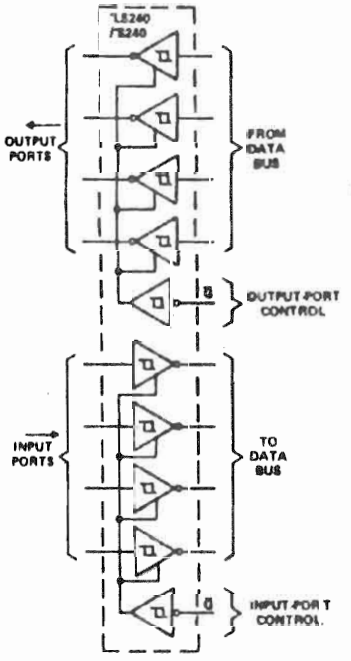
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



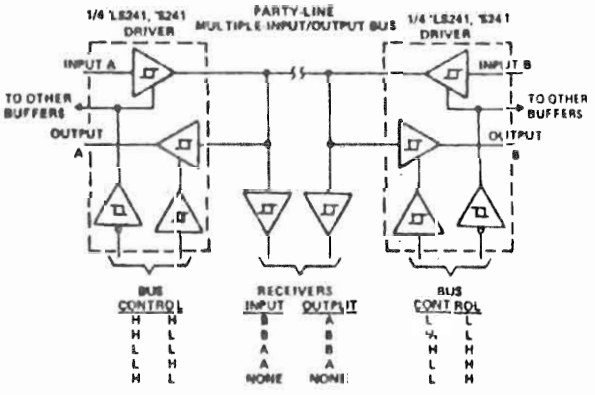
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS241, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



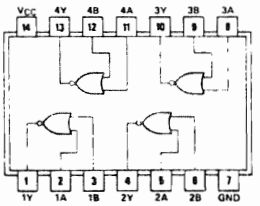
PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

#443-792

74LS132

SN54128 . . . 75-OHM LINE DRIVER
SN74128 . . . 50-OHM LINE DRIVER

positive logic:
$Y = \overline{A+B}$



SN54128 (J, W) **SN74128 (J, N)**

recommended operating conditions

		SERIES 54 / SERIES 74 '128			SERIES 54S / SERIES 74S 'S140			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−29			−40	mA
	74 Family			−42.4			−40	
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '128			SERIES 54S / SERIES 74S 'S140			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1,2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §§				−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	54 Family	2.4	3.4					V
				74 Family	2.4	3.4					
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = −13.2 mA		2.4						
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = MAX		2						
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	54 Family				2.5	3.4		
				74 Family				2.7	3.4		
			V_{CC} = MIN, V_{IL} = 0.5 V, R_D = 50 Ω to GND					2			
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.26	0.4			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−70		−180	−50		−225	mA
I_{CC}	Supply current, Total, outputs high	7	V_{CC} = MAX			12	21		10	18	mA
	Supply current, Total, outputs low					33	57		25	44	
	Supply current, Average per gate		V_{CC} = 5 V, 50% duty cycle			5.63			8.75		

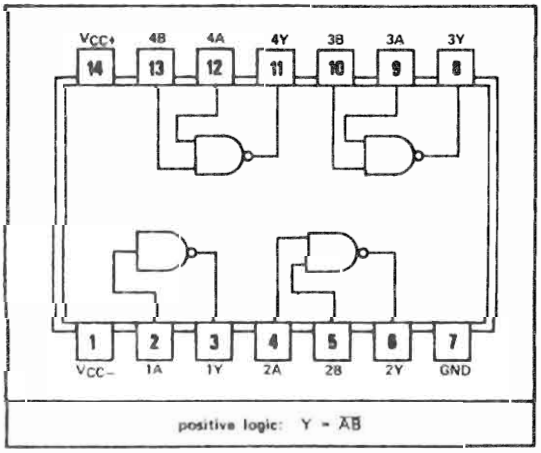
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§§I_I = −12 mA for '128 and −18 mA for 'S140.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

#443-794
1488/75188

QUADRUPLE LINE DRIVER

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with Motorola MC1488L
- Current-Limited Output . . . 10 mA Typical
- Power-Off Output Impedance . . . 300 Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

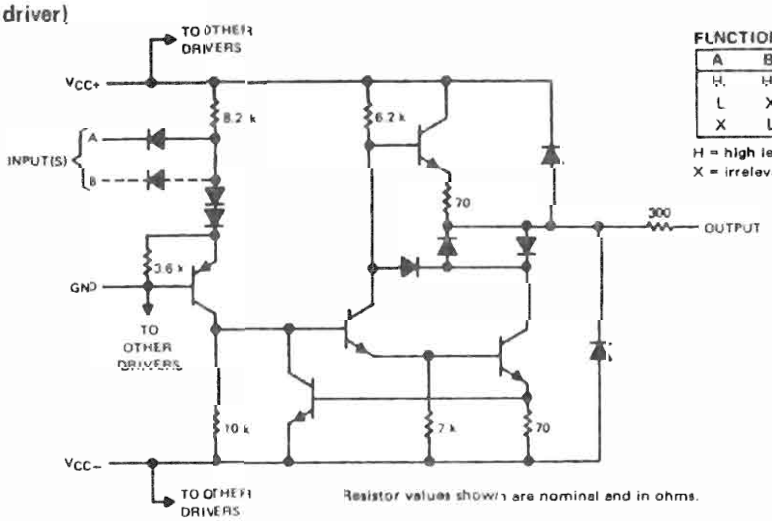
J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75188 is a monolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C. The device is characterized for operation from 0°C to 75°C.

schematic (each driver)



Resistor values shown are nominal and in ohms.

FUNCTION TABLE

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2)	15 V
Supply voltage V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2)	−15 V
Input voltage range	−15 V to 7 V
Output voltage range	−15 V to 15 V
Continuous total dissipation at (or below) 54°C free-air temperature (see Note 3)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Maximum Supply Voltage Curve, Figure 6.
3. Derate linearly to 780 mW at 75°C free-air temperature at the rate of 10.4 mW/°C.

#443-794
1488/75188 (cont)

electrical characteristics over operating free-air temperature range, V_{CC+} = 9 V, V_{CC-} = −9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level	V_I = 0.8 V,	V_O = 0	−6	−10	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level	V_I = 1.9 V,	V_O = 0	6	10	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_{CC-} = 0, V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20	mA
			All inputs at 0.8 V		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25	
			All inputs at 0.8 V		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34	
			All inputs at 0.8 V			12	
I_{CC-}	Supply current from V_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17	mA
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23	
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34	
			All inputs at 0.8 V			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576	

†All typical values are at T_A = 25°C.

NOTE 4: The algebraic convention where the most-positive (least negative) limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more-negative voltage.

switching characteristics, V_{CC+} = 9 V, V_{CC-} = −9 V, T_A = 25°C

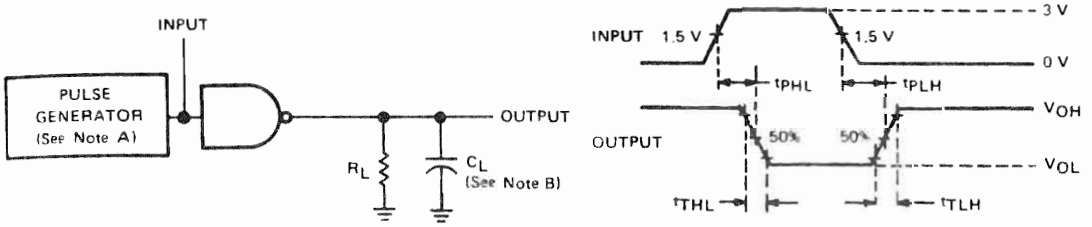
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ, See Figure 1		220	375	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	175	ns
t_{TLH}	Transition time, low-to-high-level output‡			55	100	ns
t_{THL}	Transition time, high-to-low-level output‡			45	75	ns
t_{TLH}	Transition time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		2.5		μs
t_{THL}	Transition time, high-to-low-level output§			3.0		μs

‡Measured between 10% and 90% points of output waveform.

§Measured between +3 V and −3 V points of output waveform (EIA RS-232C conditions)

#443-794
1488/75188 (cont)

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTE: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS

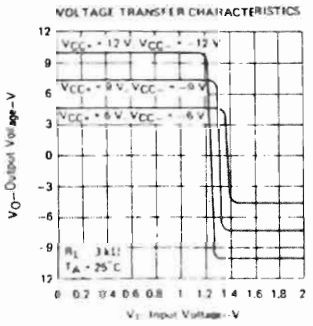


FIGURE 2

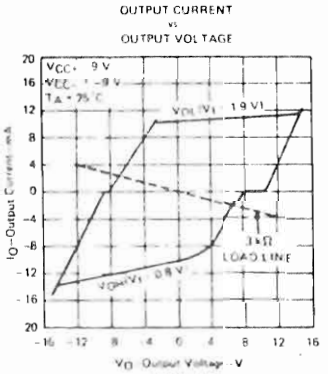


FIGURE 3

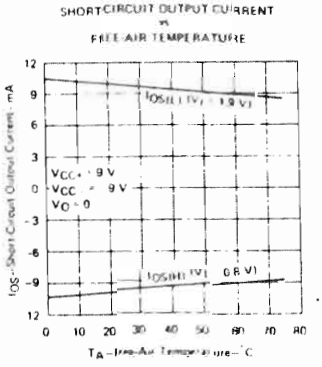


FIGURE 4

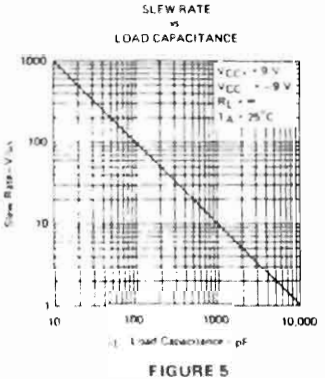


FIGURE 5

#443-794
1488/75188 (cont)

THERMAL INFORMATION

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

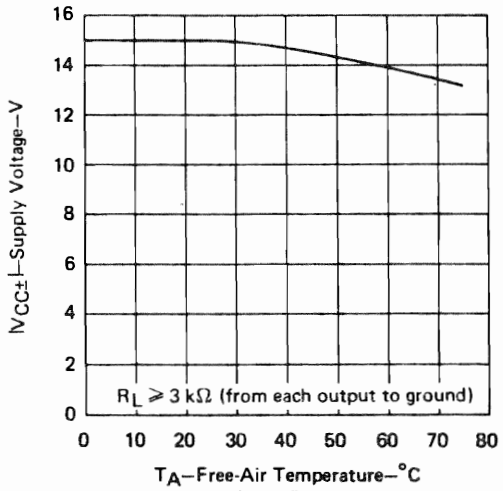


FIGURE 6

TYPICAL APPLICATION DATA

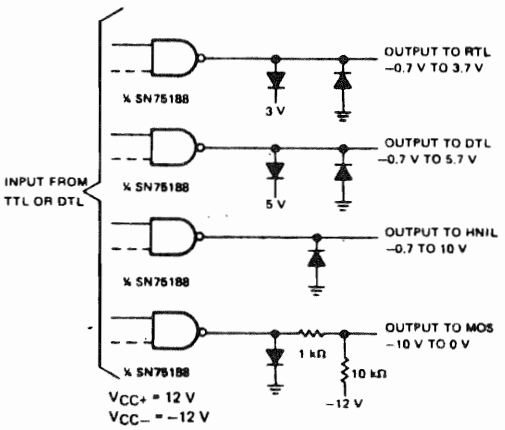
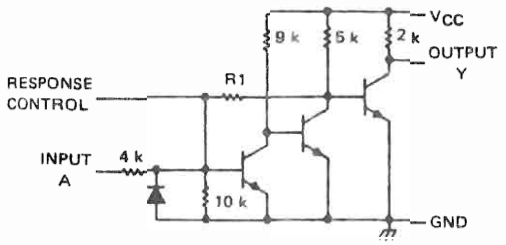


FIGURE 7—LOGIC TRANSLATOR APPLICATIONS

#443-795
1489
75189

- Input Resistance . . . 3 kΩ to 7 kΩ
- Input Signal Range . . . ±30 V
- Fully Interchangeable with Motorola MC1489, MC1489A
- Operates From Single 5-V Supply
- Built-in Input Hysteresis (Double Thresholds)
- Response Control Provides:
  Input Threshold Shifting
  Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

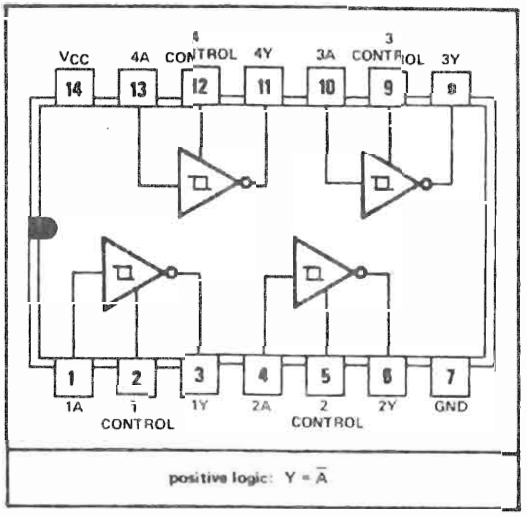
schematic (each receiver)



	SN75189	SN75189A
R1	10 k	2 k

Resistor values shown are nominal and in ohms.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75189 and SN75189A are monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected from this terminal to ground to provide input noise filtering.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage	±30 V
Output current	20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

#443-795
1489
75189 (continued)

electrical characteristics over operating free-air temperature range, V_{CC} = 5V ± 1%, (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN75189 MIN	SN75189 TYP‡	SN75189 MAX	SN75189A MIN	SN75189A TYP‡	SN75189A MAX	UNIT
V_{T+}	Positive-going threshold voltage	1			1		1.5	1.75	1.9	2.25	V
V_{T-}	Negative-going threshold voltage	1			0.75		1.25	0.75	0.97	1.25	V
V_{OH}	High-level output voltage	1	V_I = 0.75 V,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	V
			Input open,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	
V_{OL}	Low-level output voltage	1	V_I = 3 V,	I_{OL} = 10 mA		0.2	0.45		0.2	0.45	V
I_{IH}	High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
			V_I = 3 V		0.43			0.43			
I_{IL}	Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
			V_I = −3 V		−0.43			−0.43			
I_{OS}	Short-circuit output current	3				−3			−3		mA
I_{CC}	Supply current	2	V_I = 5 V,	Outputs open		20	26		20	26	mA

†All characteristics are measured with the response control terminal open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	4	C_L = 15 pF, R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Propagation delay time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		25	50	
t_{TLH}	Transition time, low-to-high-level output		C_L = 15 pF, R_L = 3.9 kΩ		120	175	ns
t_{THL}	Transition time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION§

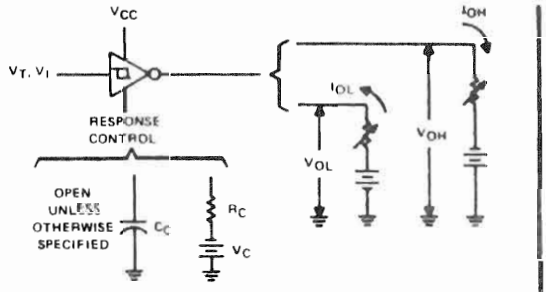
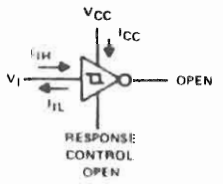


FIGURE 1–V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously

FIGURE 2–I_{IH}, I_{IL}, I_{CC}

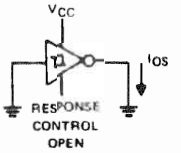
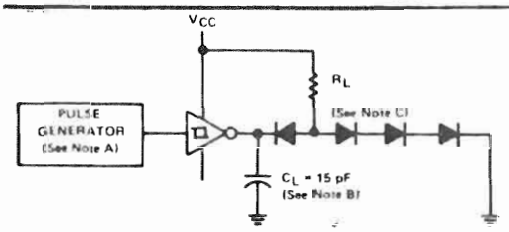
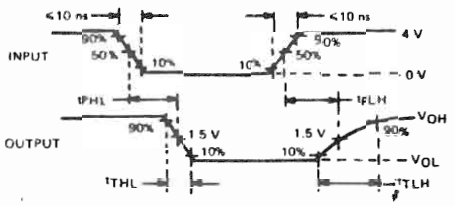


FIGURE 3–I_{OS}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} ≈ 50 Ω, t_w = 500 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 4–SWITCHING TIMES

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TYPICAL CHARACTERISTICS

SN75189
OUTPUT VOLTAGE vs INPUT VOLTAGE

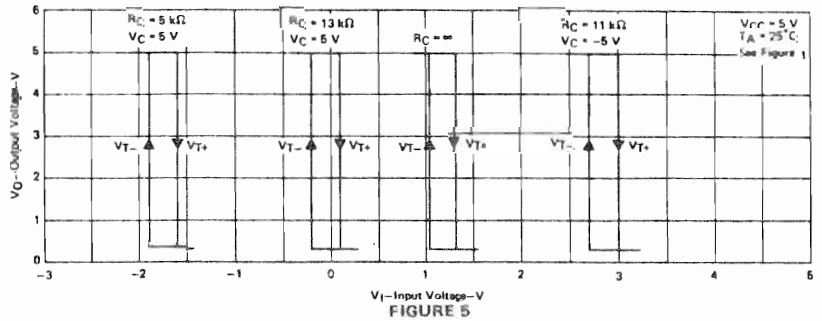


FIGURE 5

SN75189A
OUTPUT VOLTAGE vs INPUT VOLTAGE

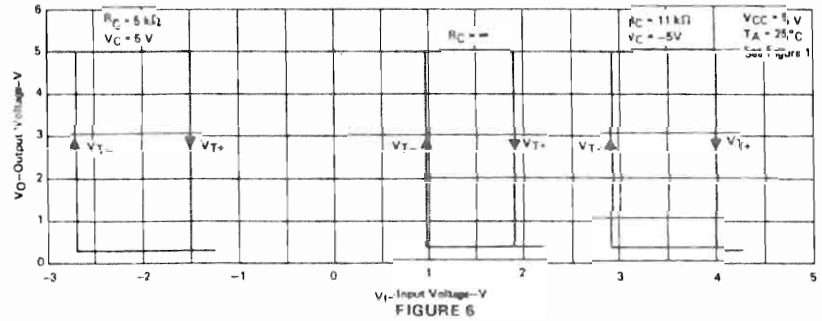


FIGURE 6

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

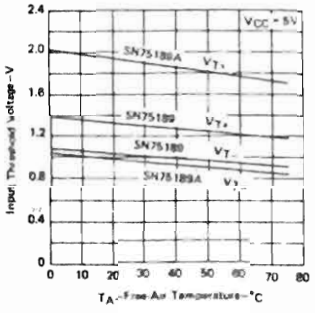


FIGURE 7

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

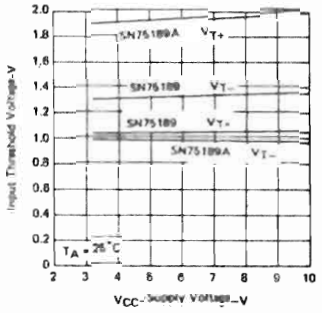


FIGURE 8

TYPICAL CHARACTERISTICS

SN75189
NOISE REJECTION

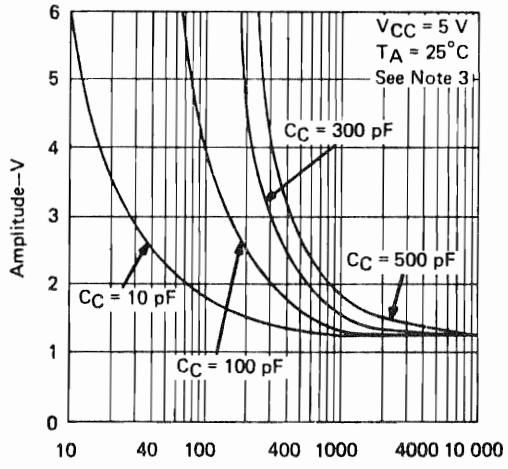


FIGURE 9

SN75189A
NOISE REJECTION

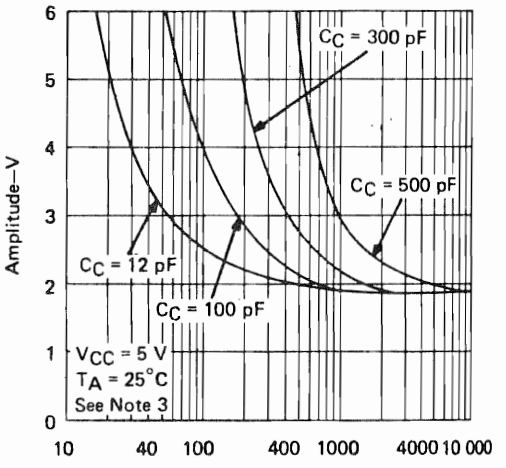


FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

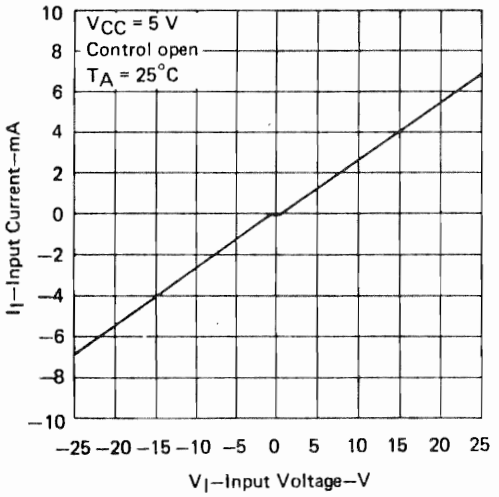


FIGURE 11

THERMAL INFORMATION

DISSIPATION DERATING CURVE

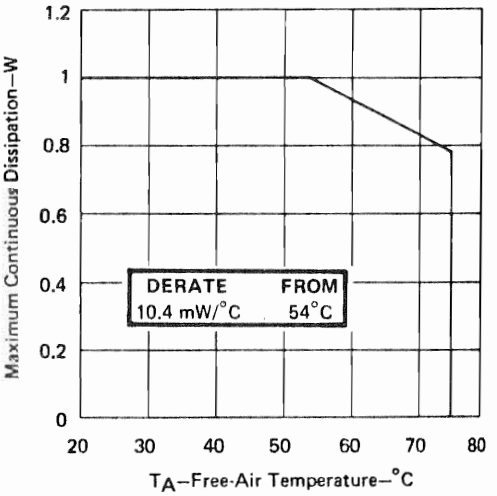


FIGURE 12

NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

#443-799

74LS157

TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

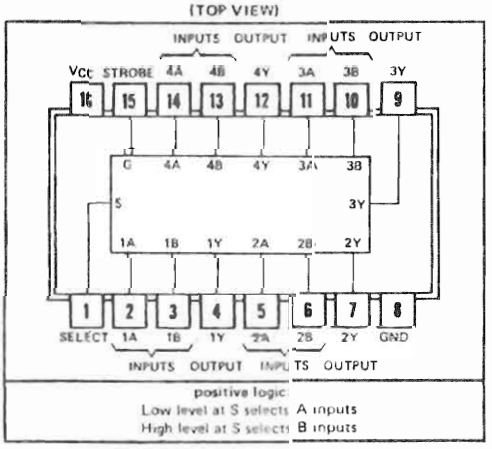
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

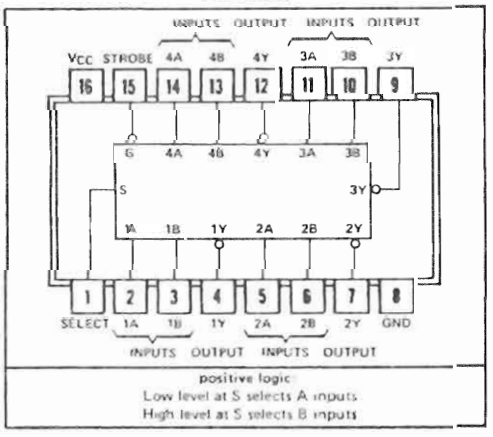
INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

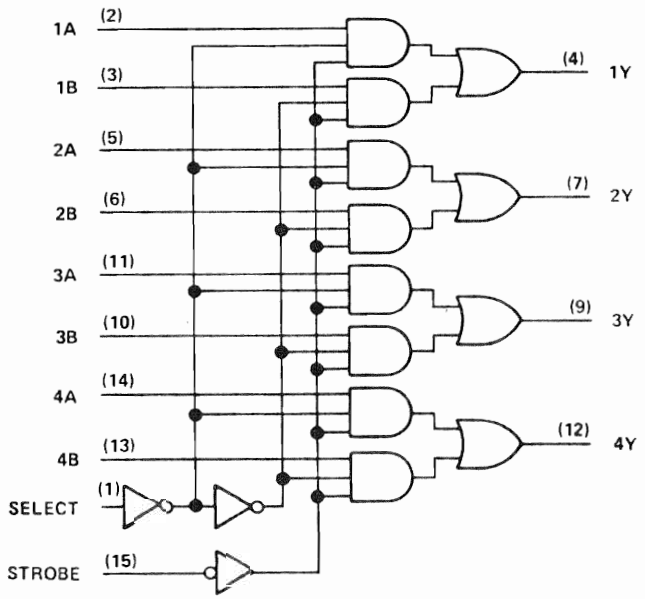
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#443-799
74LS157
(cont)

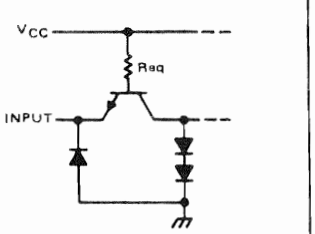
functional block diagram

'157, 'L157



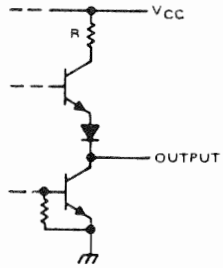
schematics of inputs and outputs

'157, 'L157
EQUIVALENT OF EACH INPUT



'157: Req = 4 kΩ NOM
'L157: Req = 8 kΩ NOM

'157, 'L157
TYPICAL OF ALL OUTPUTS



'157: R = 100 Ω NOM
'L157: R = 200 Ω NOM

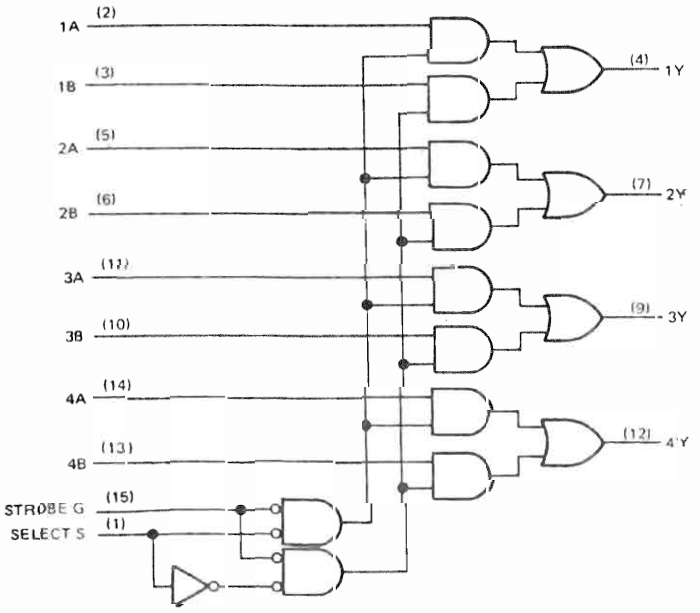
#443-799

74LS157

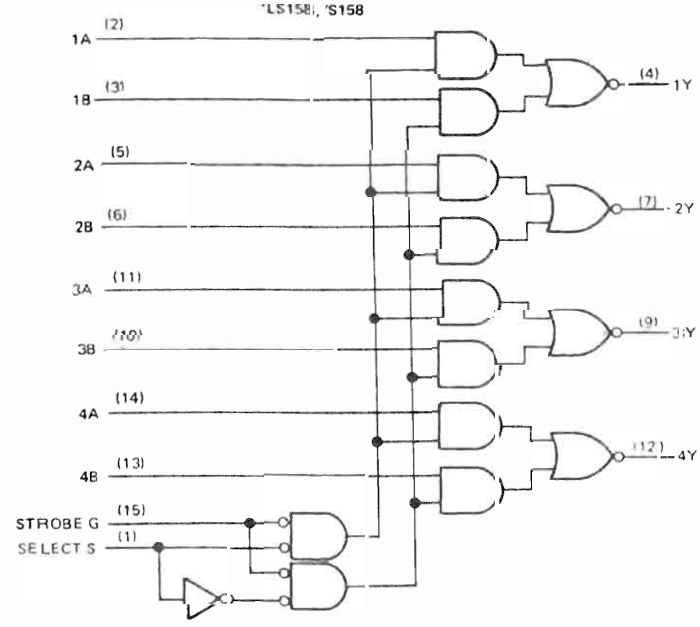
(cont)

functional block diagrams

'LS157, 'S157

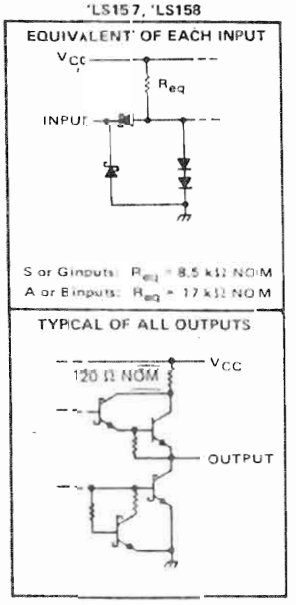


'LS158, 'S158

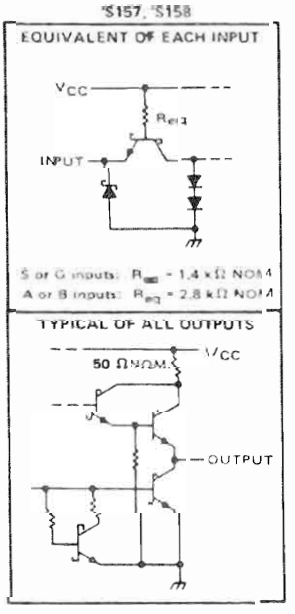


schematics of inputs and outputs

'LS157, 'LS158



'S157, 'S158



#443-799

74LS157

(cont)

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54157			SN74157			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		30	48		30	48	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω,		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

#443-799

74LS157

(cont)

recommended operating conditions

	SN54L157			SN74L157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−9		−28	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		15	24	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 800 Ω,		18	28	ns
t_{PHL}				18	28	
t_{PLH}	Strobe			26	40	ns
t_{PHL}				28	42	
t_{PLH}	Select			30	46	ns
t_{PHL}				36	54	

¶t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low level output

#443-799

74LS157

(cont)

TYPES SN54LS157, SN54LS158, SN74LS157, SN74LS158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	S or G input	V_{CC} = MAX,	V_I = 7 V				0.2			0.2	mA
		A or B input						0.1			0.1	
I_{IH}	High-level input current	S or G input	V_{CC} = MAX,	V_I = 2.7 V				40			40	μA
		A or B input						20			20	
I_{IL}	Low-level input current	S or G input	V_{CC} = MAX,	V_I = 0.4 V				−0.8			−0.8	mA
		A or B input						−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2	'LS157		9.7	16		9.7	16	mA
					'LS158		4.8	8		4.8	8	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	'LS157			'LS158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 2 kΩ,		9	14		7	12	ns
t_{PHL}				9	14		7	12	
t_{PLH}	Strobe			13	20		11	17	ns
t_{PHL}				14	21		12	18	
t_{PLH}	Select			15	23		13	20	ns
t_{PHL}				18	27		16	24	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

#443-799

74LS157

(cont)

TYPES SN54S157, SN54S158, SN74S157, SN74S158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S157 SN74S157			SN54S158 SN74S158			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	S or G input	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
	A or B input					50			50	
I_{IL} Low-level input current	S or G input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
	A or B input					−2			−2	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC} Supply current		V_{CC} = MAX, All inputs at 4.5 V, See Note 2			50	78		39	61	mA
		V_{CC} = MAX, A inputs at 4.5 V, B,G,S, inputs at 0 V, See Note 2							81	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
Note 2: I_{CC} is measured with all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 280 Ω,		5	7.5		4	6	ns
t_{PHL}				4.5	6.5		4	6	
t_{PLH}	Strobe			8.5	12.5		6.5	11.5	ns
t_{PHL}				7.5	12		7	12	
t_{PLH}	Select			9.5	15		8	12	ns
t_{PHL}				9.5	15		8	12	

¶ t_{PLH} propagation delay time, low to high-level output
t_{PHL} propagation delay time, high to low-level output

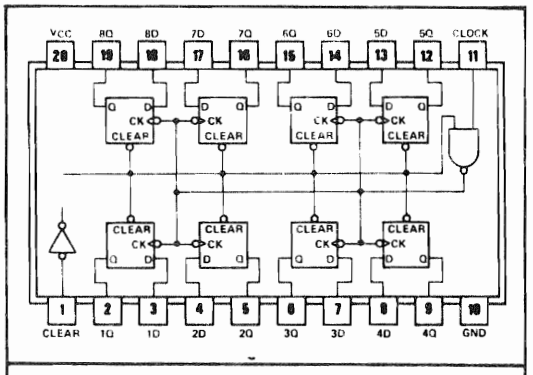
#443-805

74LS273

OCTAL D-TYPE FLIP-FLOP WITH CLEAR

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

N DUAL-IN-LINE
PACKAGE (TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 25 MHz while maximum clock frequency is typically 35 megahertz. Typical power dissipation is 39 milliwats per flip-flop.

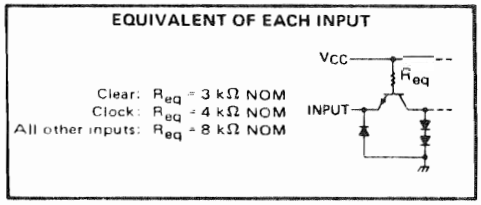
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

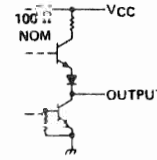
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.

schematics of inputs and output

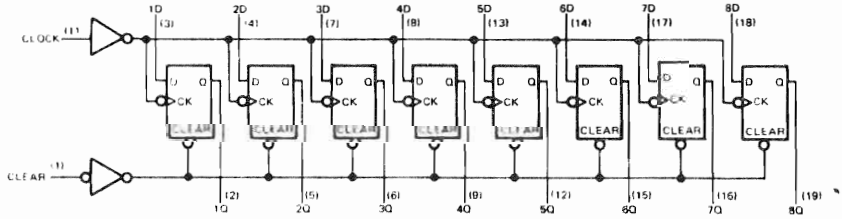
EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



functional block diagram



#443-805 (cont)

74LS273

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock or clear pulse, t_w		20			ns
Setup time, t_{setup}	Data input	20†			ns
	Clear inactive state	25†			ns
Data hold time, t_{hold}		5†			ns
Operating free-air temperature, T_A		0		70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2			V
V_{IL} Low-level input voltage					0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH} High-level input current	Clear	V_{CC} = MAX, V_I = 2.4 V			80	μA
	Clock or D				40	
I_{IL} Low-level input current	Clear	V_{CC} = MAX, V_I = 0.4 V			−3.2	mA
	Clock or D				−1.6	
I_{OS} Short-circuit output current§		V_{CC} = MAX	−18		−57	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2		62	94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

INS8250 Asynchronous Communications Element

General Description

The INS8250 is a programmable Asynchronous Communications Element (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250 is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

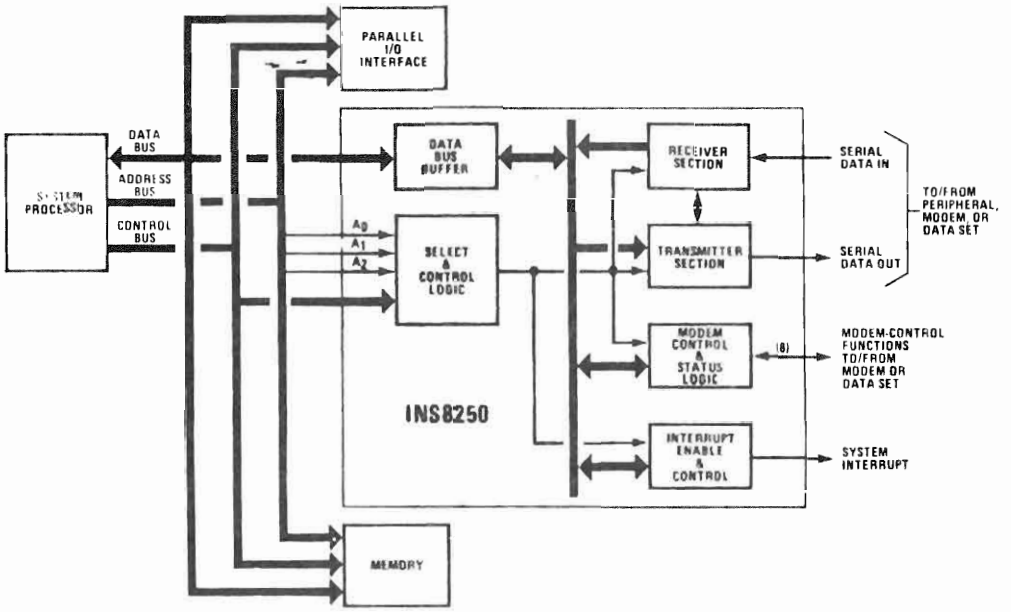
The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM and parallel-to serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

In addition to providing control of asynchronous data communications, the INS8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the INS8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Features

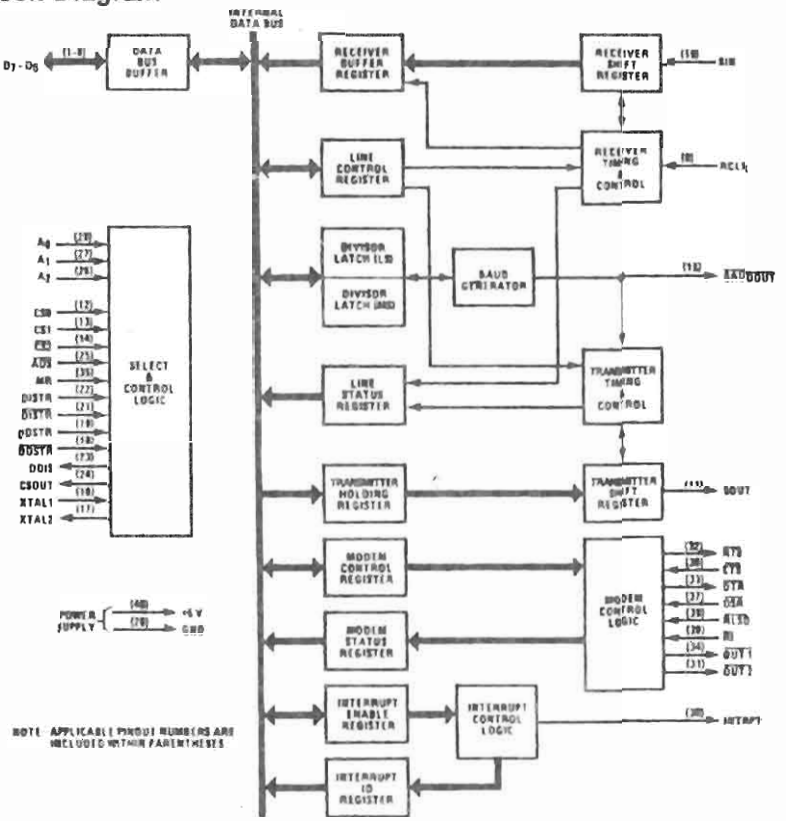
- Designed to be Easily Interfaced to Most Popular Microprocessors (SC/MP, PACE, 8080A, 6800, etc.)
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1½-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56k Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- TRI-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Single +5 Volt Power Supply

INS8250 General System Configuration



#443-874
INS8250 (continued)

INS8250 Block Diagram



INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 - 14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 - 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB is reset low when the Master Reset (MR) input is active (low); the DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM Control Register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT\ 2}$) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7 - D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt sources has an active high condition. Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Pin Configuration

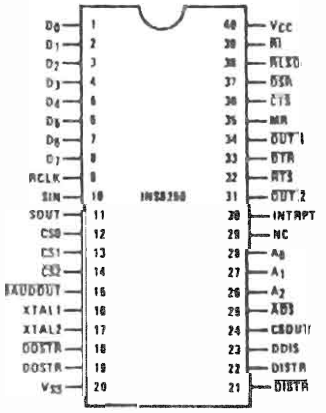


Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1 - 7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 Are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low
	MODEM Signal Inputs	Bits 4 - 7 = Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{BAUDOUT}$	Writing into Either Divisor Latch	Low
CSOUT	$\overline{ADS}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = CSOUT · RCLK · DISTR (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
$\overline{OUT 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT 1}$	Master Reset	High
D_7 - D_0 Data Bus Lines	In TRI-STATE Mode, Unless CSOUT · DISTR = High or CSOUT · DOSTR = High	TRI-STATE Data (ACE to CPU) Data (CPU to ACE)

INS8250 Accessible Registers

The system programmer may access or control any of the INS8250 registers summarized in table 2 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Table 2. Summary of INS8250 Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 PROGRAMMABLE BAUD RATE GENERATOR

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 5 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–
56000	3	14.285

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the INS8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1. Bit 1 is reset to logic 0 immediately upon reading the Interrupt Identification Register.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state, the receiver Serial Input (SIN) is disconnected, the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input, the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the INS8250 chip in an INS8080A system and in a microcomputer system with a high-capacity data bus.

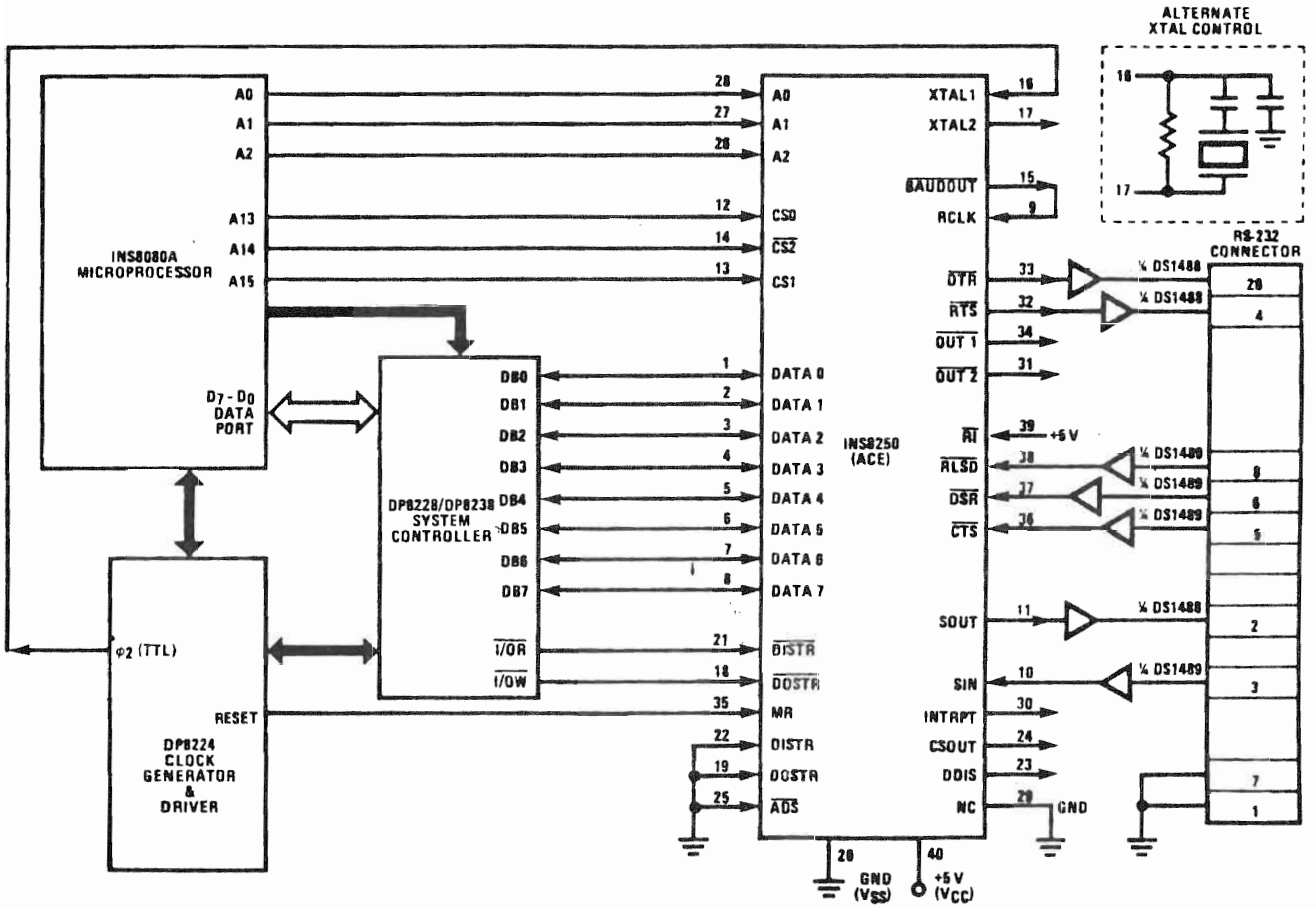


Figure 1. Typical INS8080A/INS8250 RS-232 Terminal Interface

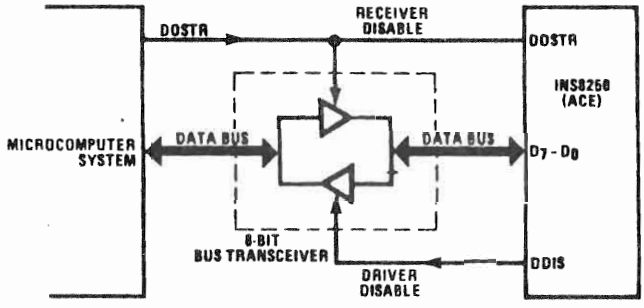


Figure 2. Typical Interface for a High-Capacity Data Bus

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to V_{SS} . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 400 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

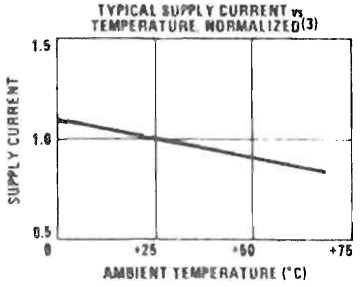
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	−0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA on all outputs, I_{OH} = −100 μA
V_{OH}	Output High Voltage	2.4			V	
I_{CC} (AV)	Avg Power Supply Current (V_{CC})		65	80	mA	
I_{IL}	Input Leakage			±10	μA	
I_{CL}	Clock Leakage			±10	μA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0 V

Symbol	Parameter	Typ	Max	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	f_c = 1 MHz Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	



#443-874
INS8250 (continued)

AC Electrical Characteristics

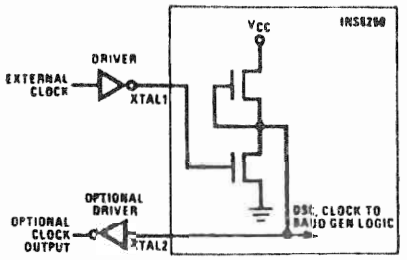
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%

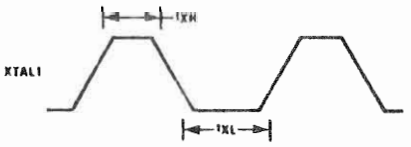
Symbol	Parameter	Typical	Units	Test Conditions
t_{AW}	Address Strobe Width	100	ns	
t_{AS}	Address Setup Time	110	ns	
t_{AH}	Address Hold Time	10	ns	
t_{CSS}	Chip Select Output Delay from Strobe	100	ns	
t_{DID}	$\overline{DISTR}$/DISTR Strobe Delay	100	ns	
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	200	ns	
t_{RC}	Read Cycle Delay	2000	ns	
RC	Read Cycle = $t_{AW} + t_{DID} + t_{DIW} + t_{RC}$	2400	ns	
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	150	ns	
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	250	ns	
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	100	ns	
t_{DOD}	$\overline{DOSTR}$/DOSTR Strobe Delay	200	ns	
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	200	ns	
t_{WC}	Write Cycle Delay	2000	ns	
WC	Write Cycle = $t_{AW} + t_{DOD} + t_{DOW} + t_{WC}$	2500	ns	
t_{DS}	Data Setup Time	200	ns	
t_{DH}	Data Hold Time	50	ns	
t_{CSC}	Chip Select Output Delay from Select	200	ns	
t_{DIC}	$\overline{DISTR}$/DISTR Delay from Select	200	ns	
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select	200	ns	

*Applicable only when $\overline{ADS}$ input is not tied permanently low.

AC Electrical Characteristics (cont'd.)

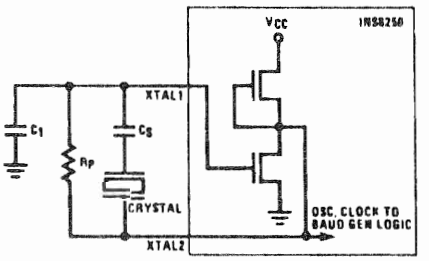
Symbol	Parameter	Min	Max	Units	Test Conditions
BAUD GENERATOR					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100 pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100 pF Load
t_{LW}	Baud Output Down Time	425 typ		ns	100 pF Load
t_{HW}	Baud Output Up Time	330 typ		ns	100 pF Load
RECEIVER					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100 pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt		1 typ	μs	100 pF Load
TRANSMITTER					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt		1 typ	μs	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start		1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)		1 typ	μs	100 pF Load
MODEM CONTROL					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output		1 typ	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		1 typ	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)		1 typ	μs	100 pF Load





Timing	Min	Units
tXH	100	ns
tXL	115	ns

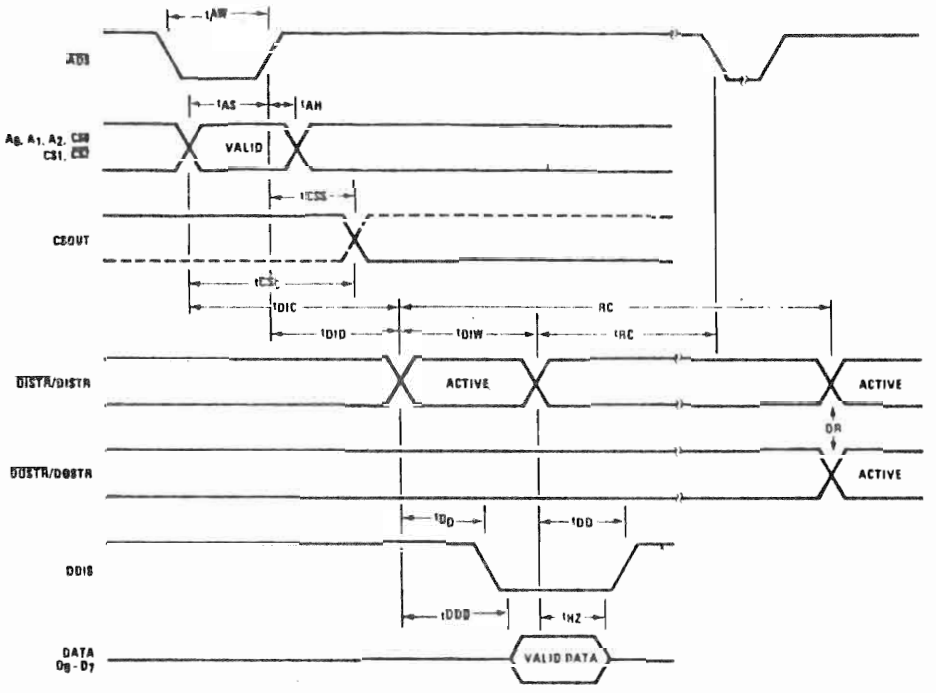
A. External Clock Input (3.1 MHz Max.)



CRYSTAL	RP	CS	C1
3.1 MHz	1 MΩ	60 pF	10 pF

B. Typical Crystal Oscillator Network

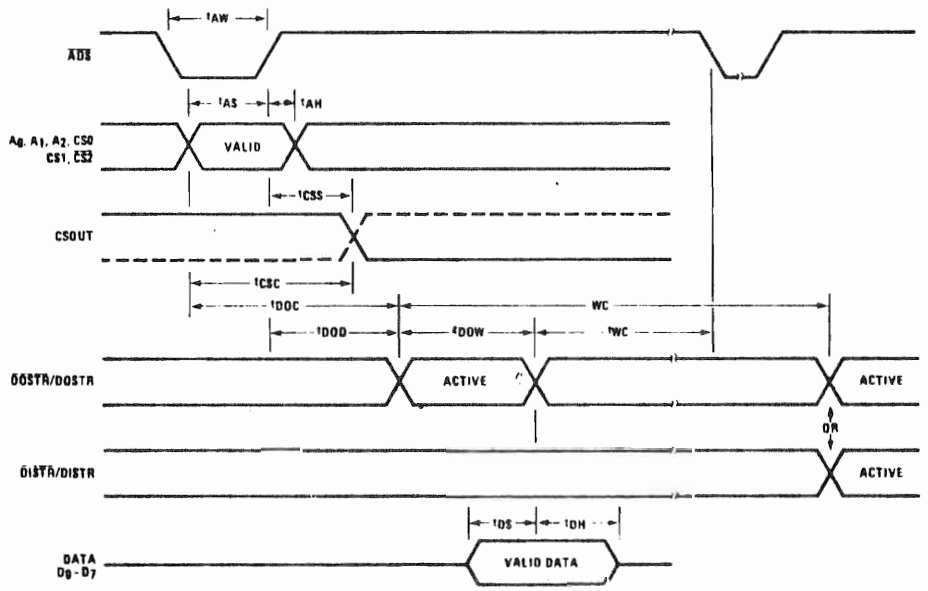
Timing Waveforms



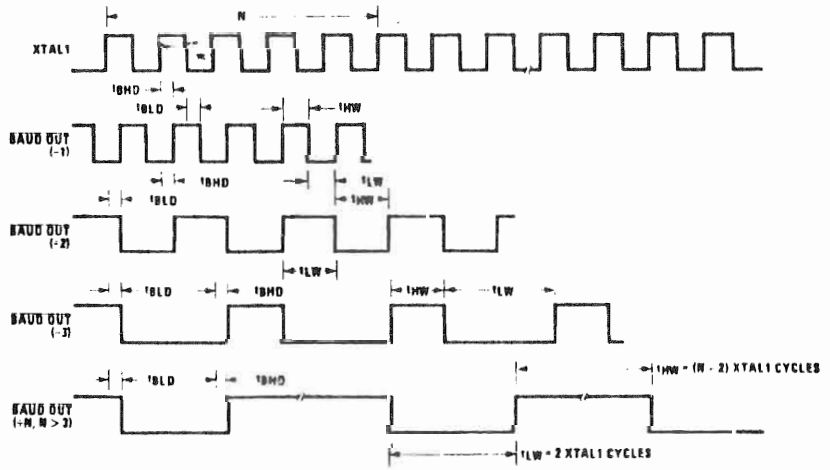
Read Cycle

#443-874
INS8250 (continued)

Timing Waveforms (cont'd.)



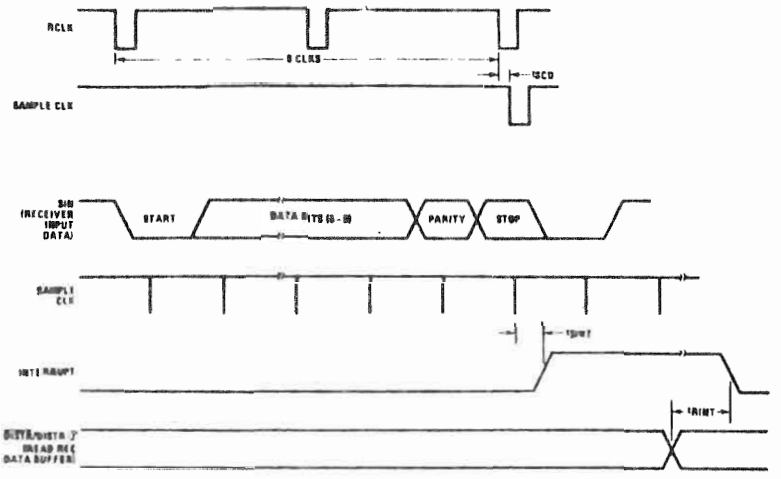
Write Cycle



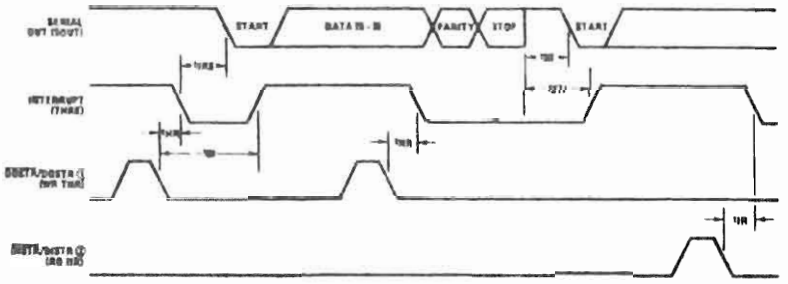
BAUDOUT Timing

#443-874
INS8250 (continued)

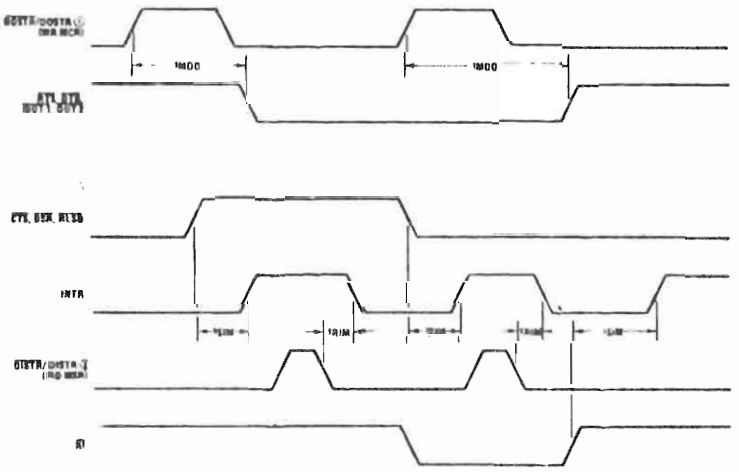
Timing Waveforms (cont'd.)



Receiver Timing



Transmitter Timing



MODEM Controls Timing

NOTES:
(1) See Write Cycle Timing
(2) See Read Cycle Timing

#443-877

74LS138

TTL
MSI

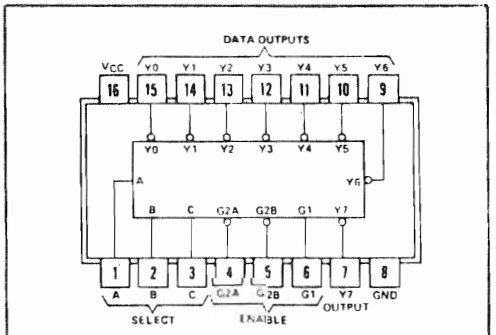
TYPES SN54LS138, SN54LS139, SN54S138, SN54S139, SN74LS138, SN74LS139, SN74S138, SN74S139 DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7611804, DECEMBER 1972—REVISED OCTOBER 1976

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Clamped for High Performance

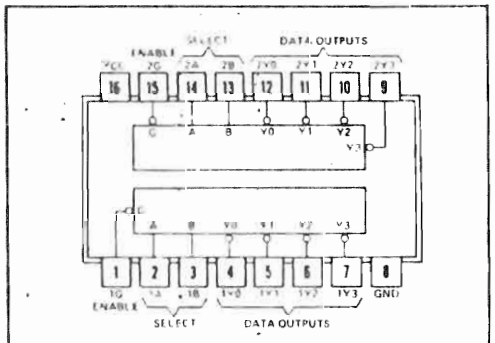
TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139	22 ns	34 mW
'S139	7.5 ns	300 mW

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74LS139, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C. Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.

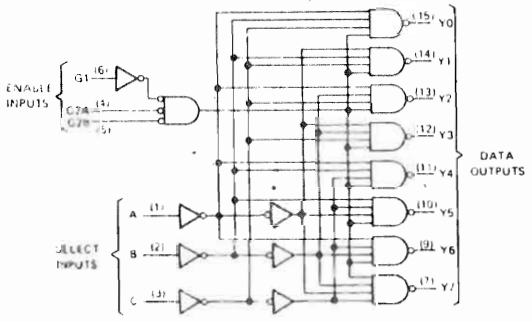
#443-877

74LS138

TYPES SN54LS138, SN54S138, SN54LS139, SN54S139
SN74LS138, SN74S138, SN74LS139, SN74S139
DECODERS/DEMULTIPLEXERS

functional block diagrams and logic

'LS138, 'S138



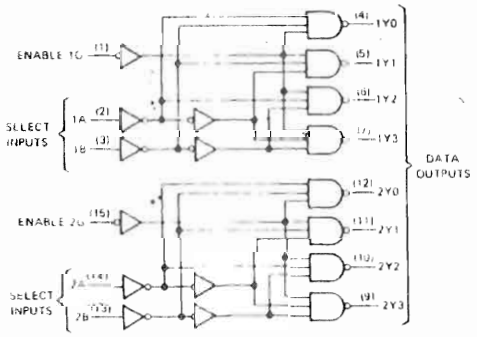
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139, 'S139

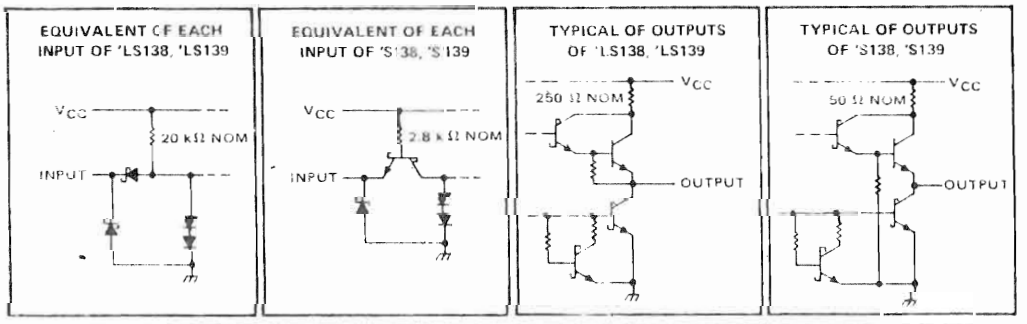


'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

schematics of inputs and outputs



#443-877

74LS138

TYPES SN54LS138, SN54LS139, SN74LS138, SN74LS139, DECODERS/DEMULTIPLEXERS

REVISED OCTOBER 1976

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS138, SN54LS139 Circuits . . . . . −55°C to 125°C
SN74LS138, SN74LS139 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS138 SN54LS139			SN74LS138 SN74LS139			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS138 SN54LS139			SN74LS138 SN74LS139			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\,max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\,max}$	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC} Supply current	V_{CC} = MAX, Outputs enabled and open	LS138		6.3	10		6.3	10	mA
		LS139		6.8	11		6.8	11	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS138 SN74LS138			SN54LS139 SN74LS139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	C_L = 15 pF, R_L = 2 kΩ,		13	20		13	20	ns
t_{PHL}						27	41		22	33	ns
t_{PLH}			3			18	27		18	29	ns
t_{PHL}						26	39		25	38	ns
t_{PLH}	Enable	Any	2			12	18		16	24	ns
t_{PHL}						21	32		21	32	ns
t_{PLH}			3			17	26				ns
t_{PHL}						25	38				ns

¶t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S138, SN54S139 Circuits . . . . . −55°C to 125°C
SN74S138, SN74S139 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54S138 SN74S139			SN74S138 SN74S139			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S138 SN74S138			SN54S139 SN74S139			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		2.5	3.4		V
		SN74S'	2.7	3.4		2.7	3.4		
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC} Supply current	V_{CC} = MAX, Outputs enabled and open			49	70		60	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S138, SN74S138			SN54S139 SN74S139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary select	Any	2	C_L = 15 pF, R_L = 280 Ω,	4.5	7		5	7.5		ns
t_{PHL}					7	10.5		6.5	10		
t_{PLH}			3		7.5	12		7	12		ns
t_{PHL}					8	12		8	12		
t_{PLH}	Enable	Any	2		5	8		5	8		ns
t_{PHL}					7	11		6.5	10		
t_{PLH}			3		8	13					ns
t_{PHL}					7	11					

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

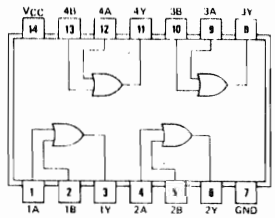
#443-875

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

positive logic:
Y = A+B



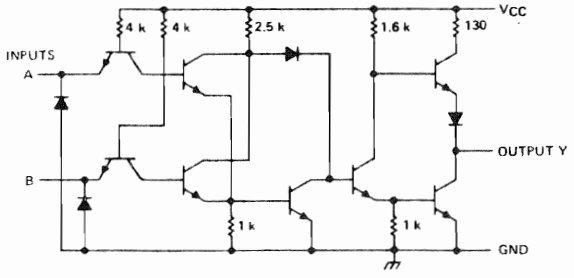
SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

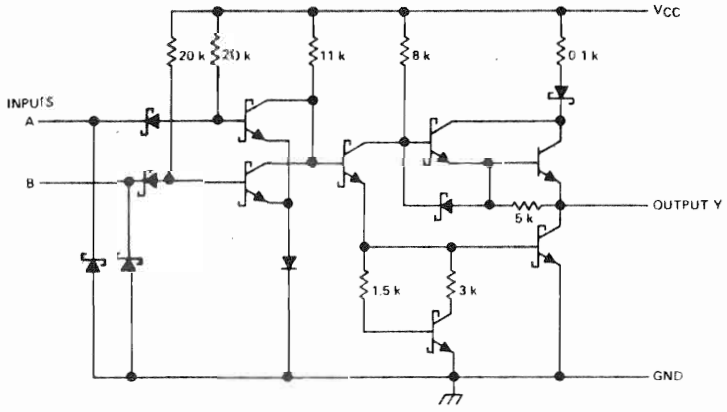
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
'LS32	C_L = 15 pF, R_L = 2 kΩ		14	22		14	22

schematics (each gate)



'32 CIRCUITS



'LS32 CIRCUITS

Resistor values shown are nominal and in ohms.

#443-875 (cont)

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '32			SERIES 54LS / SERIES 74LS 'LS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400	μA
Low-level output current, I_{OL}	54 Family			16			4	mA
	74 Family			16			8	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '32			SERIES 54LS / SERIES 74LS 'LS32			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		1, 2			2			2			V
V_{IL} Low-level input voltage		1, 2		54 Family			0.8			0.7	V
				74 Family			0.8			0.8	
V_I Input clamp voltage		3	V_{CC} = MIN, I_I = §,				*−1.5			−1.5	V
V_{OH} High-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.7	3.4		
V_{OL} Low-level output voltage		2	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4	V
				74 Family		0.2	0.4		0.35	0.5	
I_I Input current at maximum input voltage		4	V_{CC} = MAX, V_I = 5.5 V				1			0.1	mA
I_{IH} High-level input current		4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						20	
I_{IL} Low-level input current		5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−0.36	mA
I_{OS} Short-circuit output current♦		6	V_{CC} = MAX	54 Family	−20		−55	−6		−40	mA
				74 Family	−18		−55	−5		−42	
I_{CC} Supply current	Total, outputs high	7	V_{CC} = MAX			15	22		3.1	6.2	mA
	Total, outputs low					23	38		4.9	9.8	
	Average per gate		V_{CC} = 5 V, 50% duty cycle			4.75			1.00		

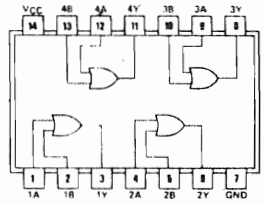
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS'.
♦Not more than one output should be shorted at a time.
*The input clamp voltage specification is effective for Series 54/74 parts date coded 7332 or higher.

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

Positive logic:
$Y = A+B$



SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			SERIES 54S SERIES 74S 'S32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.25	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400			−1000	μA
Low-level output current, I_{OL}		54 Family			16			4			20	mA
		74 Family			16			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			SERIES 54S SERIES 74S 'S32			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		1, 2			2			2			2			V
V_{IL}	Low-level input voltage		1, 2		54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN, I_I =				−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IL} = V_{IL} max	I_{OL} = MAX										V
					54 Family		0.2	0.4		0.25	0.4			0.5	
					74 Family		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX	V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current		4	V_{CC} = MAX	V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current		5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6			−0.4				mA
					V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX	54 Family	−20		−55	−20		−100	−40		−100	mA
					74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	Total, outputs high	7	V_{CC} = MAX			15	22		3.1	6.2		18	32	mA
		Total, outputs low					23	38		4.9	9.8		28	68	
		Average per gate		V_{CC} = 5 V, 50% duty cycle			1.75			1.0			7		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of the short circuit should be less than one second.

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74LS32

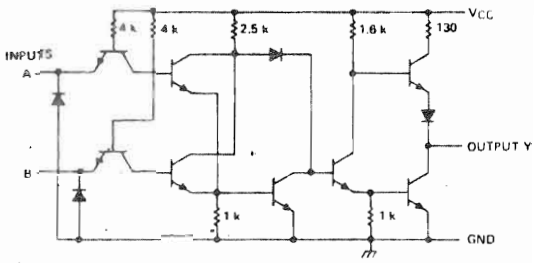
(cont.)

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

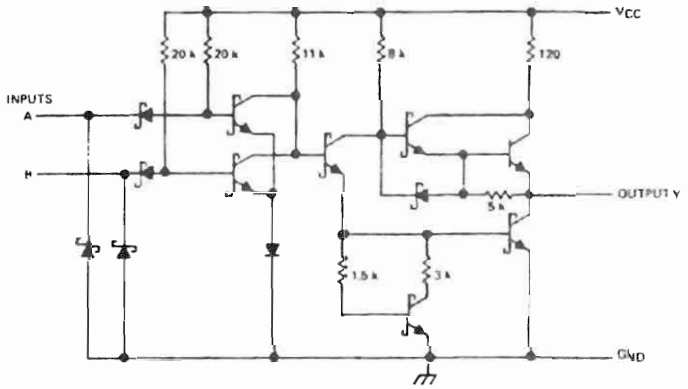
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
'LS32	C_L = 15 pF, R_L = 2 kΩ		14	22		14	22
'S32	C_L = 15 pF, R_L = 280 Ω		4	7		4	7
	C_L = 50 pF, R_L = 280 Ω		5			5	

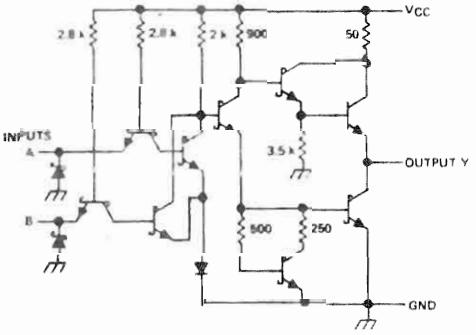
schematics (each gate)



'32 CIRCUITS



'LS32 CIRCUITS



'S32 CIRCUITS

Resistor values shown are nominal and in ohms.

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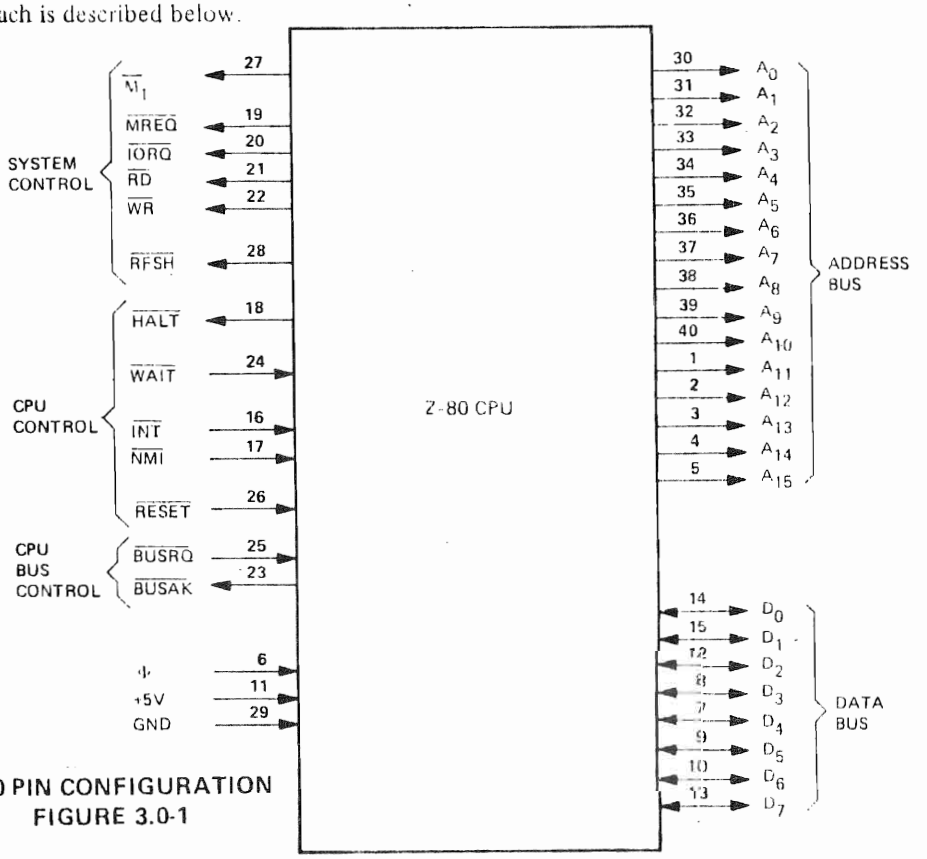
Z80 CPU

Z-80 CPU PIN DESCRIPTION

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in figure 3.0-1 and the function of each is described below.



Z-80 PIN CONFIGURATION
FIGURE 3.0-1

A_0-A_{15} (Address Bus)

Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7 (Data Bus)

Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one)

Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. $\overline{M1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$ (Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

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Z80 CPU (cont)

$\overline{IORQ}$ (Input/Output Request)	Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.
$\overline{RD}$ (Memory Read)	Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{WR}$ (Memory Write)	Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{RFSH}$ (Refresh)	Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.
$\overline{HALT}$ (Halt state)	Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.
$\overline{WAIT}$ (Wait)	Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.
$\overline{INT}$ (Interrupt Request)	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).
$\overline{NMI}$ (Non Maskable Interrupt)	Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note *that continuous* WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override a $\overline{NMI}$.

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Z80 CPU (cont)

$\overline{\text{RESET}}$	Input, active low. $\overline{\text{RESET}}$ forces the program counter to zero and initializes the CPU. The CPU initialization includes: 1) Disable the interrupt enable flip-flop 2) Set Register I = 00_H 3) Set Register R = 00_H 4) Set Interrupt Mode 0 During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.
$\overline{\text{BUSRQ}}$ (Bus Request)	Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When $\overline{\text{BUSRQ}}$ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.
$\overline{\text{BUSAK}}$ (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.
Φ	Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

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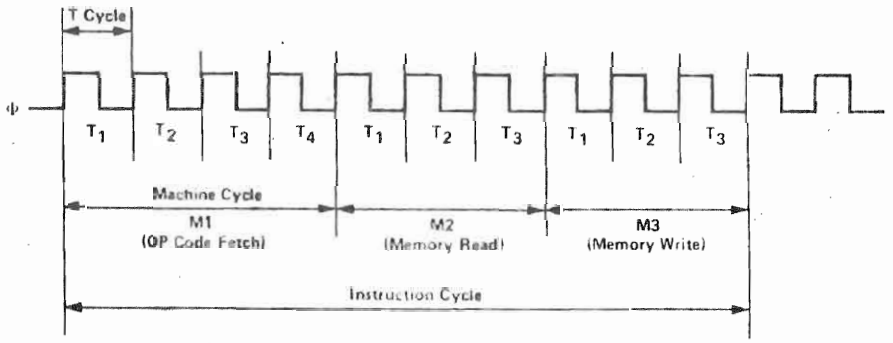
4.0 CPU TIMING — Z80 CPU (cont)

The Z-80 CPU executes instructions by stepping through a very precise set of a few basic operations. These include:

Memory read or write
I/O device read or write
Interrupt acknowledge

All instructions are merely a series of these basic operations. Each of these basic operations can take from three to six clock periods to complete or they can be lengthened to synchronize the CPU to the speed of external devices. The basic clock periods are referred to as T cycles and the basic operations are referred to as M (for machine) cycles. Figure 4.0-0 illustrates how a typical instruction will be merely a series of specific M and T cycles. Notice that this instruction consists of three machine cycles (M1, M2 and M3). The first machine cycle of any instruction is a fetch cycle which is four, five or six T cycles long (unless lengthened by the wait signal which will be fully described in the next section). The fetch cycle (M1) is used to fetch the OP code of the next instruction to be executed. Subsequent machine cycles move data between the CPU and memory or I/O devices and they may have anywhere from three to five T cycles (again they may be lengthened by wait states to synchronize the external devices to the CPU). The following paragraphs describe the timing which occurs within any of the basic machine cycles. In section 7, the exact timing for each instruction is specified.



BASIC CPU TIMING EXAMPLE
FIGURE 4.0-0

All CPU timing can be broken down into a few very simple timing diagrams as shown in figure 4.0-1 through 4.0-7. These diagrams show the following basic operations with and without wait states (wait states are added to synchronize the CPU to slow memory or I/O devices).

4.0-1. Instruction OP code fetch (M1 cycle)
4.0-2. Memory data read or write cycles
4.0-3. I/O read or write cycles
4.0-4. Bus Request/Acknowledge Cycle
4.0-5. Interrupt Request/Acknowledge Cycle
4.0-6. Non maskable Interrupt Request/Acknowledge Cycle
4.0-7. Exit from a HALT instruction

INSTRUCTION FETCH

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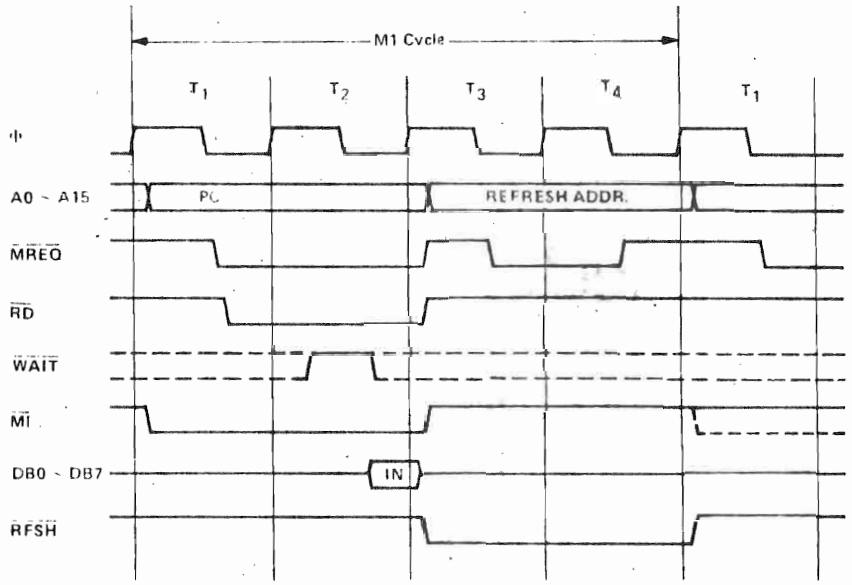
Z80 CPU (cont)

Figure 4.0-1 shows the timing during an M1 cycle (OP code fetch). Notice that the PC is placed on the address bus at the beginning of the M1 cycle. One half clock time later the $\overline{MREQ}$ signal goes active. At this time the address to the memory has had time to stabilize so that the falling edge of $\overline{MREQ}$ can be used directly as a chip enable clock to dynamic memories. The $\overline{RD}$ line also goes active to indicate that the memory read data should be enabled onto the CPU data bus. The CPU samples the data from the memory on the data bus with the rising edge of the clock of state T3 and this same edge is used by the CPU to turn off the $\overline{RD}$ and $\overline{MRQ}$ signals. Thus the data has already been sampled by the CPU before the $\overline{RD}$ signal becomes inactive. Clock state T3 and T4 of a fetch cycle are used to refresh dynamic memories. (The CPU uses this time to decode and execute the fetched instruction so that no other operation could be performed at this time). During T3 and T4 the lower 7 bits of the address bus contain a memory refresh address and the $\overline{RFSH}$ signal becomes active to indicate that a refresh read of all dynamic memories should be accomplished. Notice that a $\overline{RD}$ signal is not generated during refresh time to prevent data from different memory segments from being gated onto the data bus. The $\overline{MREQ}$ signal during refresh time should be used to perform a refresh read of all memory elements. The refresh signal can not be used by itself since the refresh address is only guaranteed to be stable during $\overline{MREQ}$ time.



INSTRUCTION OP CODE FETCH
FIGURE 4.0-1

Figure 4.0-1A illustrates how the fetch cycle is delayed if the memory activates the $\overline{WAIT}$ line. During T2 and every subsequent Tw, the CPU samples the $\overline{WAIT}$ line with the falling edge of Φ. If the $\overline{WAIT}$ line is active at this time, another wait state will be entered during the following cycle. Using this technique the read cycle can be lengthened to match the access time of any type of memory device.

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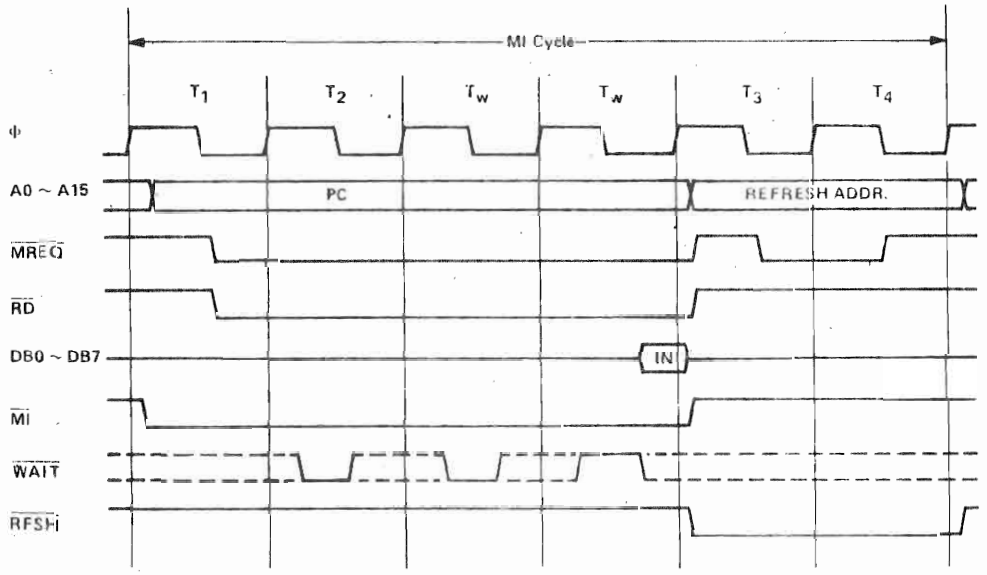
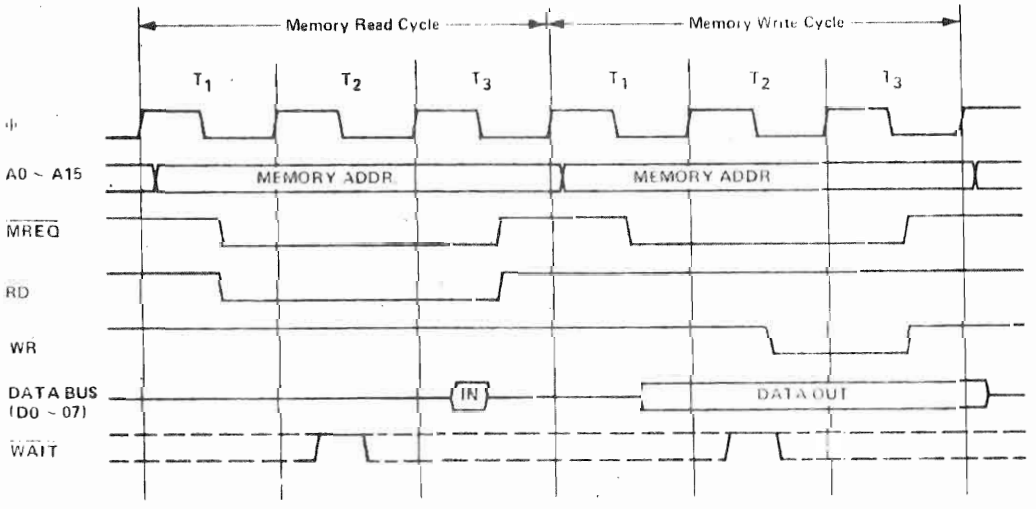
Z80 CPU (cont)



INSTRUCTION OP CODE FETCH WITH WAIT STATES
FIGURE 4.0-1A

MEMORY READ OR WRITE

Figure 4.0-2 illustrates the timing of memory read or write cycles other than an OP code fetch (M1 cycle). These cycles are generally three clock periods long unless wait states are requested by the memory via the WAIT signal. The MREQ signal and the RD signal are used the same as in the fetch cycle. In the case of a memory write cycle, the MREQ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The WR line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory. Furthermore the WR signal goes inactive one half T state before the address and data bus contents are changed so that the overlap requirements for virtually any type of semiconductor memory type will be met.

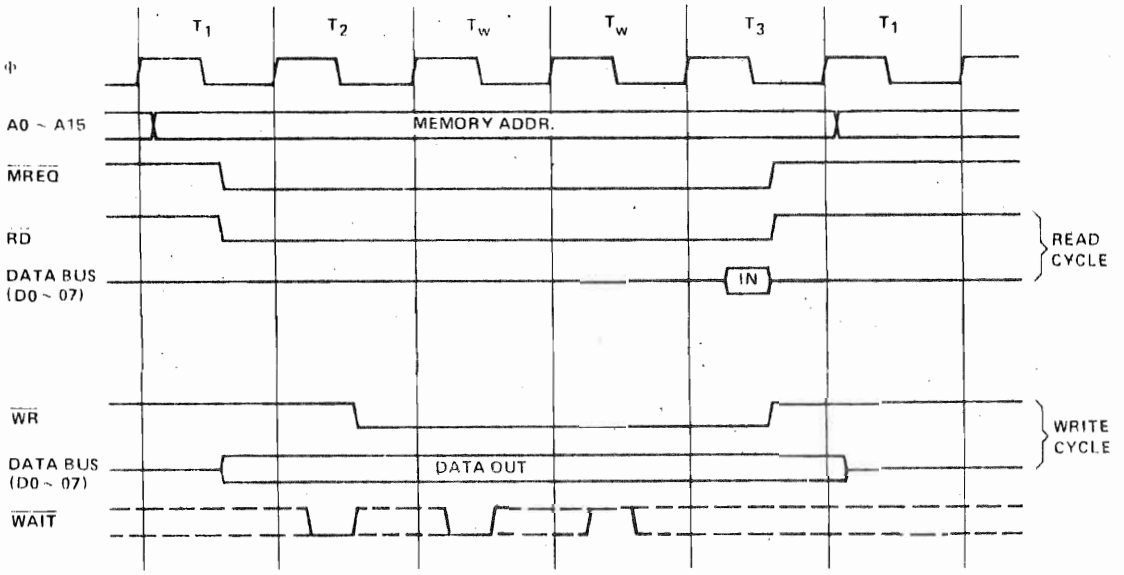


MEMORY READ OR WRITE CYCLES
FIGURE 4.0-2

#443-881

Z80 CPU (cont)

Figure 4.0-2A illustrates how a $\overline{WAIT}$ request signal will lengthen any memory read or write operation. This operation is identical to that previously described for a fetch cycle. Notice in this figure that a separate read and a separate write cycle are shown in the same figure although read and write cycles can never occur simultaneously.



MEMORY READ OR WRITE CYCLES WITH WAIT STATES
FIGURE 4.0-2A

INPUT OR OUTPUT CYCLES

Figure 4.0-3 illustrates an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted. The reason for this is that during I/O operations, the time from when the $\overline{IORQ}$ signal goes active until the CPU must sample the $\overline{WAIT}$ line is very short and without this extra state sufficient time does not exist for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required. Also, without this wait state it is difficult to design MOS I/O devices that can operate at full CPU speed. During this wait state time the $\overline{WAIT}$ request signal is sampled. During a read I/O operation, the $\overline{RD}$ line is used to enable the addressed port onto the data bus just as in the case of a memory read. For I/O write operations, the $\overline{WR}$ line is used as a clock to the I/O port again with sufficient overlap timing automatically provided so that the rising edge may be used as a data clock.

Figure 4.0-3A illustrates how additional wait states may be added with the $\overline{WAIT}$ line. The operation is identical to that previously described.

BUS REQUEST/ACKNOWLEDGE CYCLE

Figure 4.0-4 illustrates the timing for a Bus Request/Acknowledge cycle. The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last clock period of any machine cycle. If the $\overline{BUSRQ}$ signal is active, the CPU will set its address, data and tri-state control signals to the high impedance state with the rising edge of the next clock pulse. At that time any external device can control the buses to transfer data between memory and I/O devices. (This is generally known as Direct Memory Access [DMA] using cycle stealing). The maximum time for the CPU to respond to a bus request is the length of a machine cycle and the external controller can maintain control of the bus for as many clock cycles as is desired. Note, however, that if very long DMA cycles are used, and dynamic memories are being used, the external controller must also perform the refresh function. This situation only occurs if very large blocks of data are transferred under DMA control. Also note that during a bus request cycle, the CPU cannot be interrupted by either a $\overline{NMI}$ or an $\overline{INT}$ signal.

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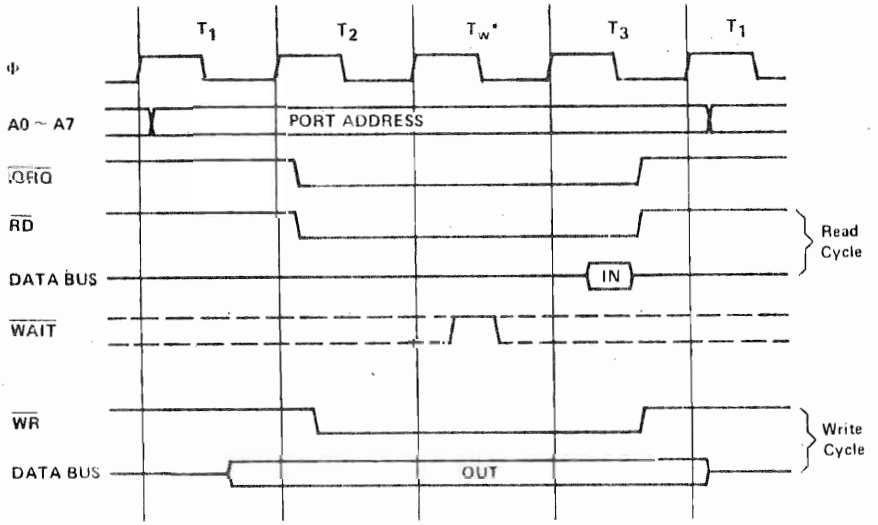
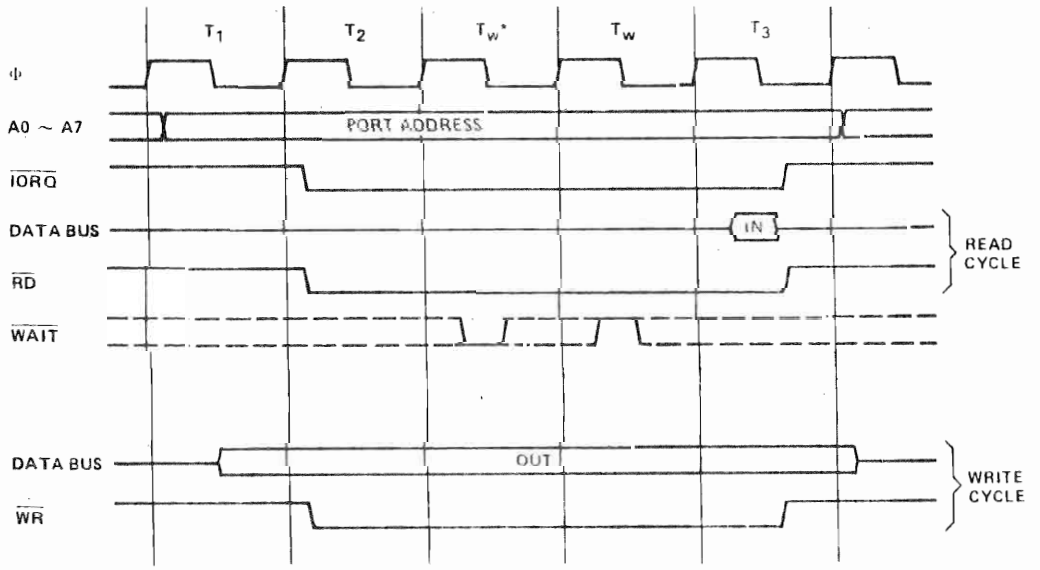
Z80 CPU (cont)



INPUT OR OUTPUT CYCLES
FIGURE 4.0-3

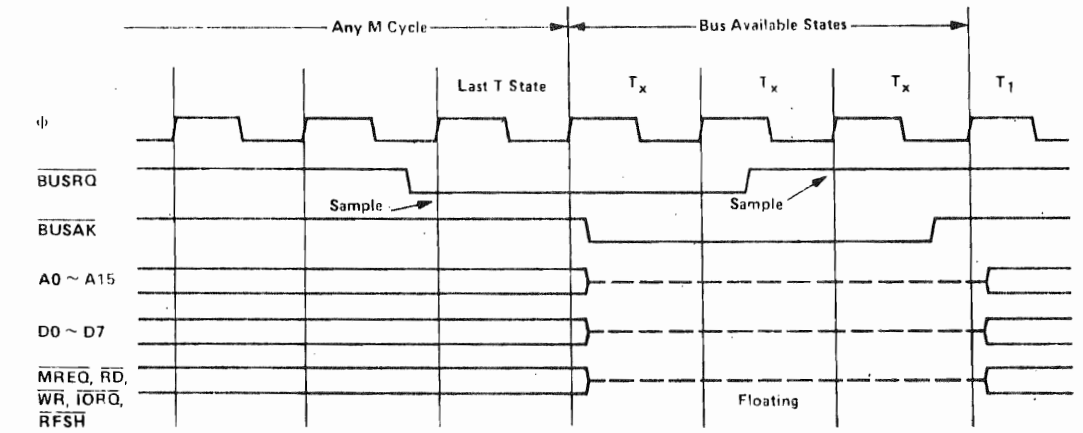


INPUT OR OUTPUT CYCLES WITH WAIT STATES
FIGURE 4.0-3A

* Automatically inserted WAIT state

#443-881

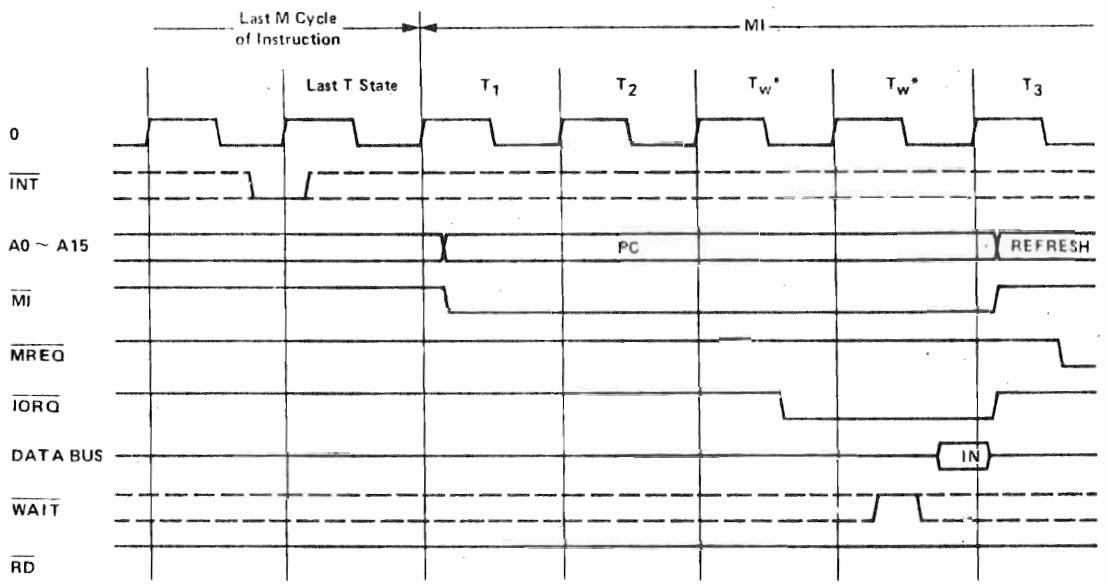
Z80 CPU (cont)



BUS REQUEST/ACKNOWLEDGE CYCLE
FIGURE 4.0-4

INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

Figure 4.0-5 illustrates the timing associated with an interrupt cycle. The interrupt signal (INT) is sampled by the CPU with the rising edge of the last clock at the end of any instruction. The signal will not be accepted if the internal CPU software controlled interrupt enable flip-flop is not set or if the BUSRQ signal is active. When the signal is accepted a special M1 cycle is generated. During this special M1 cycle the IORQ signal becomes active (instead of the normal MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. Notice that two wait states are automatically added to this cycle. These states are added so that a ripple priority interrupt scheme can be easily implemented. The two wait states allow sufficient time for the ripple signals to stabilize and identify which I/O device must insert the response vector. Refer to section 8.0 for details on how the interrupt response vector is utilized by the CPU.

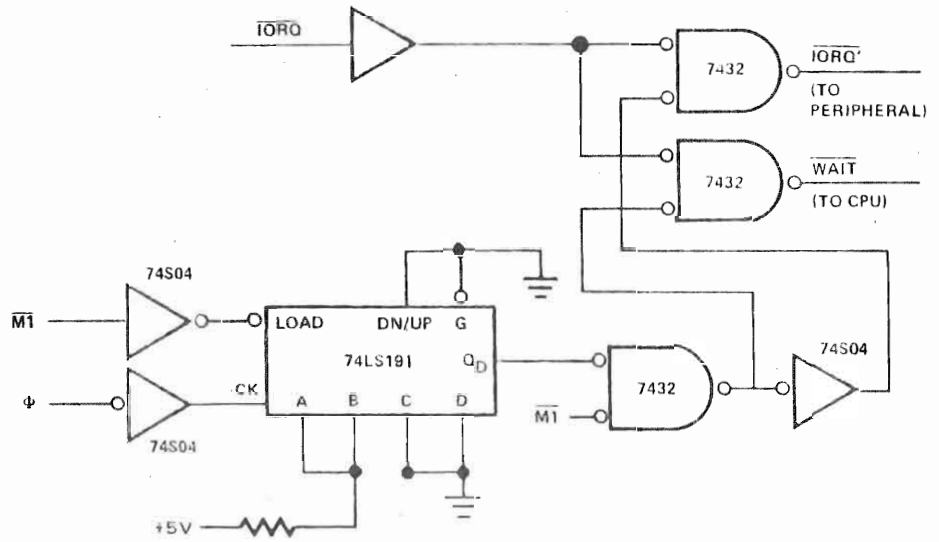


INTERRUPT REQUEST/ACKNOWLEDGE CYCLE
FIGURE 4.0-5

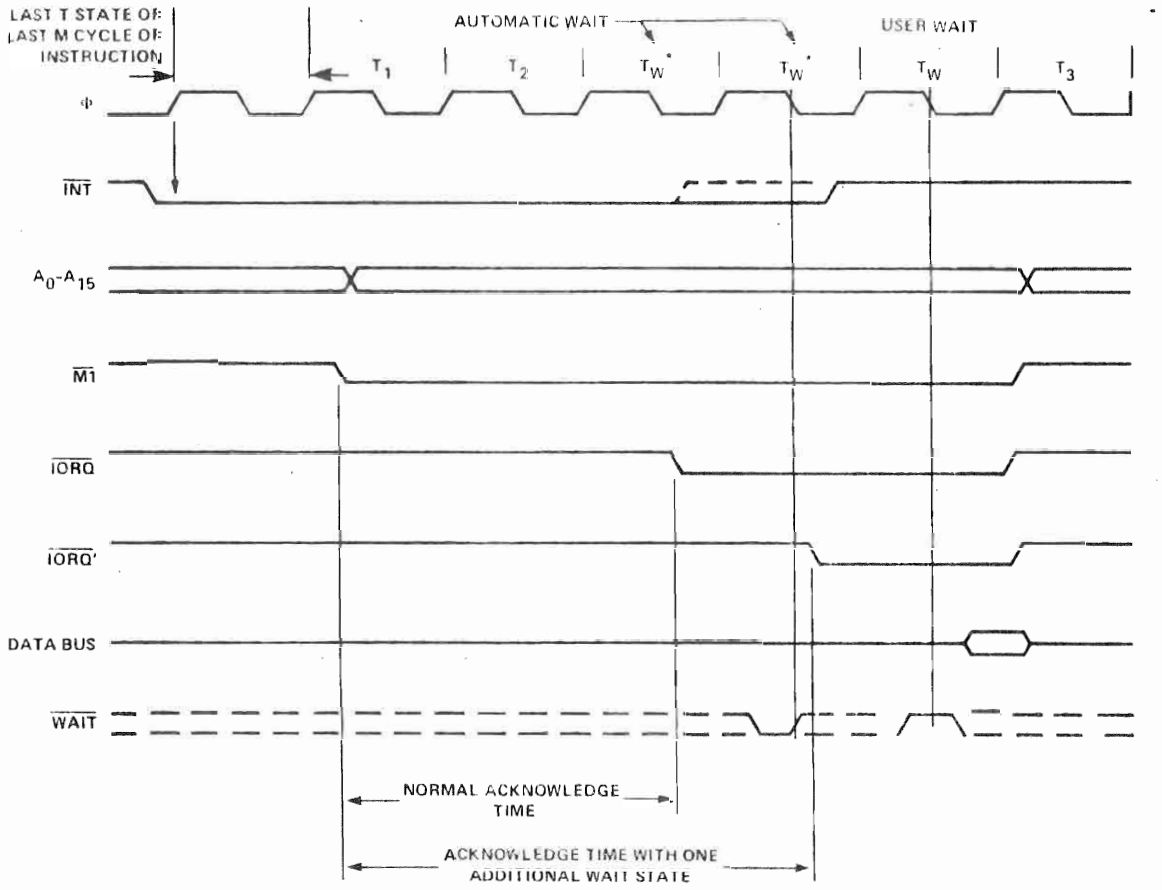
#443-881

Z80 CPU (cont)

Figures 4.0-5A and 4.0-5B illustrate how a programmable counter can be used to extend interrupt acknowledge time. (Configured as shown to add one wait state)



EXTENDING INTERRUPT ACKNOWLEDGE TIME WITH WAIT STATE
FIGURE 4.0-5A



REQUEST/ACKNOWLEDGE CYCLE WITH ONE ADDITIONAL WAIT STATE
FIGURE 4.0-5B

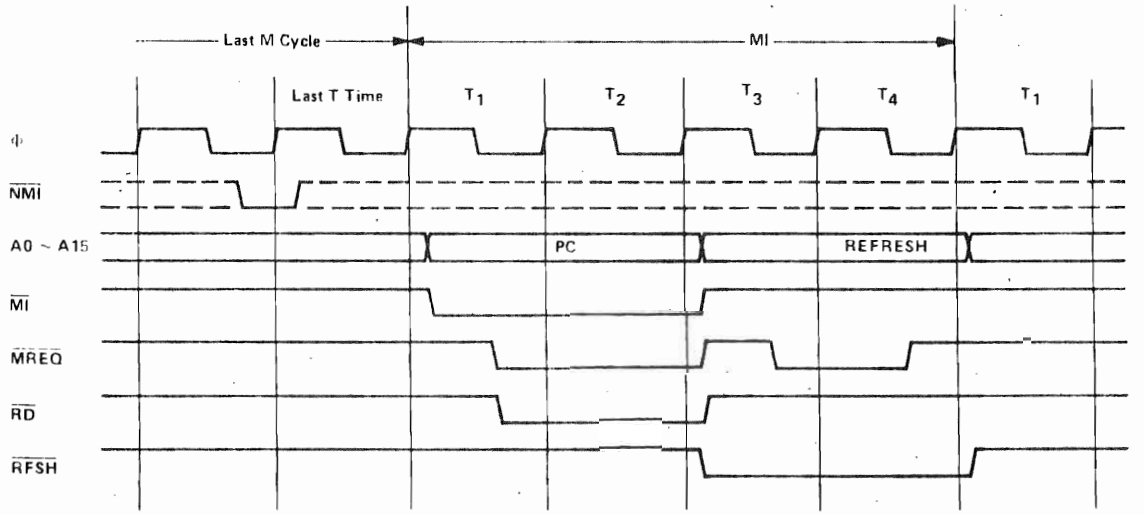
#443-881

NON MASKABLE INTERRUPT RESPONSE

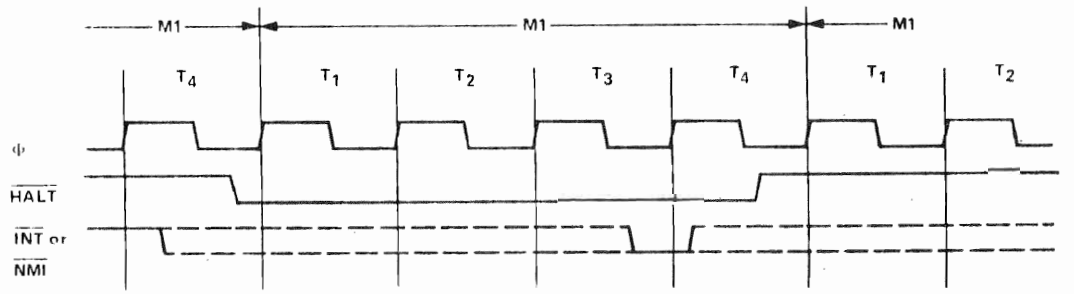
Figure 4.0-6 illustrates the request/acknowledge cycle for the non maskable interrupt. This signal is sampled at the same time as the interrupt line, but this line has priority over the normal interrupt and it can not be disabled under software control. Its usual function is to provide immediate response to important signals such as an impending power failure. The CPU response to a non maskable interrupt is similar to a normal memory read operation. The only difference being that the content of the data bus is ignored while the processor automatically stores the PC in the external stack and jumps to location 0066_H. The service routine for the non maskable interrupt must begin at this location if this interrupt is used.

HALT EXIT

Whenever a software halt instruction is executed the CPU begins executing NOP's until an interrupt is received (either a non maskable or a maskable interrupt while the interrupt flip flop is enabled). The two interrupt lines are sampled with the rising clock edge during each T4 state as shown in figure 4.0-7. If a non maskable interrupt has been received or a maskable interrupt has been received and the interrupt enable flip-flop is set, then the halt state will be exited on the next rising clock edge. The following cycle will then be an interrupt acknowledge cycle corresponding to the type of interrupt that was received. If both are received at this time, then the non maskable one will be acknowledged since it has highest priority. The purpose of executing NOP instructions while in the halt state is to keep the memory refresh signals active. Each cycle in the halt state is a normal M1 (fetch) cycle except that the data received from the memory is ignored and a NOP instruction is forced internally to the CPU. The halt acknowledge signal is active during this time to indicate that the processor is in the halt state.



NON MASKABLE INTERRUPT REQUEST OPERATION
FIGURE 4.0-6



HALT INSTRUCTION IS RECEIVED DURING THIS MEMORY CYCLE

HALT EXIT
FIGURE 4.0-7

#443-881

Z80 CPU (cont)

Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}

I_{cc} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max	Unit
C_Φ	Clock Capacitance	35	pf
C_{IN}	Input Capacitance	5	pf
C_{OUT}	Output Capacitance	10	pf

Z80-CPU Ordering Information

C - Ceramic
P - Plastic
S - Standard 5V ±5% 0° to 70°C
E - Extended 5V ±5% -40° to 85°C
M - Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max	Unit
C_Φ	Clock Capacitance	35	pf
C_{IN}	Input Capacitance	5	pf
C_{OUT}	Output Capacitance	10	pf

Z80A-CPU Ordering Information

C Ceramic
P Plastic
S Standard 5V ±5% 0° to 70°C

A.C. Characteristics

Z80 CPU (cont)

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	4	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[F]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF
	$t_{f(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\bar{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\bar{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(MRL)}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(MRH)}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(WRL)}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(NML)}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{f(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 210$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 80$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(\overline{WR}L)} = t_c - 40$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

NOTES

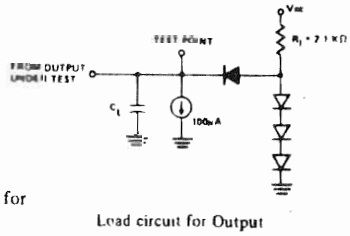
A Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D Output Delay vs. Loaded Capacitance
TA = 70 C Vcc = +5V +5%
Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

I Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum



Load circuit for Output

A.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	250	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110	[12]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50pF
	$t_{f(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[11]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{s\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{s\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 50$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 170$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 70$

[8] $t_{w(\overline{MRL})} = t_c - 30$

[9] $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$

[10] $t_{w(\overline{WRL})} = t_c - 30$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

NOTES

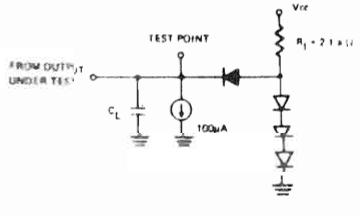
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum



Load Circuit for Output

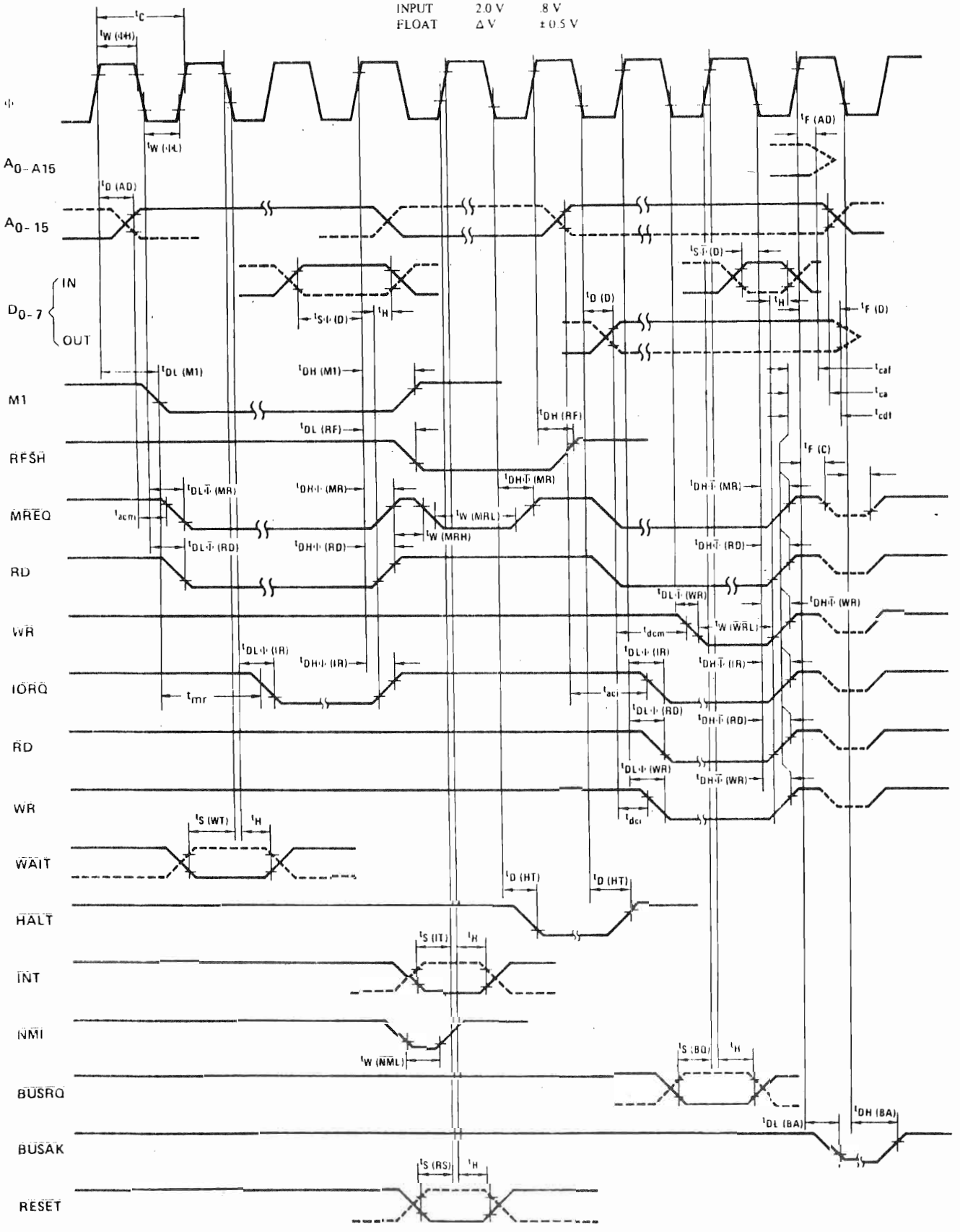
A.C. Timing Diagram

#443-881

Z80 CPU (cont)

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{cc} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	± 0.5 V



#443-885

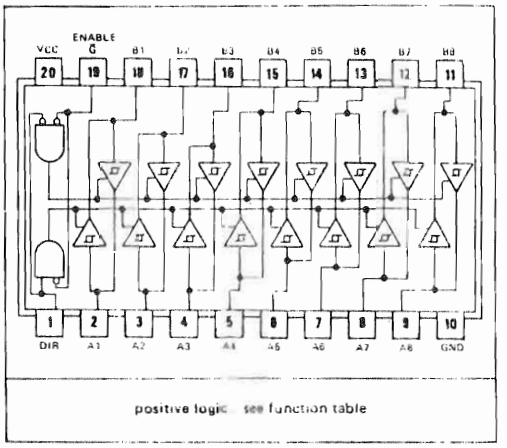
74LS245

TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns
- Typical Enable/Disable Times . . . 17 ns

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	−12 mA
SN74LS245	24 mA	−15 mA

SN54LS245 . . . J PACKAGE
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

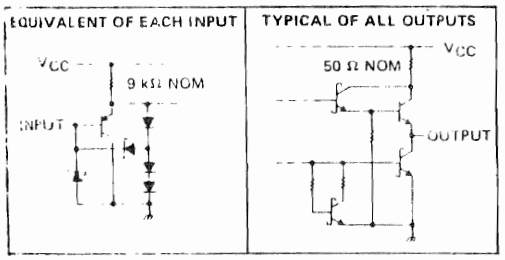
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS245 . . . . . −55°C to 125°C
SN74LS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#443-885

74LS245 (cont)

TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

REVISED AUGUST 1977

recommended operating conditions

PARAMETER	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS245			SN74LS245			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{G}$ at 2 V	V_O = 2.7 V			10			10	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Total, outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF,	R_L = 667 Ω, See Note 2		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output				8	12	ns
t_{PZL}	Output enable time to low level				27	40	ns
t_{PZH}	Output enable time to high level				25	40	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	R_L = 667 Ω, See Note 2		15	25	ns
t_{PHZ}	Output disable time from high level				15	25	ns

NOTE 2: Load circuit and waveforms are shown on page 3-11.

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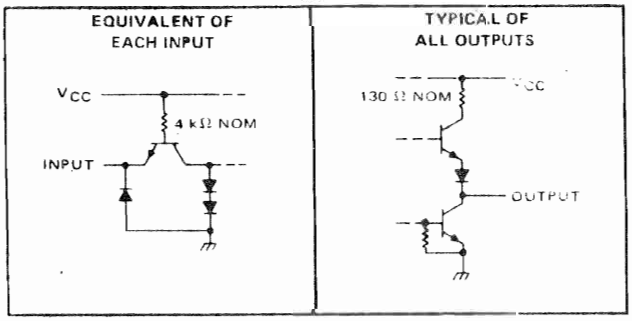
74LS86

TTL MSI

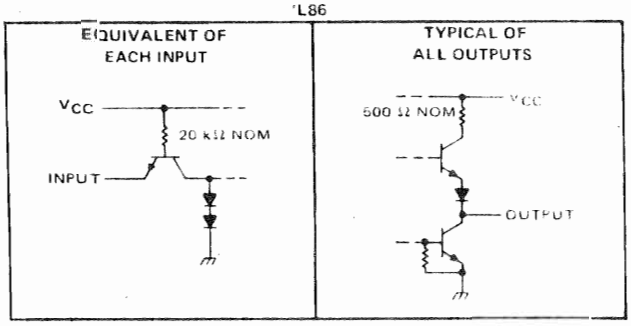
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

schematics of inputs and outputs

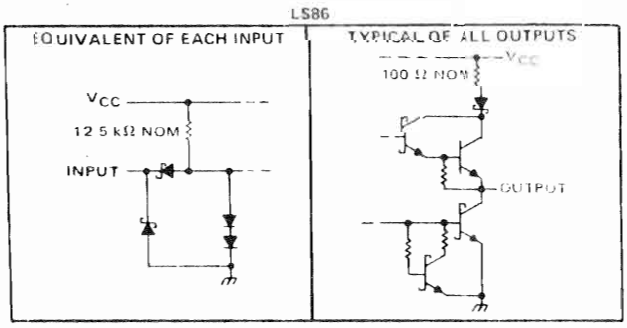
'86



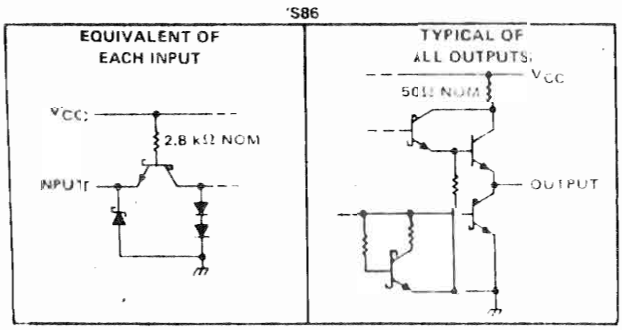
'L86



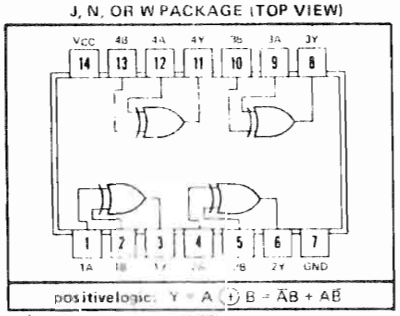
LS86



'S86

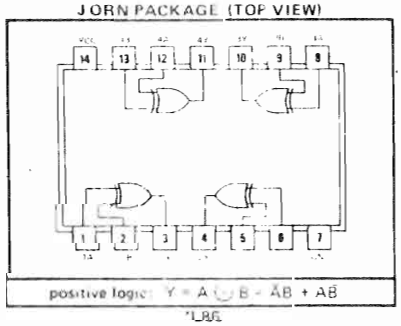


'86, 'LS86, 'S86
J, N, OR W PACKAGE (TOP VIEW)



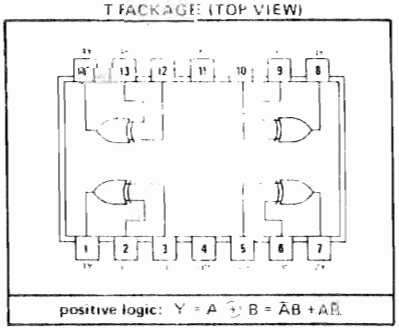
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

'L86
J OR N PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

'LS86
T PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	35 ns	15 mW
LS86	10 ns	30.5 mW
S86	7 ns	250 mW

443-891

74LS86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS86 . . . . . −55°C to 125°C
SN74LS86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS86			SN74LS86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS86			SN74LS86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.6			−0.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		6.1	10		6.1	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 7		10	17	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	17	ns
t_{PHL}					10	17	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 149.

#443-892

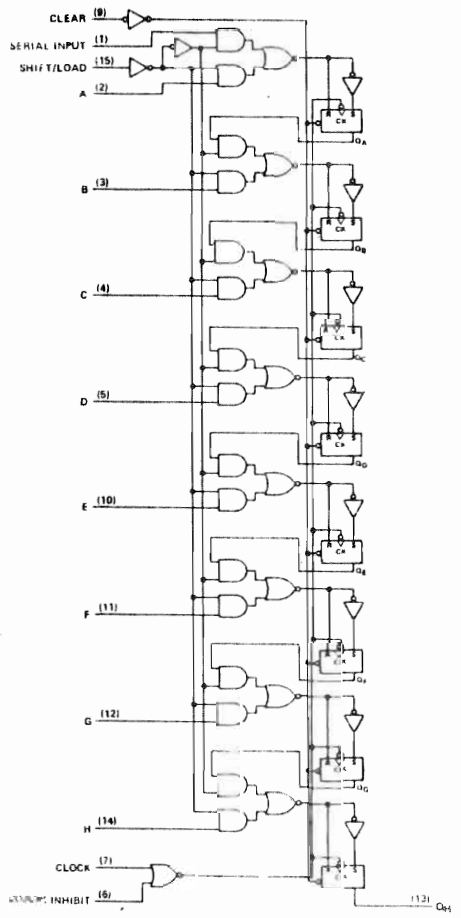
74LS166

TYPES SN54166, SN54LS166, SN74166, SN74LS166
8-BIT SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

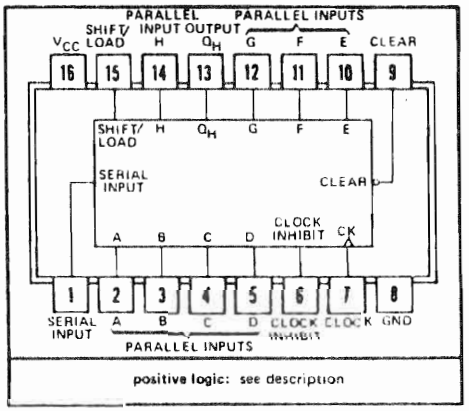
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz	360 mW
'LS166	35 MHz	110 mW

functional block diagram



. . . dynamic input activated by transition from a high level to a low level.

SN54166, SN54LS166 . . . J OR W PACKAGE
SN74166, SN74LS166 . . . J OR N PACKAGE
(TOP VIEW)



description

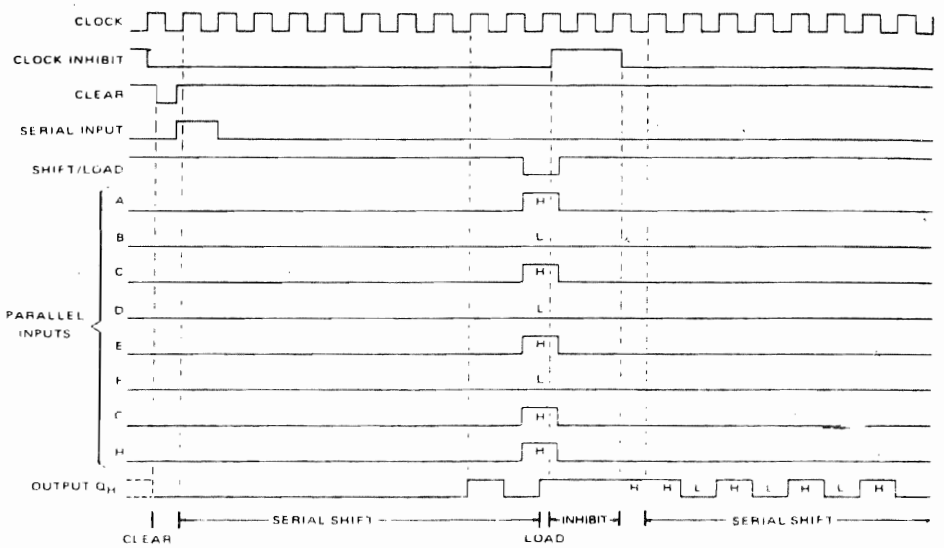
The '166 and 'LS166 8-bit shift registers are compatible with most other TTL and DTL logic families. All '166 and 'LS166 inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

#443-892
74LS166 (cont)

TYPES SN54166, SN54LS166, SN74166, SN74LS166
8-BIT SHIFT REGISTERS

typical clear, shift, load, inhibit, and shift sequences



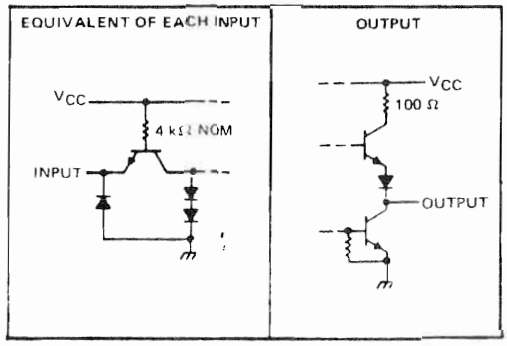
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

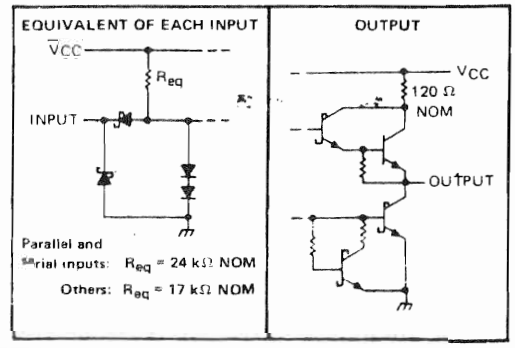
See explanation of function tables on page 3-8.

schematics of inputs and outputs

'166



'LS166



#443-892

74LS166 (cont)

TYPES SN54LS166,SN74LS166
8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS166 . . . . . −55°C to 125°C
SN74LS166 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS166			SN74LS166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS166			SN74LS166			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			32	38		22	38	mA

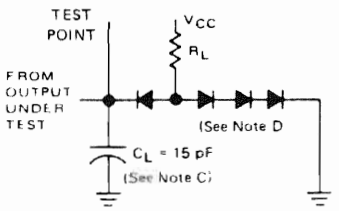
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 3. With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	24	35	ns

#443-892
74LS166 (cont)

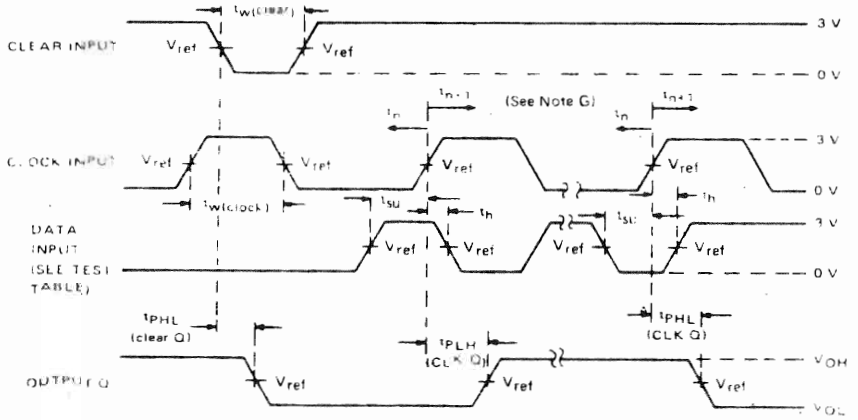
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTE A. All pulse generators have the following characteristics: Z_{out} = 50 Ω; for '166, $t_r \leq 7$ ns and $t_f \leq 7$ ns; for 'LS166, t_r = 15 ns and t_f = 6 ns.

B. The clock pulse has the following characteristics: $t_{w(clock)}$ = 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)}$ = 20 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N3064 or 1N916.

E. A clear pulse is applied prior to each test.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

G. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

H. For '166 V_{ref} = 1.5 V; for 'LS166 V_{ref} = 1.3 V.

FIGURE 1

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP 54/7474

SPEED/PACKAGE AVAILABILITY

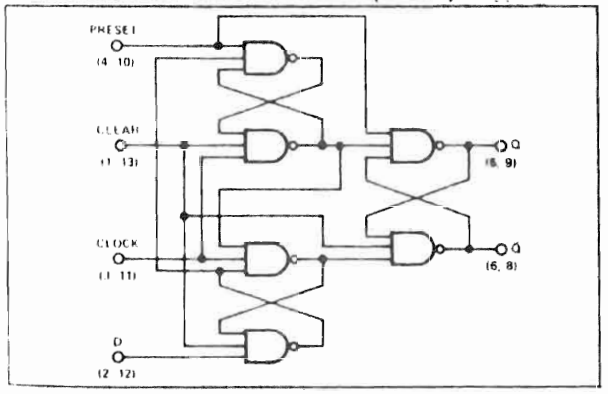
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

DESCRIPTION

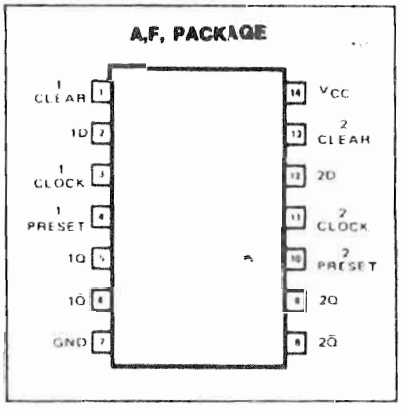
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

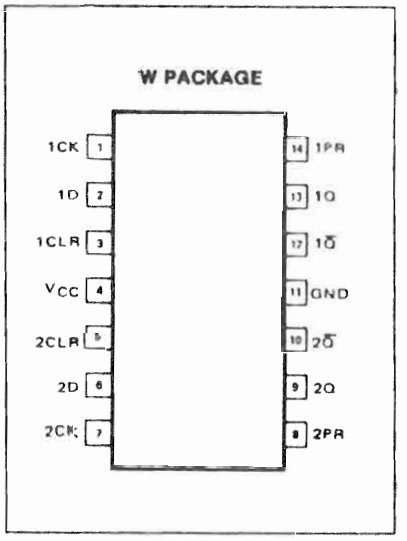
Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION





TRUTH TABLE (Each Flip-Flop)

	Inputs			Outputs	
Preset	Clear	Clock	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state) L = low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

#443-730/#443-900
74LS74/74S74(cont)

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP - 54/7474

SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	25		35	43		25	33		75	90		MHz
$t_{w(Clock)}$	Width of clock input pulse									25						
	Clock high			30			15						6			ns
	Clock low			37			13.5						7.3			
$t_{w(Clear}$	Width of clear input pulse			30			25			25			7			ns
$t_{w(Preset)}$	Width of preset input pulse			30			25			25			7			ns
t_{Setup}	Input setup time			20↑	15								3↓			ns
	High level						10↑			25						
	Low level						15↑			20						
t_{Hold}	Input hold time			5↑	2		5↑			5			2↓			ns
Propagation delay time																
t_{PLH}	Low-to-high	Clear, Preset				25			20		8	25		5	6 CLK=1	ns
														8	13.5 CLK=0	
t_{PHL}	High-to-low					40			30		16	40		5	8	
t_{PHL}	Low-to-high	Clock		10	14	25	4	8.5	15		8	25		7	9	ns
t_{PHL}	High-to-low			10	20	40		13	20		16	40		7	9	

Load circuit and typical waveforms are shown at the front of section.

#443-730/#443-900
74LS74/74S74 (cont)

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: T_A = 25°C (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	
t_{PLH}	Propagation Delay, Set or Clear to Output			10	15	ns	Fig. 2	
t_{PHL}		$\overline{CP}$ = L		18	24			
t_{PHL}		$\overline{CP}$ = H		26	35			

AC SET-UP REQUIREMENTS: T_A = 25°C (See Page 4-51 for Waveforms)

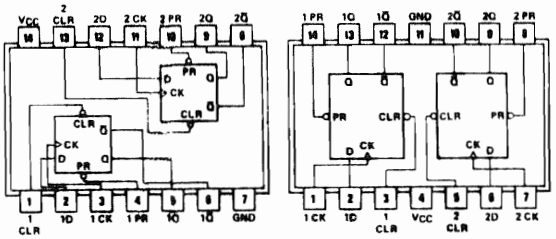
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	10	6		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−4		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	14		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−6		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)

SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{setup}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_{hold}			5↑			0↓			5↑			6↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			*−1.5			*−1.5			*−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1			1			1	mA
I_{IH}	High-level input current	D, J, K, or $\bar{R}$	V_{CC} = MAX, V_I = 2.4 V			40			40			40			40			40			40	μA
		Clear				80			80			120			160			160			80	
		Preset				80			80			80			80			160			80	
		Clock				40			80			80			80			40			120	
I_{IL}	Low-level input current	D, J, K, or $\bar{R}$	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6			−1.6			−1.6			−1.6	mA
		Clear				−3.2			−3.2			−3.2			−4.8			−3.2			−3.2	
		Preset				−3.2			−3.2			−1.6			−3.2			−3.2			−3.2	
		Clock				−1.6			−3.2			−3.2			−3.2			−1.6			−4.8	
I_{OS}	Short-circuit output current♦	Series 54	V_{CC} = MAX	−20		−57	−20		−57	−20		−57	−30		−85	−20		−57	−20		−57	mA
		Series 74		−18		−57	−18		−57	−18		−57	−30		−85	−18		−57	−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		13	26		10	20		8.5	15		9	15		20	34		14	20.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and is grounded for all the others.
*The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

#443-730/#443-900
74LS74/74S74(cont)

recommended operating conditions

		SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−1000			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		12			12			15			12			ns
	Clock low		28			28			13.5			28			
	Clear or preset low		16			16			25			16			
Setup time, t_{setup}	High-level data		0↑			0↑			10↑			0↑			ns
	Low-level data		0↑			0↑			15↑			0↑			
Hold time, t_{hold}			0↓			0↓			5↑			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			2			2			V
V_{IL} Low-level input voltage						0.8			0.8			0.8			0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −8 mA				*−1.5			*−1.5			*−1.5			*−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1			1	mA
I_{IH} High-level input current	D, J, or K	V_{CC} = MAX, V_I = 2.4 V				50			50			50			50	μA
	Clear								100			150			200	
	Preset					150			100			100			100	
	Clock					100			50			100			100	
I_{IL} Low-level input current	D, J, or K	V_{CC} = MAX, V_I = 0.4 V				−2			−2			−2			−2	mA
	Clear								−4			−4			−8	
	Preset					−6			−4			−2			−4	
	Clock					−4			−2			−4			−4	
I_{OS} Short-circuit output current#		V_{CC} = MAX		−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1	Series 54H		19	30		16	25		15	21		16	25	mA
			Series 74H		19	30		16	25		15	25		16	25	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
#Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
*The input clamp voltage specification is effective for Series 54H/74H parts date-coded 7332 or higher.

#443-730/#443-900
'74LS74/74S74 (cont)

recommended operating conditions

		SERIES 54L/74L	'L71			'L72, 'L73			'L74			'L78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54L	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74L	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		Series 54L			−100			−100			−100			−100	μA
		Series 74L			−200			−200			−200			−200	
Low-level output current, I_{OL}		Series 54L			2			2			2			2	mA
		Series 74L			3.6			3.6			3.6			3.6	
Pulse width, t_w	Clock high		200			200			200			200			ns
	Clock low		200			200			200			200			
	Clear or preset low		100			100			100			100			
Setup time, t_{setup}			0↑			0↑			50↑			0↑			ns
Hold time, t_{hold}			0↓			0↓			0↑			0↓			ns
Operating free-air temperature, T_A		Series 54L	−55		125	−55		125	−55		125	−55		125	°C
		Series 74L	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'L71			'L72, 'L73			'L74			'L78			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			V
V_{IL}	Low-level input voltage	Clock input					0.6			0.6			0.7			0.6	V
		All other inputs					0.7			0.7			0.7			0.7	
V_{OH}	High-level output voltage	Series 54L	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.3		2.4	3.3		2.4	3.3		2.4	3.3		V
		Series 74L	V_{IL} = V_{IL} max,	I_{OH} = MAX	2.4	3.2		2.4	3.2		2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	Series 54L	V_{CC} = MIN,	V_{IH} = 2 V,		0.15	0.3		0.15	0.3		0.15	0.3		0.15	0.3	V
		Series 74L	V_{IL} = V_{IL} max,	I_{OL} = MAX		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	
I_I	Input current at maximum input voltage	R, S, J, K, or D	V_{CC} = MAX,	V_I = 5.5 V			100			100			100			100	μA
		Clear					200			200			300			400	
		Preset					200			200			200			200	
		Clock					200			200			200			400	
I_{IH}	High-level input current	R, S, J, K, or D	V_{CC} = MAX,	V_I = 2.4 V			10			10			10			10	μA
		Clear					20			20			30			40	
		Preset					20			20			20			20	
		Clock					−200			−200			20			−400	
I_{IL}	Low-level input current	R, S, J, K, or D	V_{CC} = MAX,	V_I = 0.3 V			−0.18			−0.18			−0.18			−0.18	mA
		Clear					−0.36			−0.36			−0.36			−0.72	
		Preset					−0.36			−0.36			−0.18			−0.36	
		Clock					−0.36			−0.36			−0.36			−0.72	
I_{OS}	Short-circuit output current		V_{CC} = MAX		−3		−15	−3		−15	−3		−15	−3		−15	mA
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX,	See Note 1		0.76	1.44		0.76	1.44		0.8	1.5		0.76	1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

recommended operating conditions

		SERIES 54LS/74LS	'LS73, 'LS113			'LS74			'LS76, 'LS112			'LS78, 'LS114			'LS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54LS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74LS	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−400			−400	μA
Low-level output current, I_{OL}		Series 54LS			4			4			4			4			4	mA
		Series 74LS			8			8			8			8			8	
Clock frequency, f_{clock}			0		30	0		25	0		30	0		30	0		25	MHz
Pulse width, t_w	Clock high		20			25			20			20			25			ns
	Preset or clear low		25			25			25			25			25			
Setup time, t_{setup}	High-level data		20↓			25↑			20↓			20↓			20↑			ns
	Low-level data		20↓			20↑			20↓			20↓			20↑			
Hold time, t_{hold}			0↓			5↑			0↓			0↓			5↑			ns
Operating free-air temperature, T_A		Series 54LS	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74LS	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'LS73, 'LS113			'LS74			'LS76, 'LS112			'LS78, 'LS114			'LS109			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			2			V
V_{IL}	Low-level input voltage	Series 54LS					0.7			0.7			0.7			0.7			0.7	V
		Series 74LS					0.8			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OL} = MAX		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1			0.1			0.1			0.1	mA
		Clear					0.3			0.3			0.3			0.6			0.4	
		Preset					0.3			0.2			0.3			0.3			0.2	
		Clock					0.4			0.2			0.4			0.8			0.2	
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 2.7 V			20			20			20			20			20	μA
		Clear					60			60			60			120			80	
		Preset					60			40			60			60			40	
		Clock					80			40			80			160			40	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 0.4 V			−0.36			−0.4			−0.36			−0.36			−0.4	mA
		Clear					−0.8			−1.2			−0.8			−1.6			−1.6	
		Preset					−0.8			−0.8			−0.8			−0.8			−0.8	
		Clock					−0.72			−0.8			−0.72			−1.44			−0.8	
I_{OS}	Short-circuit output current♦	Series 54LS	V_{CC} = MAX		−8		−40	−8		−40	−8		−40	−8		−40	−8		−40	mA
		Series 74LS			−5		−42	−5		−42	−5		−42	−5		−42	−5		−42	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX,	See Note 1		2	4		2	4		2	4		2	4		2	4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

443-730
SN74LS74

recommended operating conditions

		SERIES 54S/74S	'S74			'S112			'S113			'S114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−1			−1			−1			−1	mA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		6			6			6			6			ns
	Clock low		7.3			6.5			6.5			6.5			
	Clear or preset low		7			8			8			8			
Input setup time, t_{setup}	High-level data		3↑	10		3↓			3↓			3↓			ns
	Low-level data		3↑	12		3↓			3↓			3↓			
Input hold time, t_{hold}			2↑			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54S	−55		125	−55		125	−55		125	−55		125	°C
		Series 74S	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'S74			'S112			'S113			'S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	Series 54S	V_{CC} = MIN, V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74S	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	J, K, or D	V_{CC} = MAX, V_I = 2.7 V			50			50			50			50	μA
		Clear				150			100						200	
		Preset				100			100			00			100	
		Clock				100			100			00			200	
I_{IL}	Low-level input current	J, K, or D	V_{CC} = MAX, V_I = 0.5 V			−2			−1.6			−1.6			−1.6	mA
		Clear				−6			−7						−14	
		Preset				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 1		15	25		15	25		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

#443-906

MC6845

CRT CONTROLLER (CRTC)

The MC6845 CRT Controller performs the interface to raster scan CRT displays. It is intended for use in processor-based controllers for CRT terminals in stand-alone or cluster configurations.

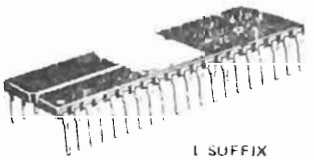
The CRTC is optimized for hardware/software balance in order to achieve integration of all key functions and maintain flexibility. For instance, all keyboard functions, R/W, cursor movements, and editing are under processor control; whereas the CRTC provides video timing and Refresh Memory Addressing.

- Applications include "glass-teletype," smart, programmable, intelligent CRT terminals, video games; information display.
- Alphanumeric, semi-graphic, and full graphic capability
- Fully programmable via processor data bus. Can generate timing for almost any alphanumeric screen density, e.g. 80 x 24, 72 x 64, 132 x 20, etc.
- Single +5 volt supply. TTL/6800 compatible I/O.
- Hardware scroll (paging or by line or by character)
- Compatible with CPU's and MPU's which provide a means for synchronizing external devices.
- Cursor register and compare circuitry.
- Cursor format and blink are programmable.
- Light pen register.
- Line buffer-less operation. No external DMA required. Refresh Memory is multiplexed between CRTC and MPU.
- Programmable interlace or non-interlace scan.
- 14 bit wide refresh address.

MOS

(N-Channel, Silicon-Gate)

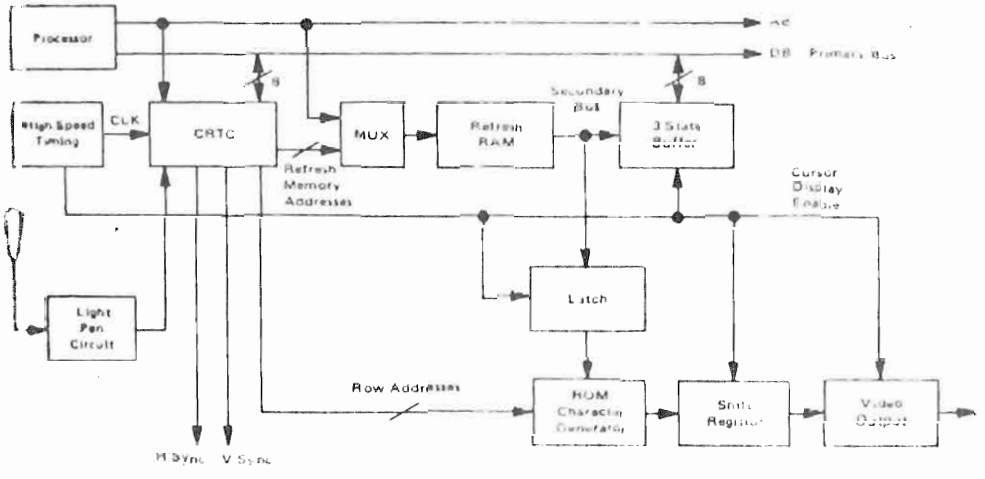
CRT CONTROLLER (CRTC)



L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN
P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 – TYPICAL CRT CONTROLLER APPLICATION



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MC6845 (cont)

SYSTEM BLOCK DIAGRAM DESCRIPTION

As shown in Figure 1, the primary function of the CRTC is to generate refresh addresses (MA0-MA13), row selects (RA0-RA4), and video monitor timing (HSYNC, VSYNC) and Display Enable. Other functions include an internal cursor register which generates a Cursor output when its contents compare to the current Refresh Address. A light-pen strobe input signal allows capture of Refresh Address in an internal light pen register.

All timing in the CRTC is derived from the Clk input. In alphanumeric terminals, this signal is the character rate. Character rate is divided down from video rate by external High Speed Timing when the video frequency is greater than 3 MHz. Shift Register, Latch, and MUX Control signals are also provided by external High Speed Timing.

The processor communicates with the CRTC through a buffered 8-bit Data Bus by reading/writing into the 18-register file of the CRTC.

The Refresh Memory address is multiplexed between the Processor and CRTC. Data appears on a Secondary Bus which is buffered from the processor Primary Bus. A number of approaches are possible for solving contentions for the Refresh Memory.

1. Processor always gets priority.
2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.
3. Synchronize processor by memory wait cycles.
4. Synchronize processor to character rate (See Figure 2). The 6800 MPU family lends itself to this configuration because it has constant cycle lengths. This method provides zero burden on the processor because there is never a contention for memory. All accesses are *"transparent."*

The secondary data bus concept in no way precludes using the Refresh RAM for other purposes. It looks like any other RAM to the Processor. For example, using Approach 4, a 64K byte RAM Refresh Memory could perform refresh and program storage functions transparently.

MAXIMUM RATINGS

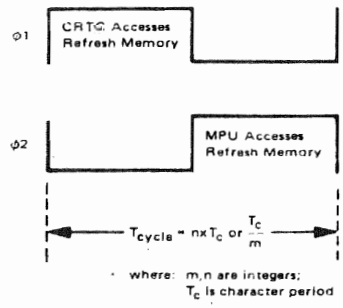
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	-0.3 to +7.0	Vdc
Input Voltage	V_{in}*	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*With respect to V_{SS} (Gnd).

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	V_{CC}	Vdc

FIGURE 2 – TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING 6800 MPU FAMILY



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MC6845 (cont)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0		V_{CC}	Vdc
Input Low Voltage		V_{IL}	-0.3		0.8	Vdc
Input Leakage Current		I_{in}	–	1.0	2.5	μAdc
Three-State (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	-10	2.0	10	μAdc
Output High Voltage (I_{load} = -205 μA) (I_{load} = -100 μA)	D0-D7 Other Outputs	V_{OH}	2.4 2.4	– –	–	Vdc
Output Low Voltage (I_{load} = 1.6 mA)		V_{OL}	–		0.4	Vdc
Power Dissipation		P_D	–	650	–	mW
Input Capacitance	D0-D7 All others	C_{in}	– –		12.5 10	pF
Output Capacitance	All Outputs	C_{out}			10	pF
Minimum Clock Pulse Width, Low		P_{WCL}	160			ns
Minimum Clock Pulse Width, High		P_{WCH}	200	–	–	ns
Clock Frequency		f_c	–	–	2.5	MHz
Rise and Fall Time for Clock Input		t_{cr}, t_{cf}	–	–	20	ns
Memory Address Delay Time		t_{MAD}			160	ns
Raster Address Delay Time		t_{RAD}			160	ns
Display Timing Delay Time		t_{DTD}			300	ns
Horizontal Sync Delay Time		t_{HSD}			300	ns
Vertical Sync Delay Time		t_{VSD}			300	ns
Cursor Display Timing Delay Time		t_{CDD}			300	ns
Light Pen Strobe Minimum Pulse Width		PW_{LPH}	100			ns
Light Pen Strobe Disable Time		t_{LPD1}	–	–	320	ns
		t_{LPD2}		–	0	ns

Note. The light penstrobe must fall to low level before VSYNC pulse rises.

BUS TIMING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
READ/WRITE				
Enable Cycle Time	t_{cycE}	1.0	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	μs
Setup Time, CS and RS valid to enable positive transition	t_{AS}	160	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time (Read) (write)	t_H	10 10	– –	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	–	25	ns
Data Setup Time	t_{DSW}	195	–	ns
Data Access Time	t_{ACC}	–	480	ns

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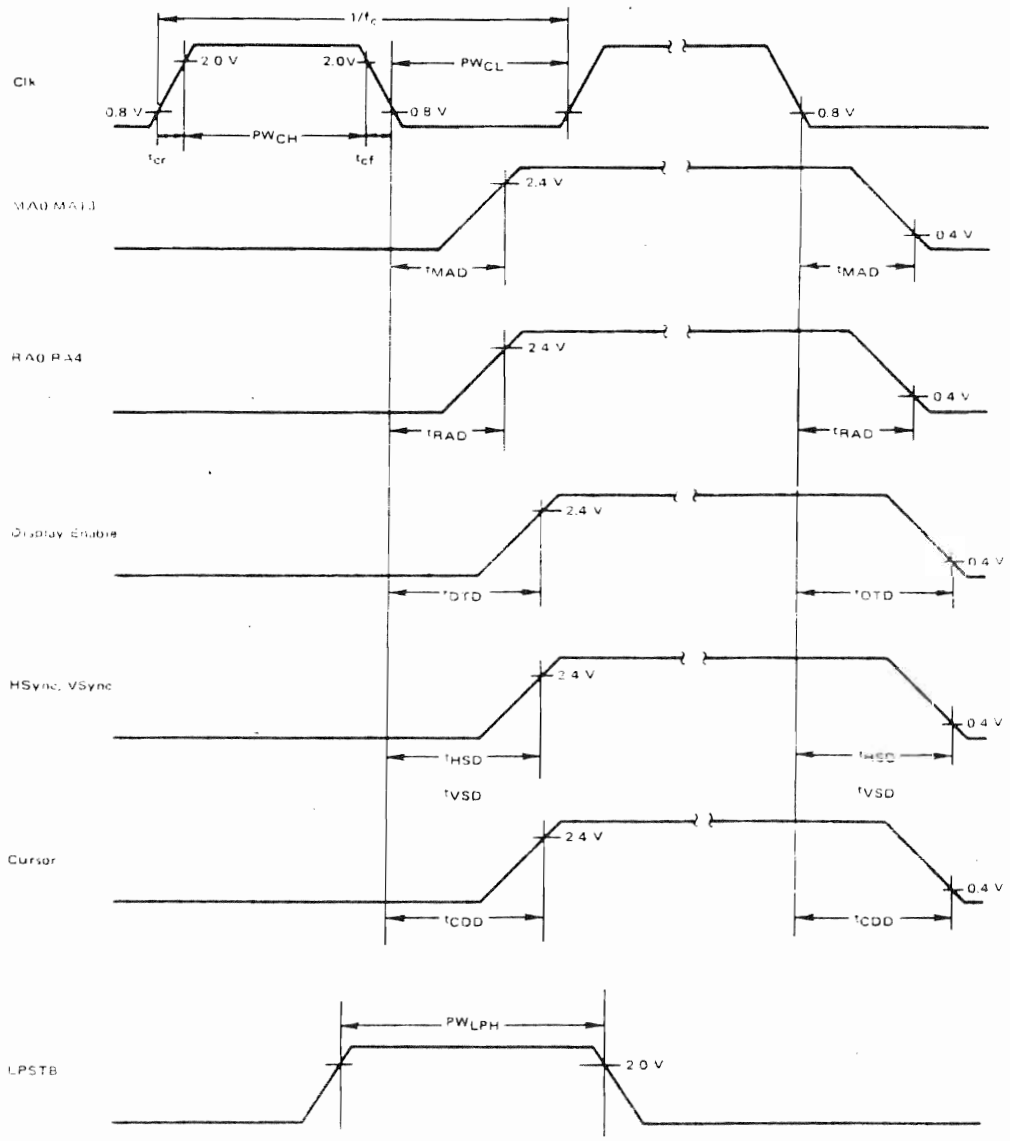
MC6845 (cont)

FIGURE 3 – CRTC TIMING CHART



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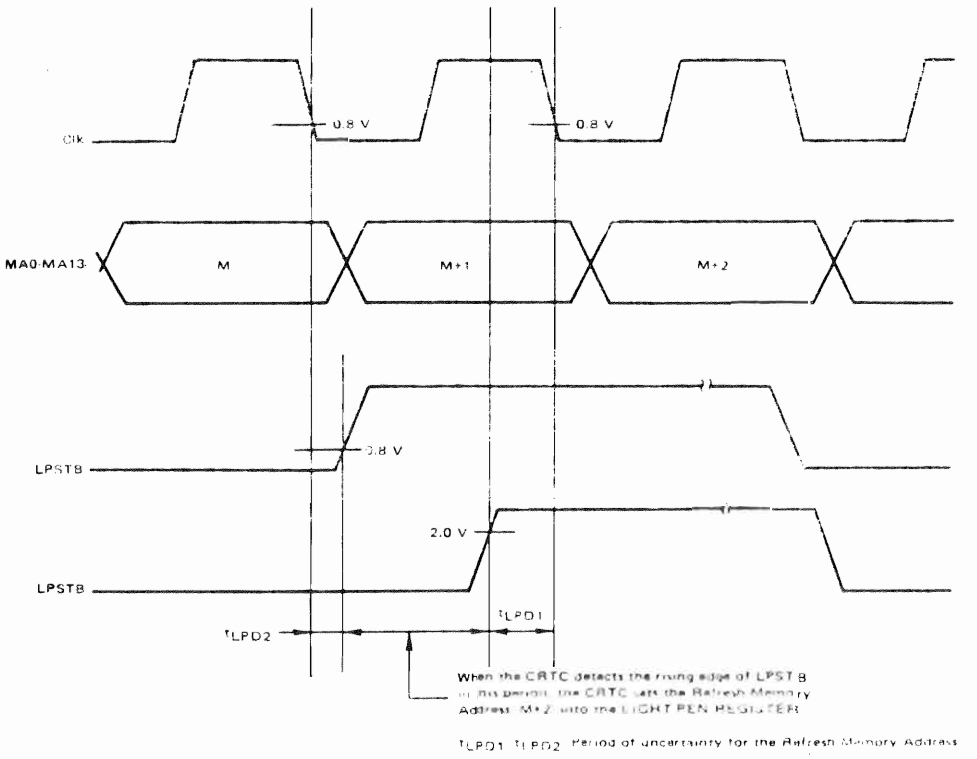
MC6845 (cont)

FIGURE 4 – RELATION BETWEEN LPSTB AND REFRESH MEMORY ADDRESS



t_{LPD1}, t_{LPD2} Period of uncertainty for the Refresh Memory Address

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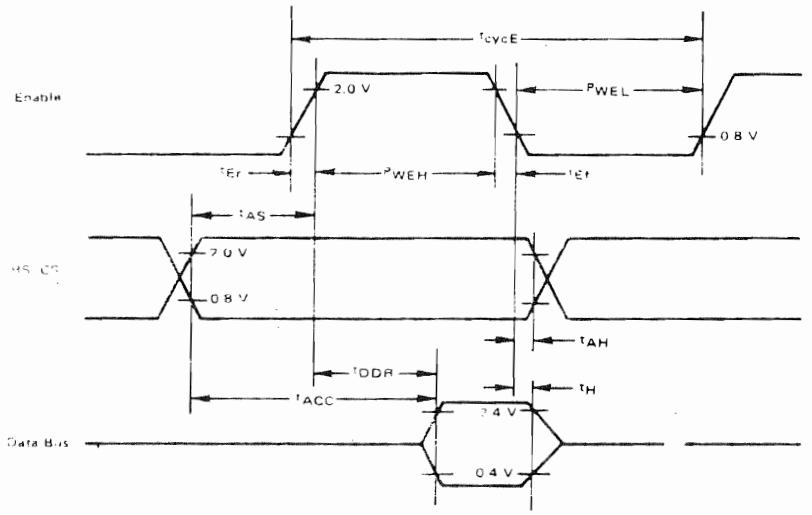
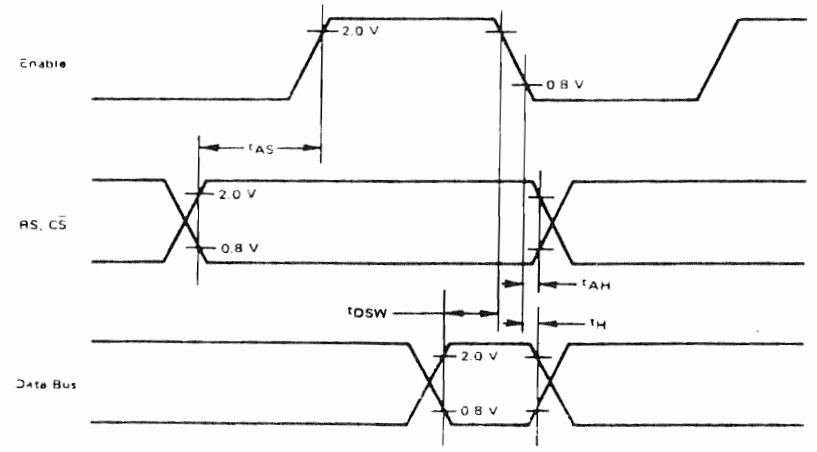
MC6845 (cont)

FIGURE 5 – BUS TIMING CHART

5a – Bus Read Timing (Read Information From CRTC)



5b – Bus Write Timing (Write Information Into CRTC)



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MC6845 (cont)

FIGURE 6 – BUS TIMING TEST LOAD

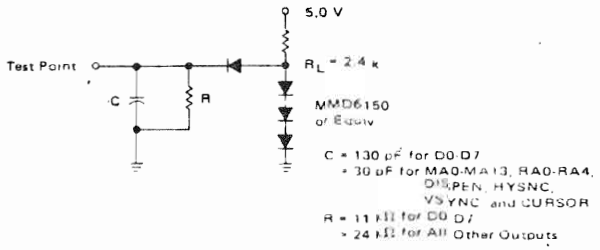
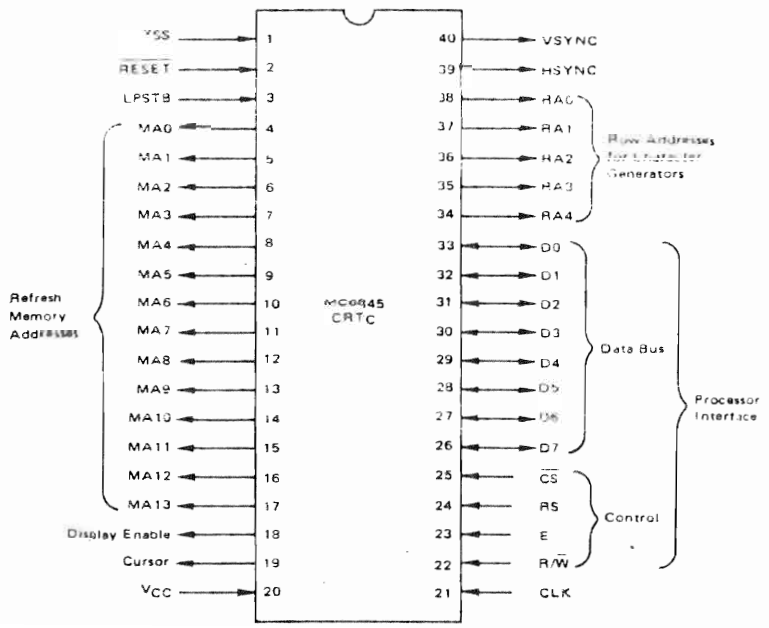


FIGURE 7 – PIN ASSIGNMENT



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MC6845 (cont)

PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) – The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal Register File and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation. A high level on a data pin is a logical "1."

Enable (E) – The Enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

Chip Select ($\overline{CS}$) – The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC when low to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) – The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active low ("0").

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and Display Enable signals.

Vertical Sync (V SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable – This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active Display Area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the Refresh RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Refresh Memory Addresses (MA0-MA13) – These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs drive a TTL load and 30pF. A high level on MA0-MA13 is a logical "1."

Raster Addresses (RA0-RA4) – These 5 outputs from the internal Raster Counter address the Character ROM for the row of a character. These outputs drive a TTL load and 30pF. A high level (on RA0-RA4) is a logical "1."

OTHER PINS

Cursor – This TTL compatible output indicates Cursor Display to external Video Processing Logic. Active high signal.

Clock (CLK) – The CLK TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTR) – This high impedance TTL/MOS compatible input latches the current Refresh Addresses in the Register File. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd

$\overline{RES}$ – The $\overline{RES}$ input is used to Reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into following status:

(A) All the counters in CRTC are cleared and the device stops the display operation.
(B) All the outputs go down to low level.
(C) Control registers in CRTC are not affected and remain unchanged.

This signal is different from other M6800 family in the following functions:

(A) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(B) After $\overline{RES}$ has gone down to low level, output signals of MA0-MA13 and RA0-RA4, synchronizing with CLK low level, goes down to low level. (At least 1 cycle CLK signal is necessary for reset.)
(C) The CRTC starts the Display operation immediately after the release of $\overline{RES}$ signal.

TABLE 1 – CRTC Operating Mode

$\overline{RES}$	LPSTB	OPERATING MODE
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

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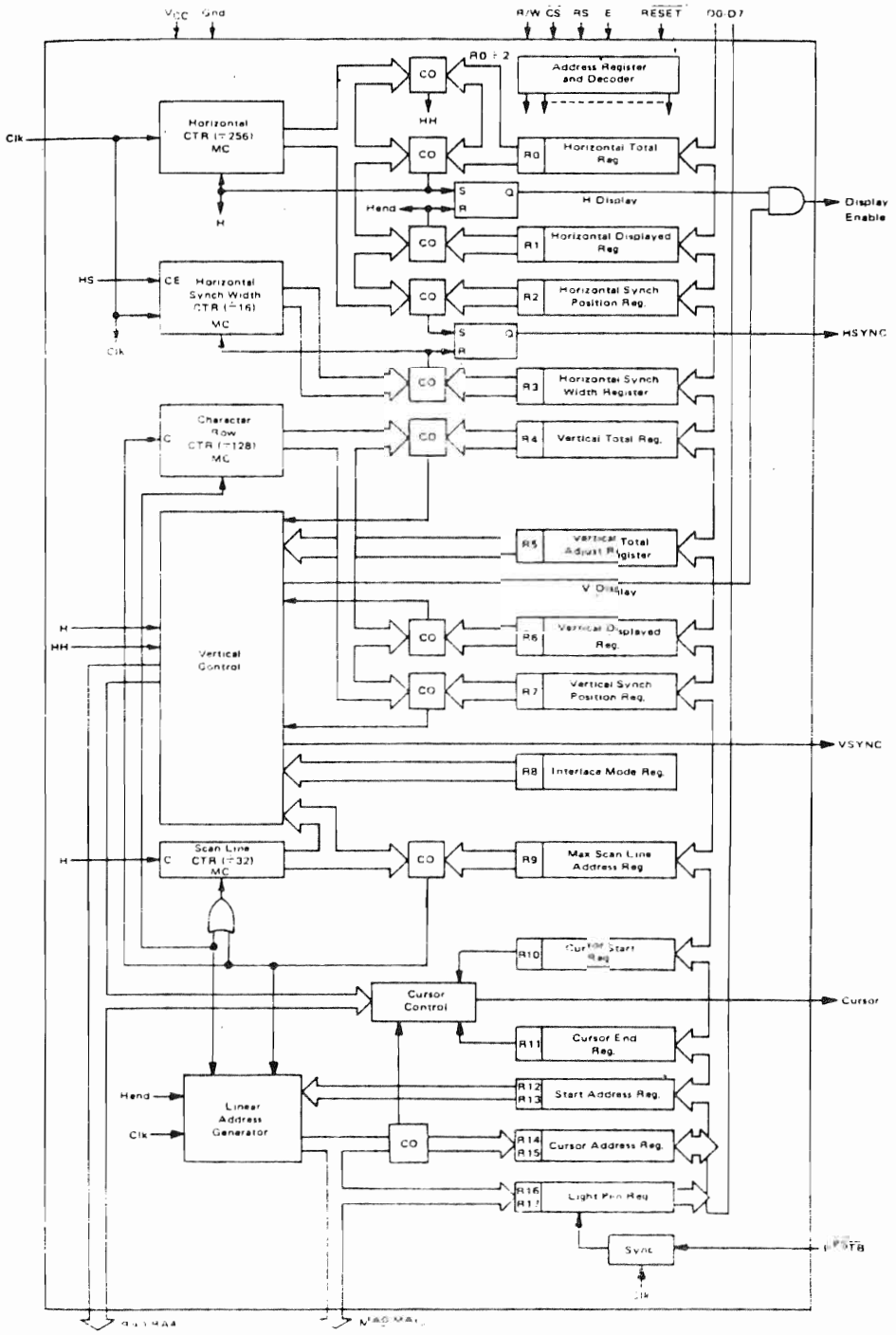
MC6845 (cont)

FIGURE 8 – CRTC FUNCTIONAL BLOCK DIAGRAM



#443-906
MC6845 (cont)

CRTC DESCRIPTION
(Figure 8: CRTC Block Diagram)

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For horizontal timing generation, comparisons result in: 1) Horizontal sync pulse (HS) of a frequency, position, and width determined by the registers, 2) Horizontal Display Signal of a frequency, position, and duration determined by the registers.

The Horizontal counter produces H clock which drives the Scan Line Counter and Vertical Control. The contents of the Raster Counter are continuously compared to the Max Scan Line Address Register. A coincidence resets the Raster Counter and clocks the Vertical Counter.

Comparisons of Vertical Counter contents and Vertical Registers result in: 1) Vertical sync pulse (VS) of a frequency and positon determined by the registers—the width is fixed at 16 raster lines in the vertical control section and is not programmable, 2) Vertical Display of a frequency and position determined by the registers.

The Vertical Control Logic has other functions.

1. Generate row selects, RA0-RA4, from the Raster Count for the corresponding interlace or non-interlace modes.
2. Extend the number of scan lines in the vertical total by the amount programmed in the Vertical Total Adjust Register.

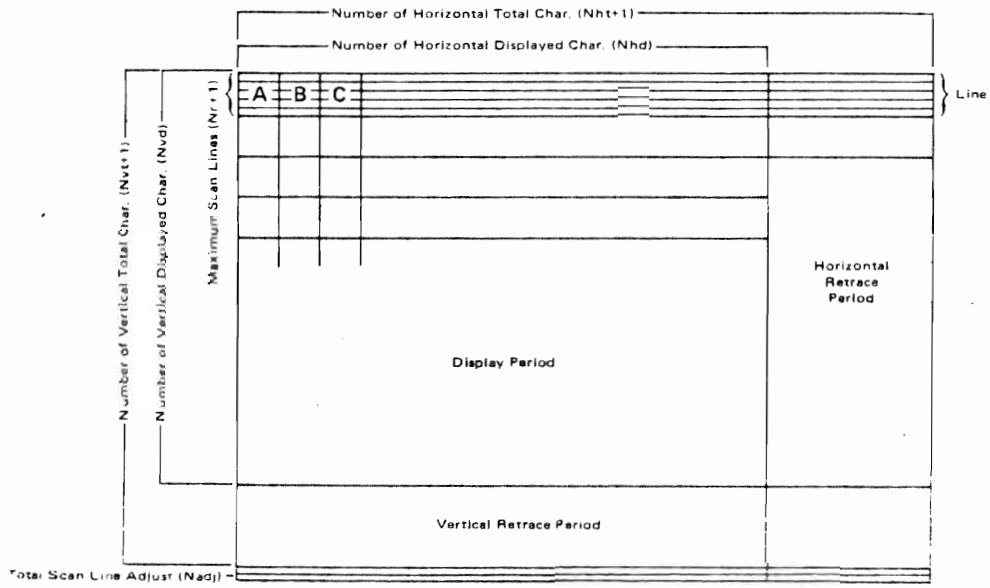
The Linear Address Generator is driven by CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines MA0-MA13, are available for addressing up to four pages of 4K characters, 8 pages of 2K characters, etc. Using the Start Address Register, hardware scrolling through 16K characters is possible. The Linear Address Generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blinking rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the Address Counter to be latched in the Light Pen Register. The contents of the Light Pen Register are subsequently read by the Processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals—R/$\overline{W}$, $\overline{CS}$, RS and E.

FIGURE 9 – ILLUSTRATION OF THE CRT SCREEN FORMAT



#443-906
MC6845 (cont)

REGISTER FILE DESCRIPTION
(See Table 2)

Nineteen registers in the CRTC can be accessed by means of the data bus. Register addressing and lengths are shown in Table 2.

ADDRESS REGISTER

The Address Register is a 5 bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the Register File is accessed.

HORIZONTAL TIMING REGISTERS R0, R1, R2, and R3

Figure 9 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in "character time" units with respect to the reference.

Horizontal Total Register (R0) – This 8 bit write-only register determines the horizontal frequency of HS. It is the total of displayed plus non-displayed character time units minus one.

Horizontal Displayed Register (R1) – This 8 bit write-only register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2) – This 8 bit write-only register determines the horizontal sync position on the horizontal line.

Horizontal Sync Width Register (R3) – This 4 bit write-only register determines the width of the HS pulse. It may not be apparent why this width needs to be programmed. However, consider that all timing widths must be programmed as multiples of the character clock period which varies. If HS width were fixed as an integral number of character times, it would vary with character rate and be out of tolerance for certain monitors. The rate programmable feature allows compensating HS width.

VERTICAL TIMING REGISTERS R4, R5, R6, R7, R8, and R9

The point of reference for vertical registers is the top character position displayed. Vertical registers are programmed in character row times or scan line times.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) – The vertical frequency of VS is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7 bit write-only Vertical Total Register; the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6) – This 7 bit write-only register determines the number of displayed character rows on the CRT screen, and is programmed in character row times.

Vertical Sync Position (R7) – This 7 bit write-only register determines the vertical sync position with respect

TABLE 2 – CRTC INTERNAL REGISTER ASSIGNMENT

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–		–	–								
0	0	X	X	X	X	X	X	Address Register	–	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char	No	Yes								
0	1	0	0	0	1	1	R3	H. Sync Width	Char	No	Yes								
0	1	0	0	1	0	0	R4	Vertical Total	Char Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char Row	No	Yes								
0	1	0	1	0	0	0	R8	Interlace Mode		No	Yes								
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes	X	B	P				(Note 1)	
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)		No	Yes								
0	1	0	1	1	0	1	R13	Start Address (L)		No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)		Yes	Yes								
0	1	0	1	1	1	1	R15	Cursor (L)		Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)		Yes	No								
0	1	1	0	0	0	1	R17	Light Pen (L)		Yes	No								

Note (1) Bit 5 of the Cursor Start Register is used for blink period control, and
Bit 6 is used to select blink or non-blink.

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MC6845 (cont)

to the reference. It is programmed in character row times.

Interlace Mode Register (R8) – This 2 bit write-only register controls the raster scan mode (see Figure 11). When bit 0 and bit 1 are reset, or bit 0 is reset and bit 1 set, the non-interlace raster scan mode is selected. Two interlace modes are available. Both are interlaced 2 fields per frame. When bit 0 is set and bit 1 is reset, the interlace sync raster scan mode is selected. Also when bit 0 and bit 1 are set, the interlace sync and video raster scan mode is selected.

Maximum Scan Line Address Register (R9) – This 5 bit write-only register determines the number of scan lines per character row including spacing. The programmed value is a max address and is one less than the number of scan lines.

OTHER REGISTERS

Cursor Start Register (R10) – This 7 bit write-only register controls the cursor format (see Figure 10). Bit 5 is the blink timing control. When bit 5 is low, the blink frequency is 1/16 of the vertical field rate, and when bit 5 is high, the blink frequency is 1/32 of the vertical field rate. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower 5 bits.

Cursor End Register (R11) – This 5 bit write-only register sets the cursor end scan line.

Start Address Register (H & L) (R12, R13) – Start Address Register is a 14 bit write-only register which determines the first address put out as a refresh address after vertical blanking. It consists of an 8 bit lower register, and a 6 bit higher register.

Light Pen Register (H & L) (R16, R17) – This 14 bit read-only register is used to store the contents of the Address Register (H & L) when the LPSTB input pulses high. This register consists of an 8 bit lower and 6 bit higher register.

Cursor Register (H & L) (R14, R15) – This 14 bit read/write register stores the cursor location. This register consists of an 8 bit lower and 6 bit higher register.

CURSOR

The Cursor Start and End Registers allow a cursor of up to 32 scan lines in height to be placed on any scan lines of the character block as shown in Figure 10. Using Bits 5 & 6 of the Cursor Start Register, the cursor is programmed with blink periods of 16 or 32 times the field period. Optional non-blink and non-display modes can also be selected. When an external 2X blink on characters is required, it may be necessary to perform cursor blink externally as well so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for blinking cursor and externally inverting the video signal with an exclusive-OR.

The cursor is positioned by changing the contents of registers R14 and R15. The cursor can be placed at any of 16K character positions, thus facilitating hardware paging and scrolling through memory without loss of the cursor's original position.

INTERLACE/NON-INTERLACE DISPLAY MODES

An illustration of the 3 raster scan modes of operation is shown in Figure 11. Normal sync mode is non-interlace. In this mode, each scan line is refreshed at the vertical field rate (e.g., 50 or 60 Hz). Frame time is divided into even and odd alternating fields. The horizontal and vertical timing relationship results in the displacement of scan lines in the odd field with respect to the even field. When the same information is painted in both fields, the mode is called "Interlace Sync;" this is a useful mode for enhancing readability by filling in a character. When the even lines of a character are displayed in the even field and the odd lines in the odd field, the mode is called "Interlace Sync and Video." This last mode effectively doubles the character density on a monitor of a given bandwidth. The disadvantage of both interlace modes is an apparent flicker effect, which can be reduced by careful monitor design.

There are restrictions on the programming of CRTC registers for interlace operation:

1) Horizontal total character count, N_{ht} must be odd (i.e., an even number of character times)
2) For Interlace Sync and Video mode only, the max scan line address, N_{sl}, must be odd (i.e., an even number of scan lines)
3) For Interlace Sync and Video mode only, the Vertical Displayed Total characters must be even. The programmed number, N_{vd}, must be *one-half* the actual number required.
4) For Interlace Sync & Video mode only, the Cursor START and Cursor End Registers must both be even or both odd.

LIGHT PEN

The contents of the CRTC Address Counter are strobed into R16/R17 Light Pen Registers on the next high to low CLK transition after LPSTB goes high. In most systems, the light pen signal would also cause a processor interrupt routine to read R16/R17. Slow light pen response requires the processor software to modify the captured address read from R16/R17 by a calibration factor.

PROGRAMMING CONSIDERATIONS

Initialization – Registers R0-R15 must be initialized after power is turned on. The processor normally loads the CRTC registers sequentially from a firmware table. Henceforth, R0-R11 are not changed in most systems. The 6800 program in Table 3 and Figure 12 shows a typical CRTC initialization.

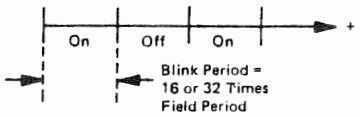
Hardware Scrolling – Registers R12/R13 contents determine which memory location is the first displayed character on the screen. Since the CRTC Linear Address Generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16K block or refresh memory. By centering the R12/R13 pointer in the middle of the available memory space, scrolling up or down is possible . . . by line, page, or character.

#443-906
MC6845 (cont)

FIGURE 10 – CURSOR CONTROL

Cursor Start Register

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate



Example of Cursor Display Mode

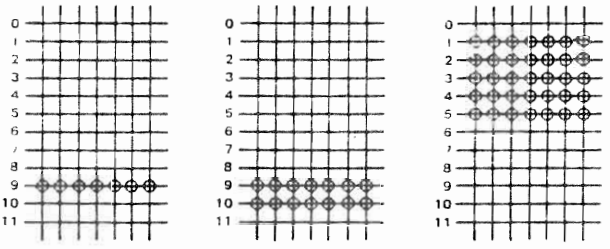
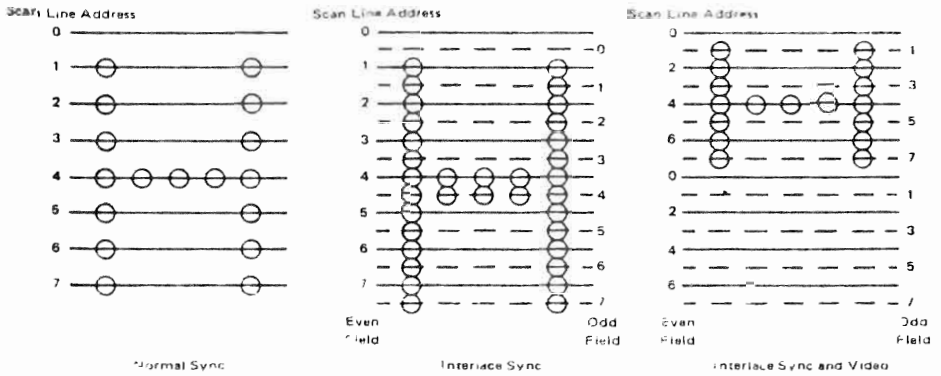


FIGURE 11 – INTERFACE CONTROL

Interlace Mode Register

Bit 1	Bit 0	Mode
0 1	0 0	Normal Sync Mode (Non-Interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode



#443-906
MC6845 (cont)

TABLE 3 – Typical 80 x 24 Screen Format Initialization of CRTC

Reg. #	Register File	Program Unit	Calculation*	Programmed Value	
				Decimal	Hex
R0	H Total	T_c	102 x .527 = 53.76 µs	102 - 1 = 101	N_{ht} = $65
R1	H Displayed	T_c	80 x .527 = 42.16 µs	80	N_{hd} = $50
R2	H Sync Position	T_c	86 x .527 = 45.32 µs	86	N_{hsp} = $56
R3	H Sync Width	T_c	9 x .527 = 4.74 µs	9	N_{hsw} = $09
R4	V Total	T_{cr}	25 x 645.12 = 16.13 ms	25 - 1 = 24	N_{vt} = $18
R5	V Total Adjust	T_{sl}	10 x 53.76 = .54 ms	10	N_{adj} = $0A
R6	V Displayed	T_{cr}	24 x 645.12 = 15.48 ms	24	N_{vd} = $18
R7	V Sync Position	T_{cr}	24 x 645.12 = 15.48 ms	24	N_{vsp} = $18
R8	Interlace Mode	–		–	$00
R9	Max Scan Line Address	T_{sl}		11	N_{sl} = $0B
R10	Cursor Start	T_{sl}		0	$00
R11	Cursor End	T_{sl}		11	$0B
R12	Start Address (H)	–		128	$00
R13	Start Address (L)				$80
R14	Cursor (H)	–		128	$00
R15	Cursor (L)	–			$80

Clock Period = T_c = .527 µs

Scan Line Period = T_{sl} = $(N_{ht} + 1) \times T_c$ = 102 x .527 µs = 53.76 µs

Character Row Period = T_{cr} = $N_{sl} \times T_{sl}$ = 12 x 53.76 µs = 645.12 µs

* These are typical values for the Motorola M3000 Monitor, values may vary for other monitors

FIGURE 12 – INITIALIZATION OF CRTC FOR 80x24 SCREEN FORMAT IN TABLE 3

```
PAGE  001   CRTINT

00001                          NAM    CRTINT
00002 0000                     ORG    $0
00003 0000 5F                  CLR B             CLEAR COUNTER
00004 0001 CE 0020             LDX    #$20
00005 0004 F7 9000 CRTII       STA B  $9000      CRTC ADDR REG
00006 0007 A6 00               LDA A  0,X
00007 0009 B7 9001             STA A  $9001      ACC TO CRTC REG
00008 000C 08                  INX
00009 000D 5C                  INC B             INC COUNTER
00010 000E C1 10               CMP B  #$10       LAST CRTC REG?
00011 0010 26 F2               BNE    CRTII
00012 0012 3F                  SWI
00013 0020                     ORG    $20
00014 0020 65       CRTTAB     FCB    $65,$50,$56,$9
00015 0024 18                  FCB    $18,$0A,$18,$18
00016 0028 00                  FCB    0,$0B,0,$0B
00017 002C 0080                FDB    $80,$80
00018      0000                END
CRTII  0004 CRTTAB 0020

TOTAL ERRORS 00000
```

#443-906
MC6845 (cont)

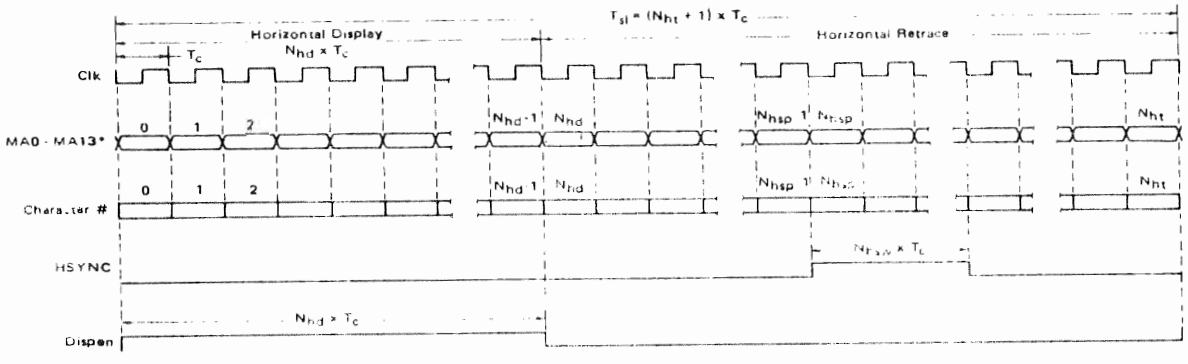
OPERATION OF THE CRTC

Timing Chart of the CRT Interface Signals – Timing charts of CRT interface signals are illustrated in this section with the aid of programmed example of the CRTC. When values listed in Table 4 are programmed into CRTC control registers, the device provides the outputs as shown in the Timing Diagrams (Figures 13 through 15). The screen format of this example is shown in Figure 9. Figure 16 is an illustration of the relation between Refresh Memory Address (MA0-MA13), Raster Address (RA0-RA4) and the position on the screen. In this example, the start address is assumed to be "0".

TABLE 4 – Values Programmed Into CRTC Registers

Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht}+1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt}+1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start		
R11	Cursor End		
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen (L)		

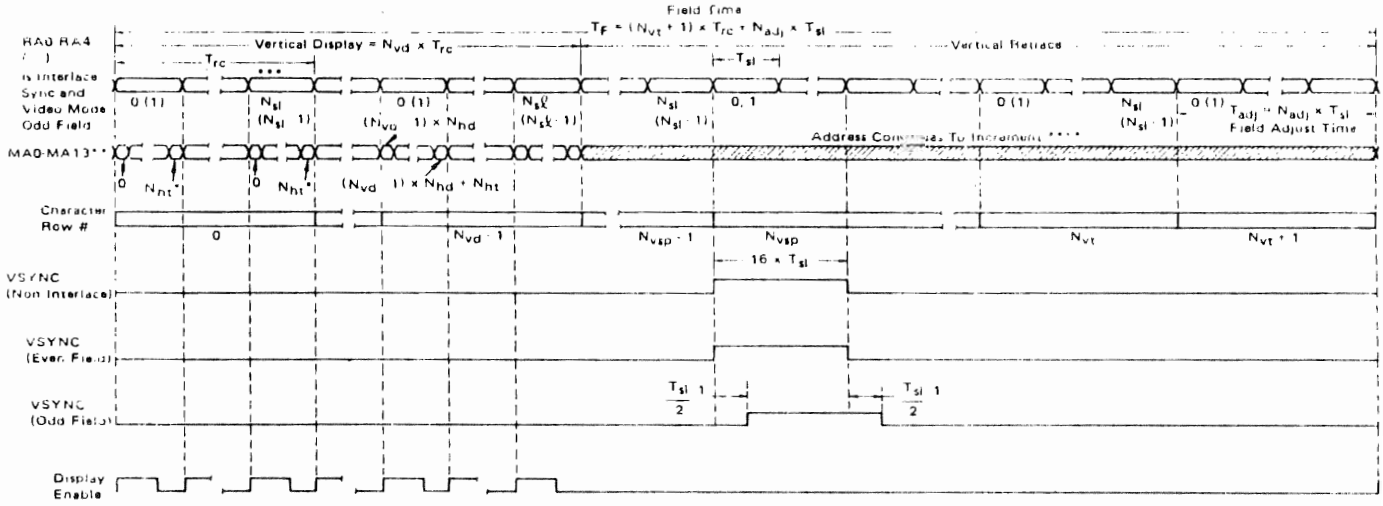
FIGURE 13 – CRTC HORIZONTAL TIMING



*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

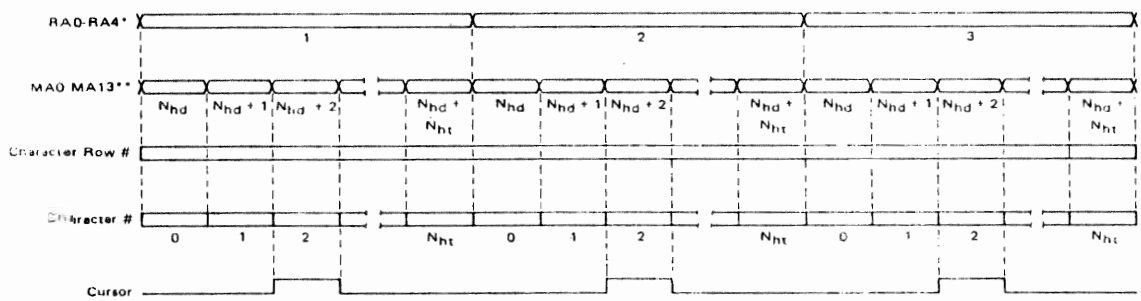
#443-906
MC6845 (cont)

FIGURE 14 – CRTC VERTICAL TIMING



*N_{ht} must be an odd number for both interlace modes.
**Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example
***N_{sl} must be an odd number for Interlace Sync and Video Mode.
****The present CRTC freezes MA addresses at $N_{vd} \times N_{hd}$ during vertical retrace. A design change is pending to allow MA to free run during vertical retrace time.

FIGURE 15 – CURSOR TIMING



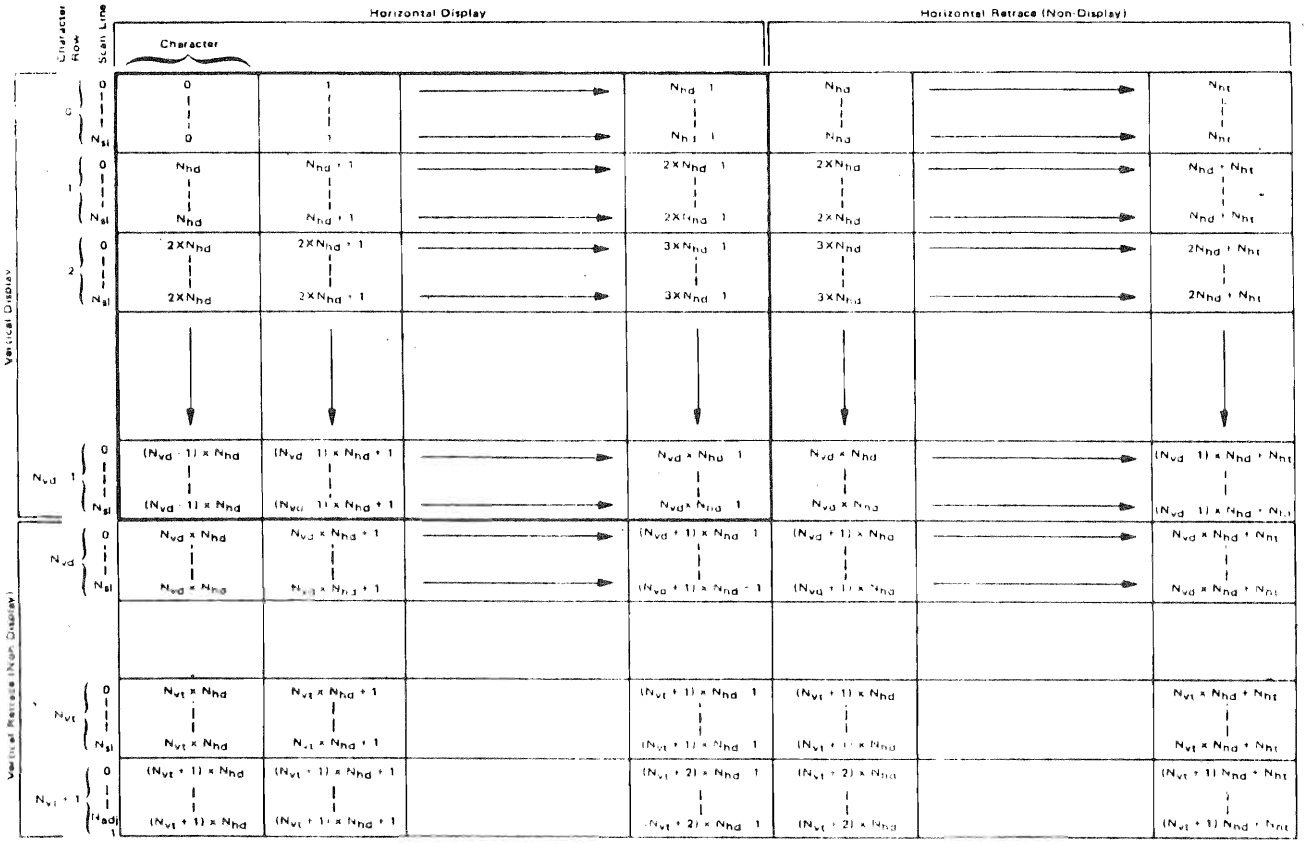
*Timing is shown for non-interlace and interlace sync modes
Example shown has cursor programmed as:
Cursor Register = N_{hd} + 2
Cursor Start = 1
Cursor End = 3

** The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

#443-906

MC6845 (cont)

FIGURE 16 – REFRESH MEMORY ADDRESSING (MA0-MA13) STATE CHART



NOTE 1 The initial MA is determined by the contents of start address register (R12/R13). Timing is shown for (R12, R13) = 0. Only Non-Interlace and Interlace Sync Modes are shown.

NOTE 2 The present CRTC freezes MA and RA at N_{vd} × N_{hd} during vertical retrace. A design change is pending to allow MA to free run during vertical retrace time.

#443-913

MM5740/AAC or MM5740/AAD

MM5740 90-key keyboard encoder

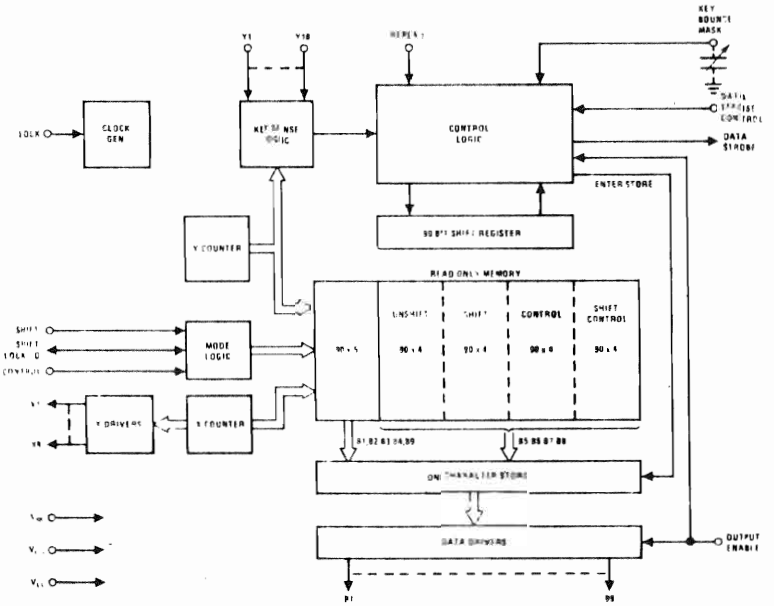
general description

The MM5740 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 90 single pole single throw switch closures into a usable 9-bit code. It is organized as a bit paired system and is capable of N key or two key rollover. The MM5740 is fabricated with silicon gate technology and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

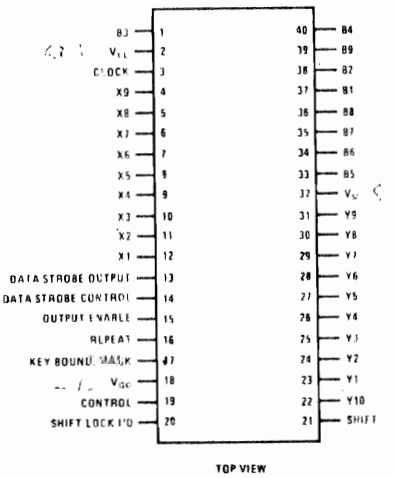
features

- TRI-STATE® data outputs directly compatible with TTL/DTL or MOS logic
- Function inputs directly compatible with TTL/DTL logic
- Only one TTL level clock required
- N key/two key rollover (mask programmable)
- 90 key-quad mode capability
- One character data storage
- Repeat function (selectable)
- Shift lock with indicator capability
- Key bounce masking by single external capacitor
- Level or pulse data strobe output
- Data strobe pulse width control

block and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings MM5740/AAC, AAD (continued)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = +25°C
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1,5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate		10		200	kHz
Clock Pulse Width	Rep. Rate = 200 kHz	2.4		2.6	μs
	Rep. Rate = 10 kHz	20		80	μs
Clock Amplitude					
Logic Level "0"				+2.4	V
Logic Level "1"		+0.4			V
Clock Transition Times					
Risetime	Rep. Rate = 200 kHz			100	ns
Falltime	Rep. Rate = 200 kHz			100	ns
Clock Input Capacitance			5.0		pF
Data Input Levels, Y1 thru Y10					
Logic Level "0"				V_{SS} − 1.5	V
Logic Level "1"		−3.0			V
Logic Level "0"				+2.4	V
Logic Level "1"		+0.4			V
Data Strobe Control					
Logic Level "0"				+3.5	V
Logic Level "1"		+0.4			V
Data Output Levels, X1 thru X9					
Logic Level "0"	When Connected to Y1 thru Y10			V_{SS} − 0.75	V
Logic Level "1"	via Switch Matrix, (C_L = 75 pF)	−3.0			V
B1 thru B9 and Data Strobe					
Logic Level "0"	I = 100μA (Note 2)			V_{SS} − 1.0	V
Logic Level "1"	I = 1.6 mA (Note 2)	+0.4			V
Shift Lock Voltage Open	Before Closure		V_{GG} − 2.0		V
Shift Lock Voltage Closed	Switch Closed		V_{SS}		V
Shift Lock Voltage Locked	After Release, (I = 1.0 mA) (Figure 2)		V_{SS} − 5.0	V_{SS} − 8.0	V
Transition Times					
Data Strobe (T_{DS1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
Data Strobe (T_{DS0})	C_L = 100 pF, I = 100μA			1.0	μs
Data Output Levels					
(T_{DO1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
(T_{DO0})	C_L = 100 pF, I = 100μA			1.0	μs
Output Enable Setup Time (T_{OES})		2.5			μs
Output Enable Release Time (T_{OER})		2.5			μs
Repeat Input Pulse Width (T_{RPW})	(Note 3)				
	f_{CLOCK} = 10 kHz	10			ms
	f_{CLOCK} = 200 kHz	0.5			ms
Power Supply Current	I_{GG}, I_{SS}		20	35	mA

Note 1: These specifications apply for V_{SS} = +5.0 VDC ±5%, V_{GG} = −12.0 VDC ±5%, V_{LL} = GND and T_A = 0°C to +70°C.

Note 2: When outputs B1 thru B9 and Data Strobe are driving TTL/DTL $V_{SS} - V_{LL} \leq 5.25V$. When driving MOS, $V_{SS} - V_{LL} < 10.0V$.

Note 3: T_{RPW} min. = $100 \times \frac{1}{f_{clock}}$

Note 4: If shift and control inputs are derived from a single pole, single throw switch closure to V_{SS}, a 100 OHM resistor returned to V_{LL} (GND) is required on these inputs.

Note 5: The following inputs have internal pull-up resistors to V_{SS}: clock, output enable, repeat, shift, control.

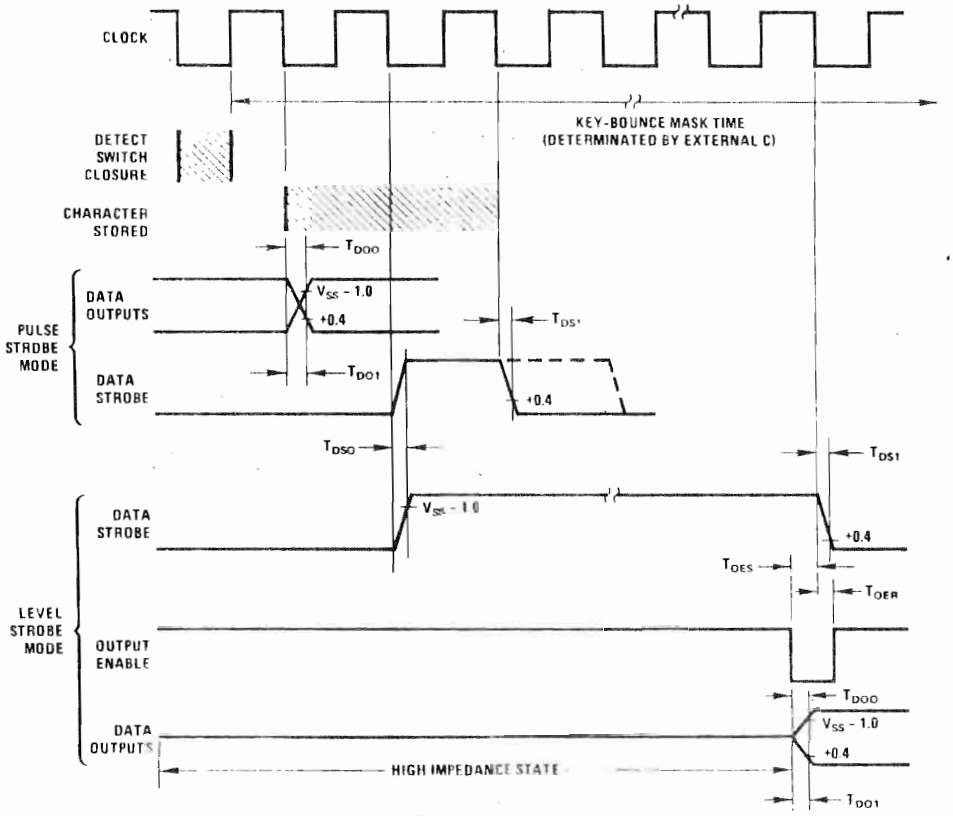
description of pin functions #443-913 MM5740/AAC, AAD (cont)

NAME	PIN NO.	FUNCTION
X1-X9	4-12	These pins are chip outputs which are used to drive the key switch matrix. When activated (at the appropriate scan time) they are driven high.
Y1-Y10	22-31	Pins 22-31 are the Y sense inputs which are connected to the X drive lines via the key switch matrix. They are internally precharged to a low state and are pulled high upon switch closure.
B1-B9	1, 33-40	These are the data outputs which represent the code for each keyswitch. They are TRI-STATE outputs with direct TTL compatibility. When the output enable input (Pin 15) is high, these outputs are in the third state.
Data Strobe Output	13	The function of this pin is to indicate that valid data has been entered by the keyboard and is ready for acceptance. An active data strobe is indicated by a high level. The data strobe may be operated in the pulse or level mode as indicated by the timing diagram.
Data Strobe Control	14	The basic purpose of this input is to provide data strobe output pulse width control. When connected to the data strobe output (Pin 13), the data strobe will exhibit a one bit wide pulse width. The pulse width may be varied by interposing an RC network between the data strobe output and the strobe control input. For level mode of operation the data strobe control input may be tied to V_{SS} or to the data strobe output.
Output Enable	15	This input serves to TRI-STATE the data output (B1-B9) lines. In addition, it controls the return of the data strobe to the idle condition (low state) which is needed in the level strobe mode of operation
Repeat	16	The repeat input is designed to accept a repeat signal via the repeat key. One data strobe will be issued for each positive interval of the repeat signal. Thus, if a 10 Hz signal is applied to the repeat input via the repeat switch, a 10 character per second data strobe will be issued when a data key and the repeat key are held depressed.
Key-Bounce Mask	17	This pin is intended as a timing node to mask switch key-bounce. The mask time interval is generated by connecting a capacitor to this pin.
Shift	21	When this input is brought to a logic "0" (V_{SS}) level, the encoder will assume the shifted character mode
Control	19	A logic "0" places the encoder in the control character mode.
Shift Lock I/O	20	This pin is intended to serve as an input when the shift lock key is depressed. It places the encoder in the shift mode. Upon release of the key, the shift mode will be maintained and this pin will serve as an output to drive an indicator. This function is reset by depressing the shift key.
Clock	3	A TTL compatible clock signal is applied to this pin. A bit time is defined as the time from one negative going transition to the succeeding negative going transition of the clock.
V_{SS}	32	+5.0V supply
V_{LL}	2	Ground
V_{GG}	18	-12V supply

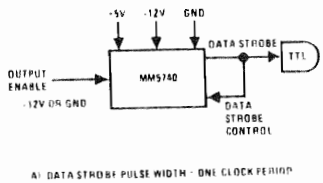
#443-913

MM5740/AAC, AAD

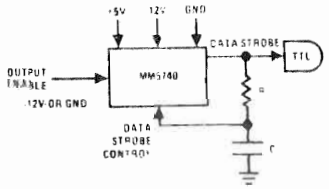
timing diagram



applications information

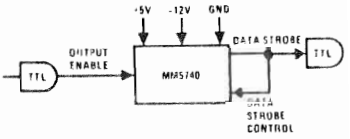


A) DATA STROBE PULSE WIDTH - ONE CLOCK PERIOD



B) WIDER DATA STROBE PULSE WIDTH CONTROLLED BY C

Pulse Data Strobe Mode



Level Data Strobe Mode

key bounce capacitor values

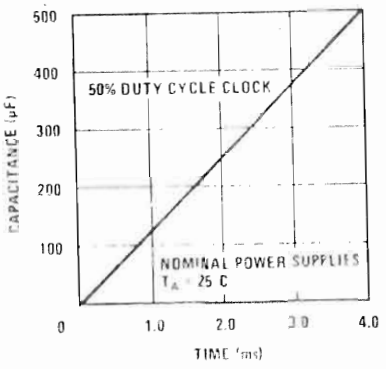


FIGURE 1. Key-Bounce Mask Time

#443-913
MM5740/AAC, AAD
(continued)

application

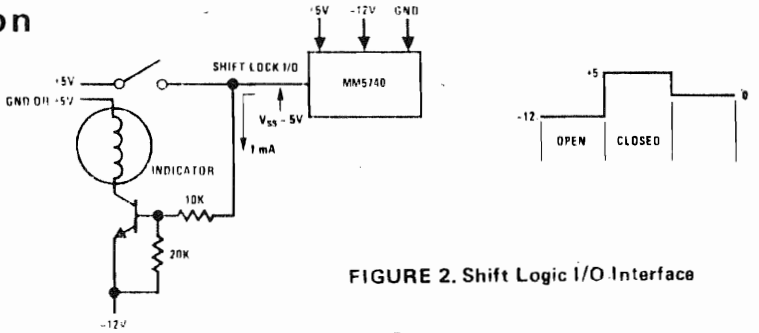
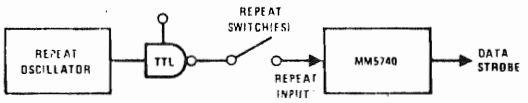
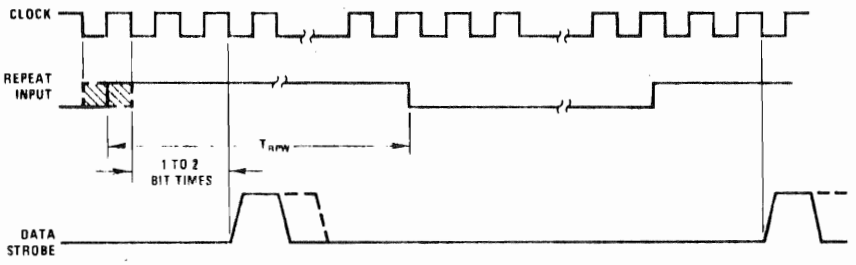


FIGURE 2. Shift Logic I/O Interface

repeat switch function



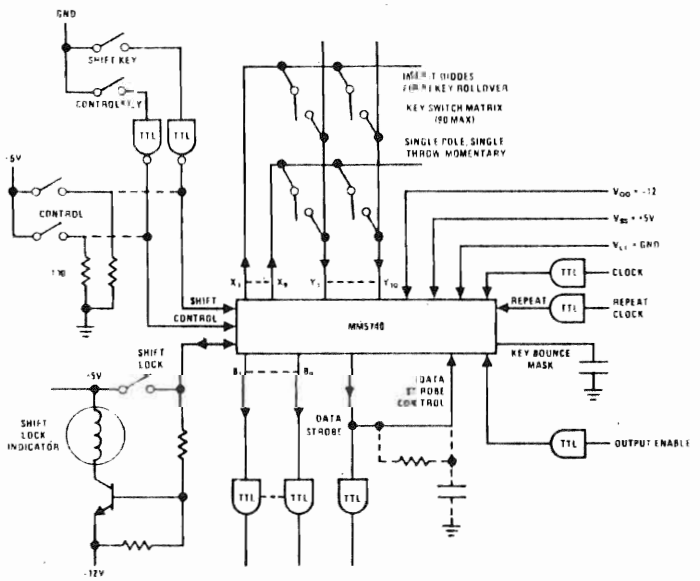
Repeat Switch Connections



Note: Both Repeat Switch and a Data Key must be depressed to enable repeat function. For N-Key Rollover, the data outputs will represent the current valid data key (N Key Roll during Repeat).

Repeat Function

typical applications



#443-913

MM5740/AAC, AAD

(continued)

CODE ASSIGNMENT CHART

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	S/C
(Note3)	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
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☐ N Key Rollover

☐ 2 Key Rollover

Page ☐ of 3 (Note 1)

Note: Use 88 J parity bit is desired

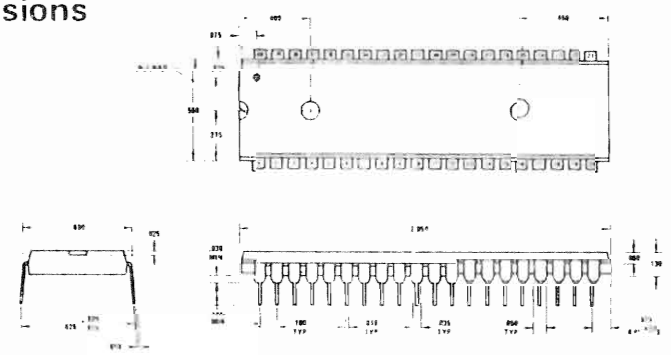
Note 1: 3 code assignment charts are required for each keyboard encoder pattern. Fill in a "1" or "0" in each output box (B1 thru B9.) Indicate page number.

Note 2: The matrix is 9 "X" locations by 10 "Y" locations.

Note 3: Write in 10 one's, 10 two's, etc. in successive X address locations up to 9. This will fill 3 charts. The first page will have address matrix location 1,1; 1,2; 1,3... 1,10; 2,1; 2,2... 2,10; 3,1, etc. up to 3,10. Page 2 has 4,1 to 6,10. Page 3 has 7,1 to 9,10.

Note 4: A contact closure at the address matrix location will cause the appropriate bit pattern to appear at the output in negative true logic. V_{OH} = "0"; V_{OL} = "1"

physical dimensions



Molded Dual-In-Line Package(N)
Order Number MM5740N

#443-913
MM5740/AAC, AAD
(continued)

MICROPROCESSOR MATES WITH MOS/LSI KEYBOARD ENCODER

ABSTRACT

This application note is intended to show how to interface a keyboard to the IMP-16 microprocessor for the purpose of text editing. An example which includes suggested hardware and software is presented to illustrate data inputting from the keyboard to the microprocessor. This example can be used either with the IMP-16 chip set or with the IMP-16C/200 or IMP-16C/300 card.

INTRODUCTION

The MM5740 keyboard encoder interfaced to an IMP-16C card microprocessor provides a very cost-effective means of data entry that takes full advantage of the benefits of MOS/LSI technology. The MM5740 is a complete keyboard interface system capable of providing quad mode* 90 key keyboard encoding in a single integrated circuit. This chip detects a key switch closure and translates it into a coded output while providing all of the necessary functions for modern keyboard system design. Data and control outputs are directly compatible with the TTL logic inputs on the IMP-16C. Characters are read from the keyboard into the read/write memory on the IMP-16C card by means of a program contained in PROM's on the card or in external memory. The characters may be reformatted, edited, converted to binary and processed, transferred to a floppy disk or cassette for more permanent recording, or transmitted to a central computer facility. Typical applications include text editing typewriters, alphanumeric CRT display controllers, remote terminal controllers, data entry and recording systems, operators console in man-machine interactive systems, supervisory or process control systems. Further application information is contained in *AN-80 MOS Keyboard Encoding* and *AN-124 IMP-16 Peripheral Interfacing Simplified. Figure 1* is a functional diagram of a keyboard/IMP-16C interface using the LSI keyboard encoder.

INTERFACE CONSIDERATIONS

The Keyboard

Connecting a physical keyboard to the MM5740 will be covered briefly in the following discussion. A more comprehensive treatment is detailed in AN-80, pgs 3 - 4. For this discussion, reference should be made to *Figure 2* which details the pin connections.

The matrix drive (X_1-X_9) and sense (Y_1-Y_{10}) lines are normally connected to each other via the switch matrix. These lines detect contact closure and sense the key that was depressed. The corresponding character is obtained from a read only memory in the MM5740 which has been mask programmed for the desired code. Nine bits are available for each character. Bits 0 to 7 are generally information bits while bits 8 and 9 may be used for parity or special character control. When a valid key is entered the corresponding 9-bit character is stored internally in latches within the MM5740. After a delay of one bit time (one clock period) the data strobe (pin 13) signal will go high, indicating that data is ready and stored in the output latches. This signal alerts the IMP-16C that the character may now be taken. The function of the data strobe control input (pin 14) is to control the resetting of the data strobe once it has been activated. The output enable (pin 15) serves as the TRI-STATE® control for the code data output lines (B_1 to B_9) and is used to control the resetting of the data strobe output.

To minimize response time, the MM5740 is operated in the pulse data strobe mode. The output enable is tied to ground so that the outputs are always enabled. The data strobe is tied directly to the data strobe control. With this connection, a pulse which is one bit time wide will appear on the data strobe line to indicate available data is present. With a 200 kHz clock, one bit time translates into a 5 μs data strobe pulse.

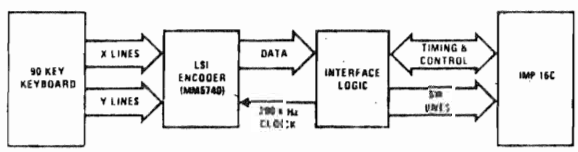


FIGURE 1. Functional Diagram

*Quad mode means the four basic keyboard modes which are; UNSHIFT, SHIFT, CONTROL, SHIFT CONTROL.

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(continued)

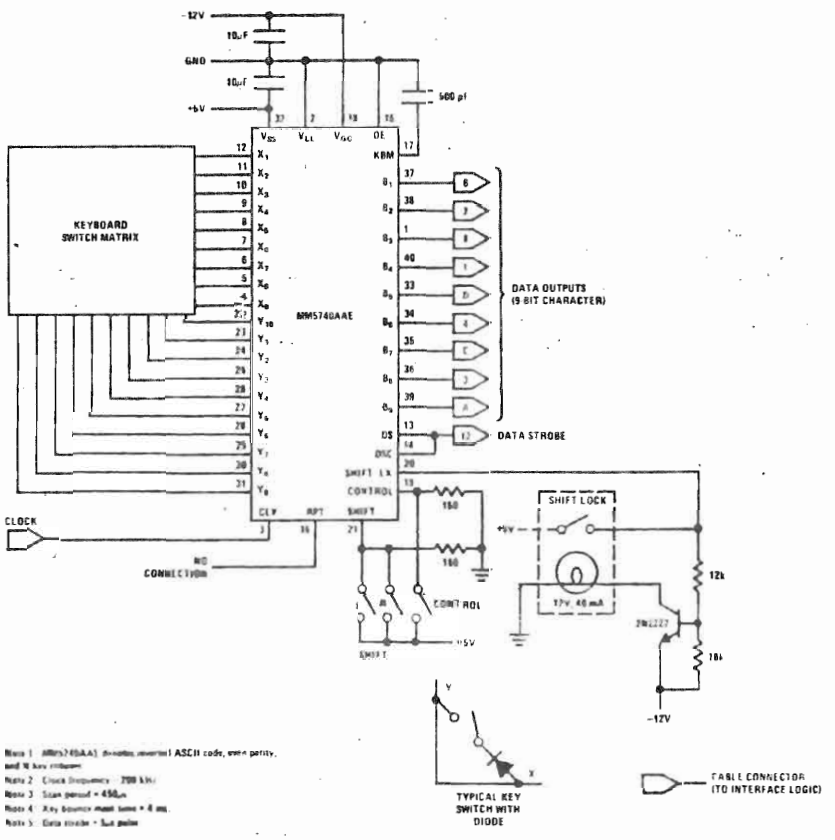

FIGURE 2. MM5740 Pin Connections

In the following sample interface design the MM5740 chip and several discrete components are mounted on a communications keyboard. A cable from the 40 pin connector on the keyboard to an 8 1/2" x 11" interface board provides the physical communications link to the processor. The interface board has space available for components to implement a cassette and CRT interface for text editing applications. Pages of text could be stored as cassette records, called up by the keyboard and displayed on the CRT. Appropriate keyboard commands could be programmed to edit the page. Lines could be inserted, deleted, copied or moved as required. The finished page could be restored on the cassette. *Figure 3* is a schematic diagram of the keyboard interface logic board.

MM5740—IMP-16C INTERFACE

Three instructions are necessary for the IMP-16C to detect that a character is ready for input and to obtain that character. These instructions are given below:

```
LI    3, X '80    ;DEVICE ADDRESS IN AC3
BOC   13, .+0     ;WAIT FOR CHARACTER READY
...               ;INPUT CHARACTER INTO AC0
```

The first instruction sets the peripheral device address of the keybaord (X'80) into accumulator 3 (AC3). This is necessary for proper execution of the RIN instruction (AC3 is added to the sign extended displacement field of the RIN instruction and sent to the peripheral over the ADX lines). The address was chosen so as not to be in conflict with any of the IMP-16P peripherals.

The BOC instruction is essentially a test for keyboard character ready. The data strobe output (DSO) from the keyboard (cable connector pin 12) is stored in a set-reset latch built from cross coupled NAND gates (see *Figure 3*). This is because the DSO pulse width is one clock period or 5.0μs and the processor might not detect DSO in the required time. Refer to *Figure 4* for IMP-16C/MM5740 timing. The complement output of the latch ($\overline{Q}$) is connected to jump condition 13 (JC13). The BOC instruction tests for JC13 and branches to the PC relative address specified in the displacement field if the condition is true. Normally JC13 is true; when a key is pressed DSO goes high which forces $\overline{Q}$ low. The jump condition will then be false and the next instruction executed. This next instruction is a RIN 0 which takes the character from the keyboard encoder (B_1 to B_8) into AC0. Thus, this program is in a one-word BOC

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Execution of the RIN instruction causes:

1. The peripheral device address and order code to be placed on the ADX lines at T4 of microcycle 6 (see *Figure 1-3, IMP-16C Application Manual* Supplement 1, pg. 1 - 3. There are eight timing pulses, T1 to T8, each microcycle. The RIN instruction requires 7 of these microcycles).
2. The RDP (Read Peripheral) flag to be pulsed at T2 of microcycle 7. This is used as a peripheral input gating signal.

The peripheral address and order codes on the ADX lines are set into TTL latches on the IMP-16C during RIN microcycle 6. The ADX lines are sent to all peripherals, but only the one whose address is specified

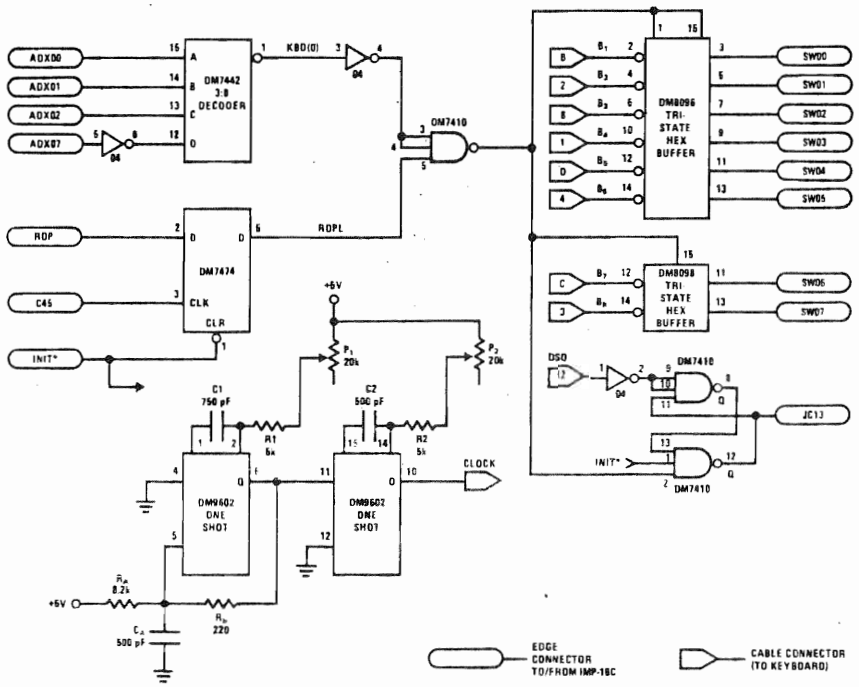

FIGURE 3. Text Editing Keyboard (TEK) Interface Logic for IMP-16C

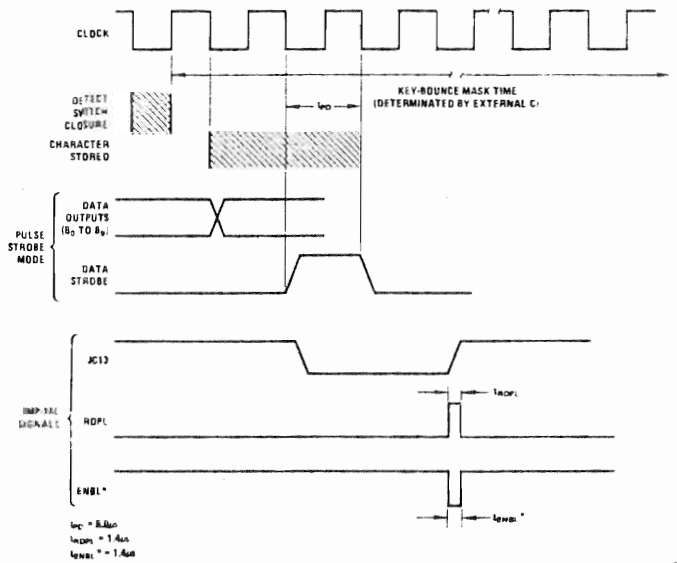

FIGURE 4. MM5740/IMP-C\Timing Diagram

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MM5740/AAC, AAD
(continued)

will respond. A BCD to binary decoder (DM7442) is used to select one of eight possible order codes. This provides modular expansion capability if new peripherals (keyboards, CRT's, cassettes, printers) are added to the keyboard microprocessor system. The RDP signal is latched (RDPL) on the interface to guarantee that it will be valid at T7 of RIN microcycle 7, when data is taken by the processor. At this time the address and order code is valid and the ENBL signal goes low. This signal enables the TRI-STATE buffers (DM8096, DM8098) which complement the inverted ASCII keyboard data (B_1 to B_8) and place it on the SW bus to the processor. The data is taken by the processor at T7 and transferred into AC0 bits 0 to 7. At this point, one character has been obtained by the processor. The ENBL signal is also used to reset the data strobe latch which makes $\overline{Q}$ high and JC13 true. This reconditions the IMP-16C to be ready for the next character.

The MM5740's clock input (CLK) is provided by a dual one shot (DM9602) connected as an oscillator. A 200 kHz square wave is generated using the logic shown in *Figure 3*.

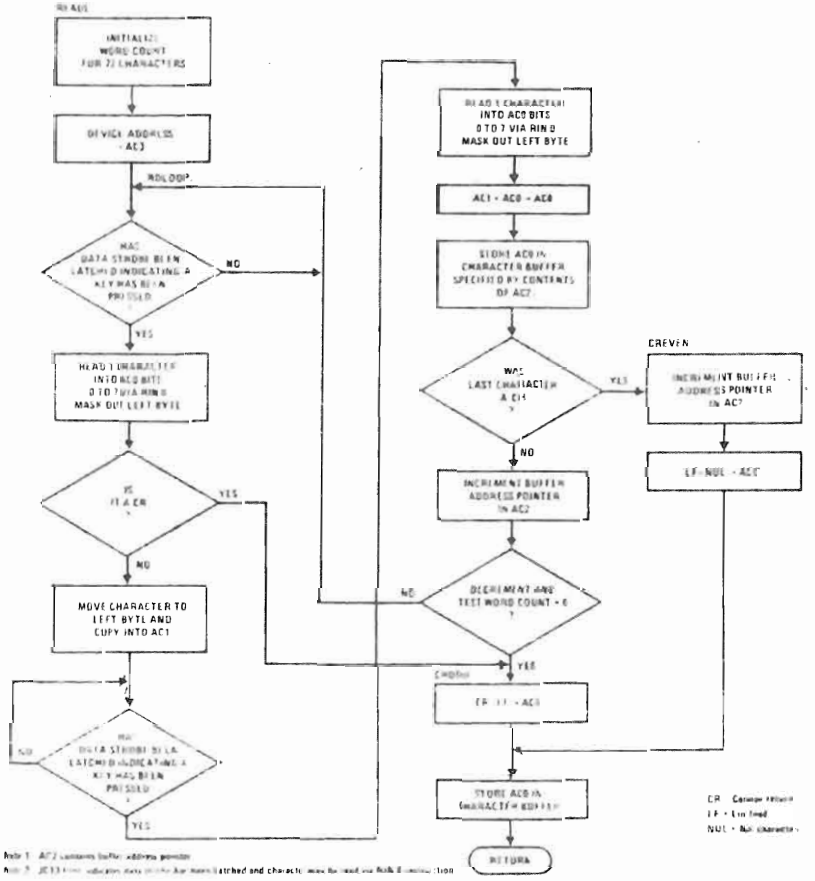
THE PROGRAM

In addition to the three instructions given, a control program is necessary to pack, store and count characters and insert line delimeters—carriage return (CR) and line feed (LF). A flow chart and coding for the program are given in *Figures 5* and *6*.

A line of text is terminated by a CR or when 72 characters have been entered. The CR–LF is inserted and an address pointer is incremented to designate the start of the next line. At this point, the user may request that the last line or entire message be typed on the teletype using the MESG routine in the TTY 16P PROM. Editing functions such as insert, delete, replace, copy, or move lines could be provided if the information was to be output to a CRT, cassette or floppy disc. Although the keyboard encoder (MM5740) used was mask programmed for inverted ASCII code with even parity, any code could be used.

CONCLUSION

The example below demonstrates a keyboard/microprocessor interface taking full advantage of the benefits of LSI technology—small size, increased reliability, fewer interconnections and much more functional capability per unit cost. These advantages may be exploited in a wide range of man-machine or operator interaction systems.



#443-913
MM5740/AAC, AAD
(continued)

```
 1                              .TITLE TEK
 2        0000                   ASECT
 3        0700                  .=X'700
 4                        ; MAIN PROGRAM
 5 0700 8914 A   TEK:     LD      2,STADDR        ;INITIALIZE MESG ADDR
 6 0701 A90C A   GO:      ST      2,MADRES
 7 0702 2914 A            JSR     READL           ;READ 1 LINE & STORE
 8                        ; PUT 1 IN AC0 FOR TTY LINE,0 TO CONTINUE READING,
 9                        ; 2 TO OUTPUT ALL LINES ON TTY
10 0703 0000 A            HALT                    ;ENTER 0/1/2 IN AC0
11 0704 1305 A            BOC     3,OUTL          ;BIT0 AC0=1 OUT LINE
12 0705 1402 A            BOC     4,OUTM          ;BIT1 AC0=1 OUT MESAG
13                        ;  CONTINUE ENTERING NEXT LINE BY DEFAULT
14 0706 4A01 A            AISZ    2,1             ;INCR ADDRESS PTR
15 0707 21F9 A            JMP     GO              ;CONTINUE
16                        ;  OUTPUT ENTIRE MESSAGE ON TTY
17 0708 850C A   OUTM:    LD      1,STADDR        ;SETUP MESG STARTING
18 0709 A504 A            ST      1,MADRES        ;    ADDRESS
19                        ; ENTER 0 AS LAST WORD FOR MESG ROUTINE IN TTY16P
20                        ;  OUTPUT LINE OR MESSAGE
21 070A 4A01 A   OUTL:    AISZ    2,1             ;INCR ADDRESS
22 070B 4C00 A            LI      0,0
23 070C A200 A            ST      0,(2)
24                        ; OUTPUT ON TTY USING MESG SR IN TTY16P PROM
25 070D 2D08 A            JSR     @MESG           ;OUTPUT ON TTY
26       070F     MADRES: .=.+1                   ;MESSAGE ADDRESS
27 070F 21F1 A            JMP     GO              ;READ NEXT LINE
28                        ;
29                        ; DATA AREA
30       0711     WDCNT   .=.+1                   ;WORD COUNT FOR KBD
31 0711 00FF A   H00FF:   .WORD   X'00FF          ;MASK RT WD
32 0712 008D A   CR:      .WORD   X'008D          ;CR W PARITY BIT
33 0713 0D0A A   CRLF:    .WORD   X'0D0A          ;'CR-LF'
34 0714 0A00 A   LFNULL:  .WORD   X'0A00          ;'LF-NUL'
35 0715 1000 A   STADDR:  .WORD   X'1000          ;ST ADDRESS OF MESG
36 0716 7EC3 A   MESG:    .WORD   X'7EC3          ;MESG SR ADDR TTY16P
37                        ; READ 1 LINE FROM KEYBOARD & STORE IN 36 WD BUFFER
38                        ; STARTING BUFFER ADDRESS IN AC2
39                        ; CHARS ARE READ,PACKED & STORED
40                        ; CR IS TERMINAING CHAR  CR LF AT END OF LINE
41                        ;   TC1X FOR DATA STROBE OUTPUT WHEN KEY IS PRESSED
42 0717 4C24 A   READL    LI      0,36            ;WORD COUNT
43 0718 A1F7 A            ST      0,WDCNT
44 0719 4F80 A            LI      3,X'80          ;DEVICE ADDRESS
45 071A 1DFF A   RDLOOP:  BOC     13, +0          ;WAIT FOR DATA STROBE
46 071B 0400 A            RIN     0               ;READ 1 CHAR INTO AC0
47 071C 61F4 A            AND     0,H00FF         ;MASK OUT LEFT BYTE
48 071D F1F4 A            SKNE    0,CR            ;IS IT A 'CR'
49 071E 210D A            JMP     CRODD
50 071F 5C08 A            SHL     0,8             ;MOVE TO LEFT BYTE
51 0720 3181 A            RCPY    0,1
52 0721 1DFF A            BOC     13,.+0          ;WAIT FOR DATA STROBE
53 0722 0400 A            RIN     0               ;READ 1 CHAR INTO AC0
54 0723 61ED A            AND     0,H00FF         ;MASK OUT LEFT BYTE
55 0724 3400 A            RADD    1,0             ;2 PACKED CHARS
56 0725 A200 A            ST      0,(2)           ;STORE IN BUFFER
57 0726 61EA A            AND     0,H00FF         ;WAS LAST CHAR A CR
58 0727 F1EA A            SKNE    0,CR
59 0728 2106 A            JMP     CREVEN
60 0729 4A01 A            AISZ    2,1             ;INCR ADDR POINTER
61 072A 7DE5 A            DSZ     WDCNT           ;DECR & TEST WD COUNT
62 072B 21EE A            JMP     RDLOOP
63                        ;.....
64                        ; ENTER CR-LF AS LAST WORD
```

FIGURE 6. Coding for Text Editing Keyboard (TEK)

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MM5740/AAC, AAD

(continued)

```
65 072C 81E6 A  CRODD:  LD      0,CRLF          ;CR/LINE FEED CHARS
66 072D A200 A          ST      0,(2)           ;STORE IN BUFFER
67 072F 0200 A          RTS     0
68                ; ENTER LF-NUL AS LAST WORD
69 072F 4A01 A  CREVEN: AISZ    2,1              ;INCR ADDRESS PTR
70 0730 81E2 A          LD      0,LFNULL        ;LINE FEED/NULL CHARS
71 0731 21FB A          JMP     CRODD+1
72                ;
73                ;  MESSAGE BUFFER
74                ;  EACH LINE CONTAINS A MAXIMUM OF 72 PACKED CHARS
75                ;  AND A CR-LF
76       1000             .=.+1000
77       0700             .END    TEK

CR       0712  A
CREVEN   072F  A
CRLF     0713  A
CRODD    072C  A
GO       0701  A
H00FF    0711  A
LFNULL   0714  A
MADRES   0706  A
MESG     071C  A
OUTL     070A  A
OUTM     0708  A
RDLOOP   071A  A
READL    0717  A
STADDR   0715  A
TEK      0700  A
WDCNT    0710  A
NO ERROR LINES
SOURCE CK. = AE1A
```

FIGURE 6. Coding for Text Editing Keyboard (TEK) (Continued)

MOS ENCODER PLUS PROM YIELD QUICK TURNAROUND KEYBOARD SYSTEMS*

INTRODUCTION

Most modern keyboard designs employ MOS/LSI keyboard encoder IC's to implement all the necessary electronic functions. The key codes specified by the customer are programmed into a read only memory which is an inherent part of the encoder. Although some common encoder formats are available off the shelf, such as ASR33 teletype (MM5740AAE or MM5740AAF), there are many instances where variations of common formats are needed. Since these formats are mask programmed into the keyboard encoder, there is a certain amount of lead time (approximately 12 weeks) before a customer receives his final circuit.

By using a binary coded keyboard encoder in conjunction with a programmable read only memory, customers can build prototype keyboard systems or fill small volume orders in minimum time. This approach keeps all the encoding electronics and timing the same as in the final system, so that a minimum of redesign is necessary to configure the actual final version. This is done when the keyboard encoder with the final mask programmed key codes is received. In addition, the usefulness of being able to reassign key codes quickly in the PROM makes system debugging and alteration an easy task.

The basic configuration for this implementation is shown in the simplified block diagram of *Figure 1*. The key switches and all timing signals are configured in the normal manner. The keyboard encoder chip will emit binary codes for each valid keyswitch closure. These binary outputs are used as addresses for the PROM which is programmed with the desired actual code for each keyswitch. Each key closure is transformed first to an address by the encoder and then to the final code by the PROM. In this manner, a general design is possible, with the only variable being the contents of the PROM which is easily and quickly programmed. When changes are necessary, the PROM may be erased and reprogrammed quickly making it an easy task to finalize design alterations.

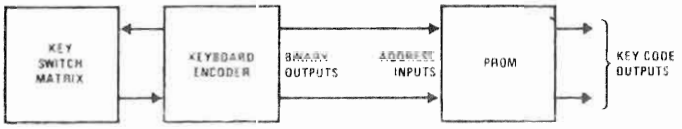

FIGURE 1. Simplified Block Diagram

#443-913
MM5740/AAC, AAD
(continued)

A typical implementation of this approach is shown in *Figure 2*. The encoder employs a dynamic scanning technique to identify key closures. Each keyswitch is defined by a particular X drive line and Y sense line of the encoder. In addition to the basic operation of translating a switch closure to a coded output, the MM5740

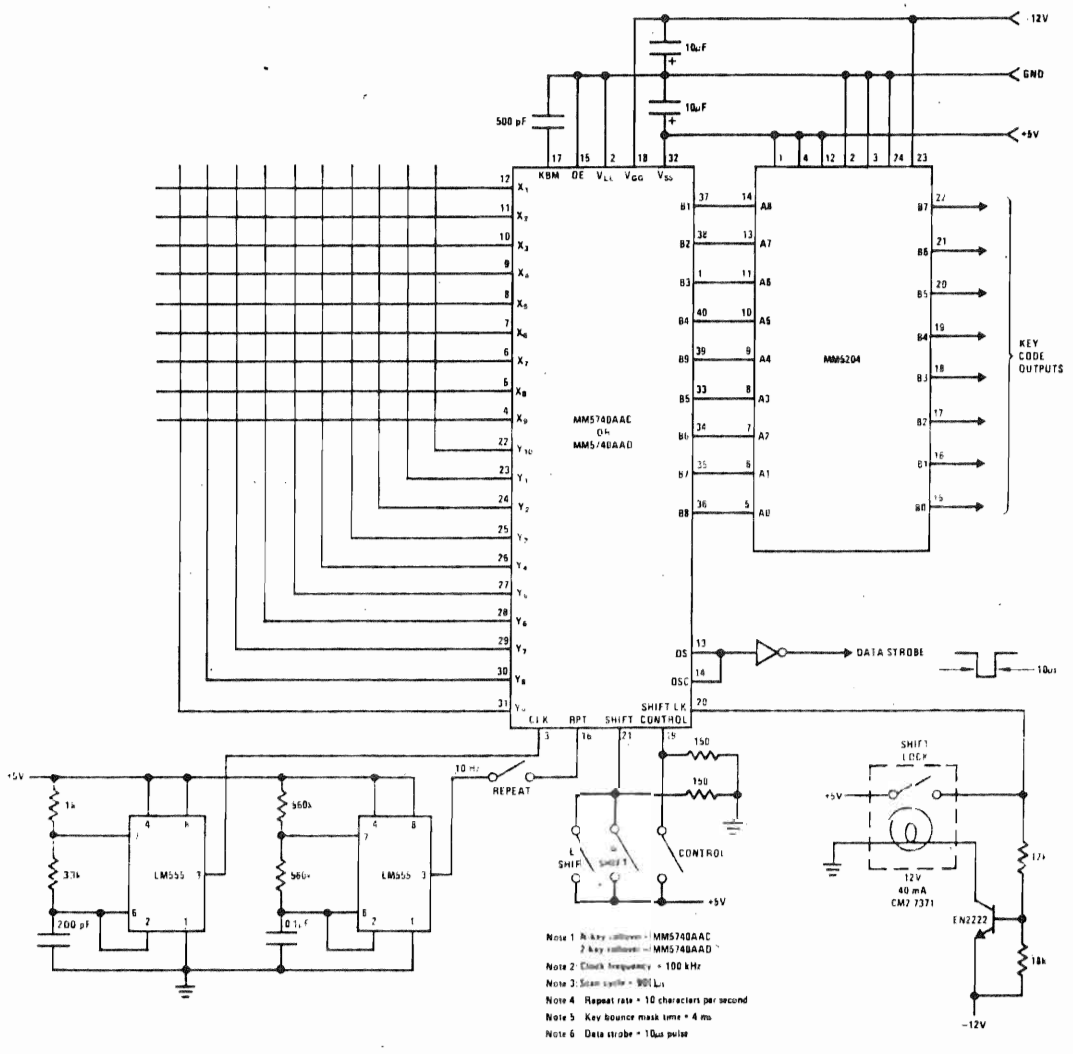

FIGURE 2. Typical Keyboard System

#443-913
MM5740/AAC, AAD
(continued)

provides all the functions necessary for modern keyboard system design. This includes all the logic necessary for key validation, 2-key or N-key rollover, bounce masking, mode selection and strobe generation. Table I illustrates the relationship between keyswitch matrix position, key mode and the binary coded outputs of the MM5740 AAC or AAD encoder. The AAC version provides for N-key rollover while the AAD is a 2-key rollover encoder. Since there are nine X lines, ten Y lines and four modes, 360 nine-bit codes are possible.

In the general application using 90 four mode keys, a 4k PROM (MM5204) should be used. If less than 64 four-mode keys are all that is required, a 2k PROM (MM5203) may be substituted. In this case, the most significant bit (B1) from the encoder is dropped and Table I addresses would go from 0–255. When programming the PROM, it should be noted that the MM5740 uses a bit paired coding system. Any particular key will have 5 common bits (B1, B2, B3, B4, B9) and 4 variable bits (B5, B6, B7, B8) which may change when going from one mode to another. In addition, encoder coding is specified in terms of negative logic so that it may be necessary to complement positive logic PROM contents when ordering encoder masks.

By careful PC board layout, the encoder/PROM prototyping system can utilize the same PC board as the final system with the PROM removed. This can be accomplished by arranging the traces so that it is possible to provide jumpers from the encoder outputs to the PROM outputs. Utilizing this approach allows for a minimum of tooling, parts counts and quick turnaround time for new designs.

TABLE I. Encoder/PROM Mapping

	KEY POSITION		MODE	ADDRESSES (ENCODER OUTPUT)									KEY CODE OUTPUTS (PROM CONTENTS)							
	X	Y		B1	B2	B3	B4	B9	B5	B6	B7	B8	B7	B6	B5	B4	B3	B2	B1	B0
KEY 1	1	1	Unshift	0	0	0	0	0	0	0	0	0								
	1	1	Shift	0	0	0	0	0	0	0	0	1								
	1	1	Control	0	0	0	0	0	0	0	1	0								
	1	1	Shift Control	0	0	0	0	0	0	0	1	1								
	1	2	Unshift	0	0	0	0	0	0	1	0	0								
	1	2	Shift	0	0	0	0	0	0	1	0	1								
	1	2	Control	0	0	0	0	0	0	1	1	0								
	1	2	Shift Control	0	0	0	0	0	0	1	1	1								
													USER DEFINED KEY CODES							
KEY 90	9	10	Unshift	1	0	1	1	0	0	1	0	0								
	9	10	Shift	1	0	1	1	0	0	1	0	1								
	9	10	Control	1	0	1	1	0	0	1	1	0								
	9	10	Shift Control	1	0	1	1	0	0	1	1	1								

*Encoder outputs are listed in positive true logic notation.

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MM5740/AAC, AAD
(continued)

TABLE II. Truth Table
MM5740/AAC or MM5740/AAD

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL			
		B1	B2	B3	B4	B9	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
1	2	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
1	3	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
1	4	1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
1	5	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
1	6	1	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
1	7	1	1	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
1	8	1	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
1	9	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
1	10	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
2	1	1	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
2	2	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
2	3	1	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
2	4	1	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
2	5	1	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
2	6	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
2	7	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
2	8	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
2	9	1	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
2	10	1	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
3	1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
3	2	1	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
3	3	1	1	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
3	4	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
3	5	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
3	6	1	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
3	7	1	1	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
3	8	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
3	9	1	1	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
3	10	1	1	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
4	1	1	0	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
4	2	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
4	3	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
4	4	1	0	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
4	5	1	0	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
4	6	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
4	7	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
4	8	1	0	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
4	9	1	0	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
4	10	1	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
5	1	1	0	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
5	2	1	0	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
5	3	1	0	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
5	4	1	0	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
5	5	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
5	6	1	0	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
5	7	1	0	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
5	8	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
5	9	1	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
5	10	1	0	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
6	1	1	0	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
6	2	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
6	3	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
6	4	1	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
6	5	1	0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
6	6	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
6	7	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
6	8	1	0	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
6	9	1	0	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
6	10	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
7	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
7	2	1	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
7	3	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
7	4	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
7	5	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
7	6	0	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
7	7	0	1	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
7	8	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
7	9	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
7	10	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
8	1	0	1	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
8	2	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
8	3	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
8	4	0	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
8	5	0	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
8	6	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
8	7	0	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
8	8	0	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
8	9	0	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
8	10	0	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
9	1	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
9	2	0	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
9	3	0	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
9	4	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
9	5	0	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
9	6	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1
9	7	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	1
9	8	0	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
9	9	0	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	1
9	10	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	1

443-915

74S86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S86 . . . . . −55°C to 125°C
SN74S86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S86			SN74S86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		50	75		50	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶		FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}		A or B	Other input low	C_L = 15 pF, R_L = 280 Ω, See Note 3		7	10.5	ns
t_{PHL}						6.5	10	
t_{PLH}		A or B	Other input high			7	10.5	ns
t_{PHL}						6.5	10	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 1-18.

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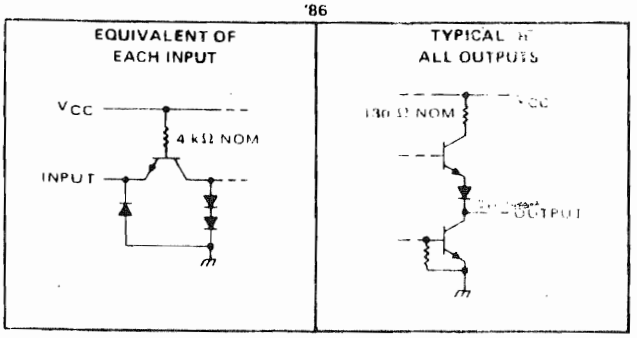
74S86

TTL MSI

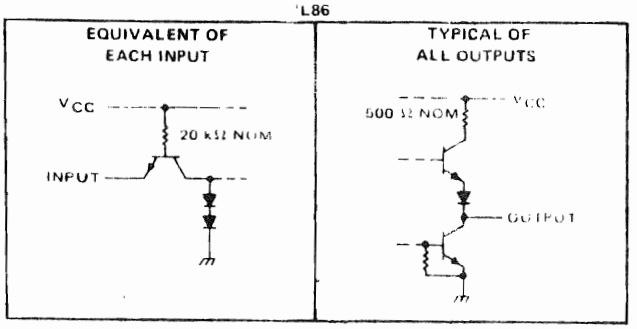
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

schematics of inputs and outputs

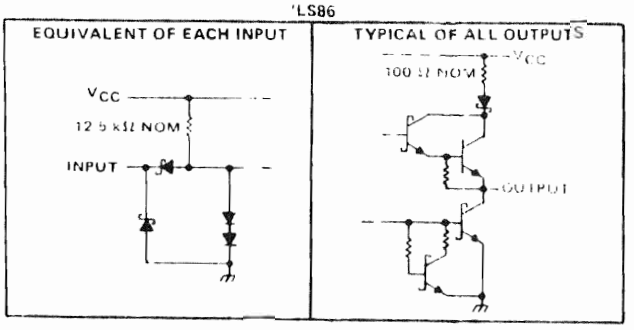
'86



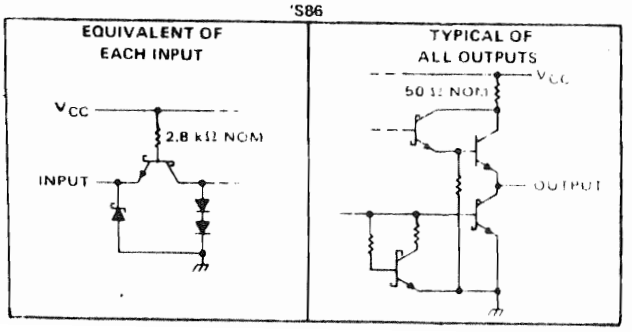
'L86



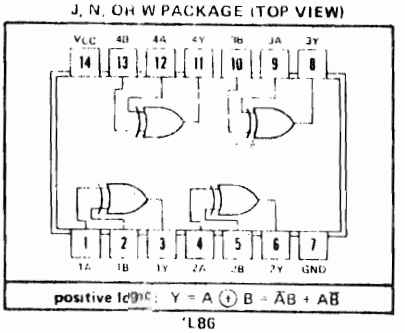
'LS86



'S86

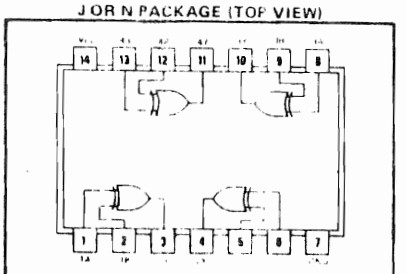


'86 'LS86, 'S86
J, N, OR W PACKAGE (TOP VIEW)



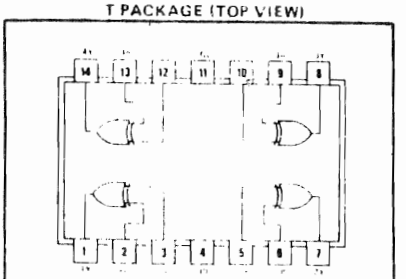
positive logic: $Y = A \oplus B = \bar{A}B + A\bar{B}$

'L86
J OR N PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \bar{A}B + A\bar{B}$

'L86
T PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \bar{A}\bar{B} + AB$

FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

#444-29/#444-37
2316 / EA8316E

EA 8316E—READ ONLY MEMORY—2048 WORDS, 8 BITS/WORD

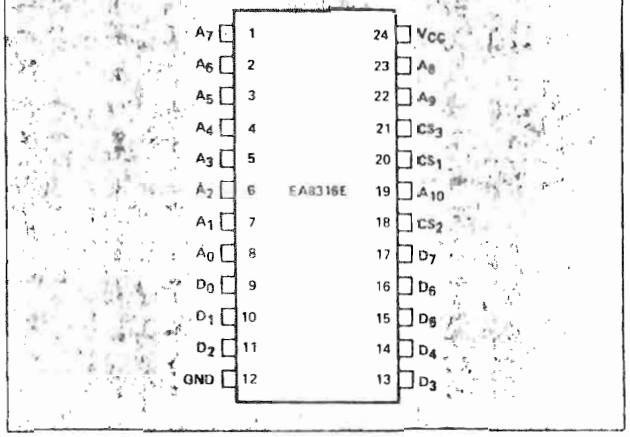
GENERAL DESCRIPTION

The EA8316E is a 16,384 bit Read Only Memory utilizing MOS N-channel metal gate technology. It is organized 2048 words by 8 bits and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has three programmable chip select inputs and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of any external logic. Programming of the device is accomplished by a custom mask during fabrication. The EA8316E pin out is compatible with the EA2708 EPROM and can replace two 2708's for production.

FEATURES

- Fast Access Time – 450 nsec
- All Inputs and Outputs Directly Compatible with TTL
- Three-State Outputs
- Single +5 Volt Power Supply
- Extended Temperature Range
- Pin Compatible with EA2708 EPROM
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Input Protected – All Inputs Have Protection Against Static Charge

CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS

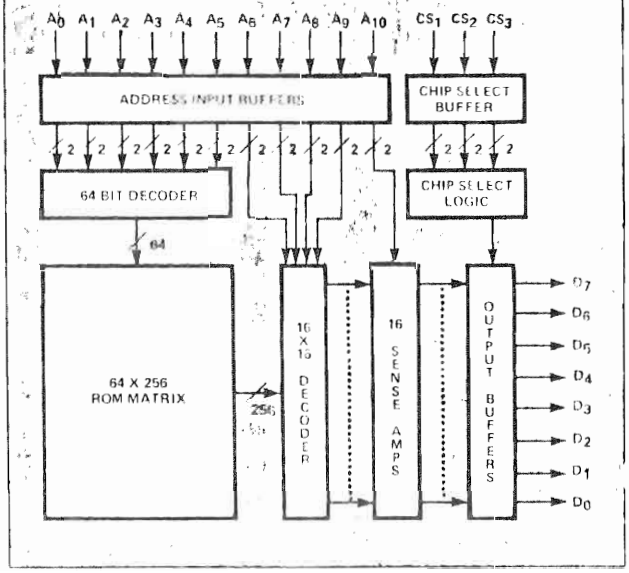
(Above which the useful life of the device may be impaired.)

Voltage on all Inputs and Supply Pins . . . . -0.5V to +7.0V
Maximum Junction Temperature . . . . . +150°C
θ_{JC} . . . . . Hermetic DIP: +65°C/W
Storage Temperature . . . . . -65°C to +150°C

ORDERING INFORMATION

	TEMP. RANGE	PACKAGE
EA8316E DC	0°C to +70°C	Hermetic 24 Pin DIP
EA8316E DL	-55°C to +100°C	Hermetic 24 Pin DIP

BLOCK DIAGRAM



ELECTRICAL PARAMETERS

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2316 / EA8316E

STANDARD CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground. Positive current flows into the referenced pin.

EA8316E C	$4.75V \leq V_{CC} \leq 5.25V$	$0°C \leq T_A \leq +70°C$
EA8316E L	$4.50V \leq V_{CC} \leq 5.50V$	$-55°C \leq T_A \leq +100°C$

D.C. AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	EA8316E L			EA8316E C			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IL}	Input "Low" Voltage		-0.5		0.8	-0.5		0.8	V
V_{IH}	Input "High" Voltage		2.2		V_{CC}	2.0		V_{CC}	V
I_{IL}	Input Load Current	V_{IN} = 0 to 5.25V			10			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +2.1mA			0.45			0.40	V
V_{OH}	Output "High" Voltage	I_{OH} = -100μA	2.2			2.4			V
I_{LO}	Output Leakage Current	Chip Disabled			10			10	μA
I_{CC}	Power Supply Current	All inputs +5.25V Data Out Open		75	140		75	105	mA

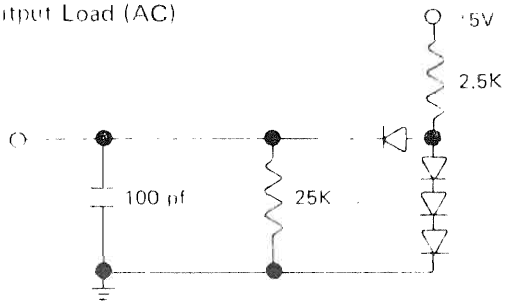
A.C. CHARACTERISTICS

Symbol	Parameter	EA8316E L			EA8316E C			Unit
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
T_{ACC}	Address to Output Delay Time		350	525		350	450	nsec
T_{CO}	Chip Select to Output Delay Time			250			200	nsec
T_{DF}	Chip Deselect to Output Data Float Time			200			150	nsec

(1) T_A = 25°C and V_{CC} = 5V

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load (AC)



CAPACITANCE – T_A = 25°C, f = 1MHz

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		7pF
C_{OUT}	Output Capacitance		14pF

Input Pulse Rise and Fall Times 20nsec
Timing Measurement Reference Level. . . . . 2.2V V_{IH}; 2.0V V_{OH}; 0.8V V_{IL}; 0.8V V_{OL}

TIMING DIAGRAM

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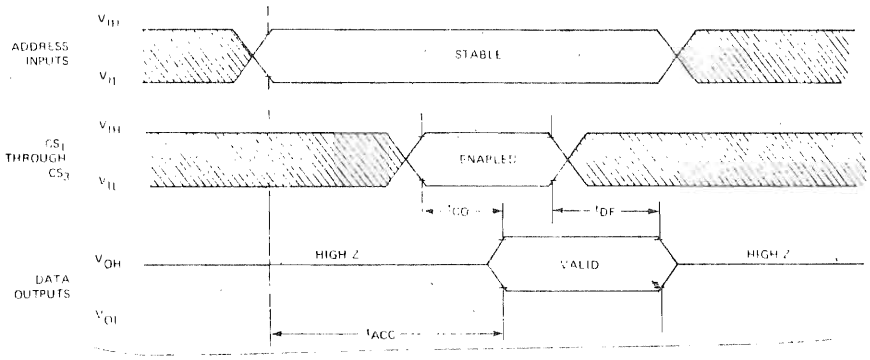
2316 / EA8316E



DEFINITIONS

Access Time, T_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

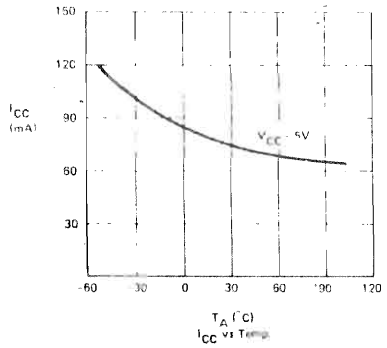
Output Enable Time, T_{CO}

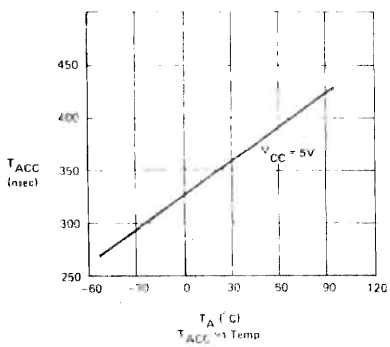
Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

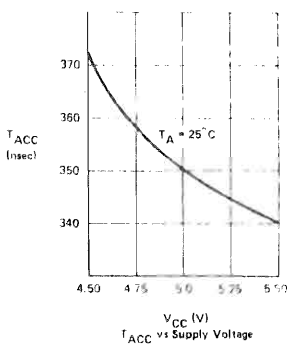
Output Disable Time, T_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

TYPICAL CHARACTERISTICS







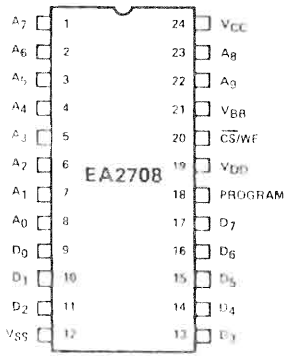
ECONOMY SUGGESTIONS

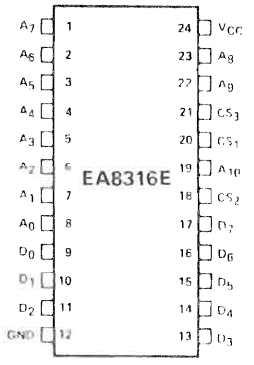
The EA8316E can be used to replace two EA 2708's. The two parts can be used as the input for programming the EA8316E. The following care should be taken:

Pin No.	EA2708	EA8316E
18	Program	$\overline{CS_2}$
19	V_{DD}	A_{10}
20	$\overline{CS}$/WE	$\overline{CS_1}$
21	V_{BB}	$\overline{CS_3}$

NOTE:
1. Wire jumpers may be needed on board for pins 18, 19 and 21.
2. A_{10} is used to identify each half of the EA8316E (i.e., EA2708 0 = $\overline{A_{10}}$, EA2708 - 1 = A_{10}) for input in formation.
3. I_{CC} for EA8316E is 105mA max and is 5mA max for EA2708. No V_{DD} supplies are needed on the EA8316E.

CONNECTION DIAGRAMS





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2316 / EA8316E

MASK OPTION SPECIFICATIONS (continued)

CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

For the very large MOS Read Only Memories now produced by EA, a computer aided technique utilizing punched computer cards is employed. This technique requires that the customer supply EA with a deck of standard 80 column computer cards describing the data to be stored in the ROM array.

TITLE CARD

All customer ROM "Data Cards" must be preceded by a "Title Card" which contains all unique information pertaining to that ROM other than the ROM data content. The required punching format is as follows:

Card Column No.	Card Contents
1	* (Asterisk)
2-19	Customer Name
20-21	Blank (no punch)
22-23	Month; i.e., 05 for May
24	/ (slash)
25-26	Day of the month; i.e., 04 for the 4th day
27	/ (slash)
28-29	The last two digits of the year
30-31	Blank
32-39	Customer's part number (only if required to be different than EA's number)
40-41	Blank
42-49	EA part number, i.e., 8316E157 (to be obtained through EA sales personnel)
50	Rev. letter (i.e., A for original Truth Table)
51	Blank
52-56	ROM Type (i.e., 8316E)
57-59	Blank
60-61	Data Format (i.e., EA = EA's)
62-63	Blank
64	CS_3 level desired for chip selection (1 or 0 only)
65	CS_2 level desired for chip selection (1 or 0 only)
66	CS_1 level desired for chip selection (1 or 0 only)
67-80	Blank

DATA CARDS

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore, the customer must submit cards defining the entire ROM contents, when portions of the ROM may be unused (zero).

Card Column No.	Card Contents
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card (this is the initial address).
5-7	Punch a 3-digit octal number representing the outputs for the initial input address.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address + 1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address + 2.
...	...
...	...
...	...
50-52	Punch a 3-digit octal number representing the outputs for the initial input address + 15
69-80	The unique number assigned to this ROM pattern by EA must be punched in this field enclosed by blank spaces.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.

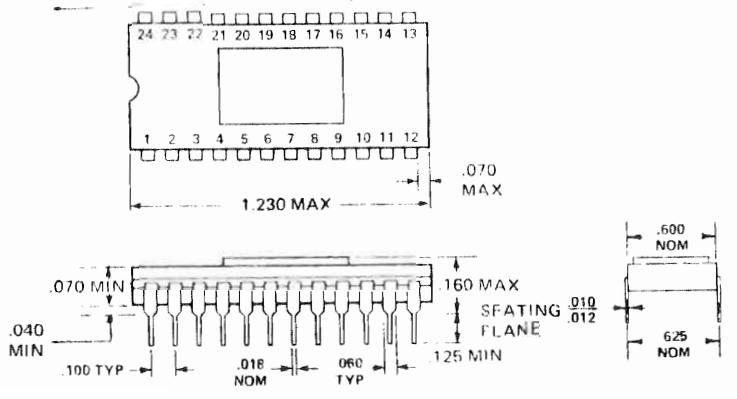
ALTERNATIVE INPUT MEDIA

In addition to the preferred 80 column "IBM Card," customers may submit their ROM bit patterns on 9-track 800-BPI mag tape or 8-channel perforated paper tape. Where one of several nationwide time sharing services is mutually available, arrangements may be made with the factory to communicate the ROM definition data directly through the service computer. Format requirements and other information required to use alternative input media may be obtained through EA sales personnel.

ALTERNATIVE DATA FILE FORMATS

In addition to the standard EA octal format, it is possible to furnish data to EA in other formats if prearranged with the factory. A standard hexadecimal format is currently available. Other non-standard formats may be acceptable. Contact EA sales personnel.

PHYSICAL DIMENSIONS



#444-44/444-45

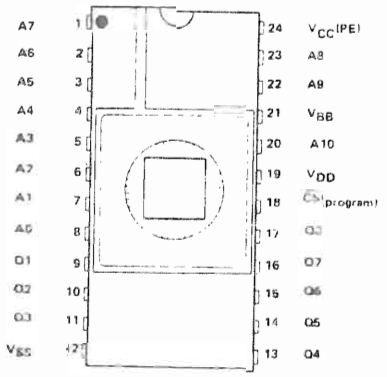
2716

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

MOS LSI

- 2048 × 8 Organization
- All Inputs and Outputs Fully TTL-Compatible
- Static Operation (No Clocks, No Refresh)
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power . . . 315 mW (Typical)

24-PIN CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The TMS 2716 JL, JDL is an ultra-violet light-erasable, electrically programmable read only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resitors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS 2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS 2716 is plug-in compatible with the TMS 2708 and the TMS 27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in 24-pin dual-in-line cerdip (JL suffix) and sidebraze (JDL suffix) packages designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers. It is desingd for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)
The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [$\overline{CS}$ (Program)]
When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program
In the program mode the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or + 12 V on this pin will cause the TMS 2716 to assume program cycle.

data out (O1-O8)
The chip must be selected before the eight bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

operation (program mode)

erase

Before programming, the TMS 2716 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity × exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25°C) only.

to start programming (see program cycle timing diagram)

First bring the V_{CC}(PE) pin to +12 V or 0 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +26V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)}$ = 1 ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable V_{CC}(PE) is brought back to ±5 volts which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to $V_{IL(PE)}$.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 15 V
All input voltage (except program) (see Note 1)	−0.3 to 20 V
Program Input (see Note 1)	−0.3 to 35 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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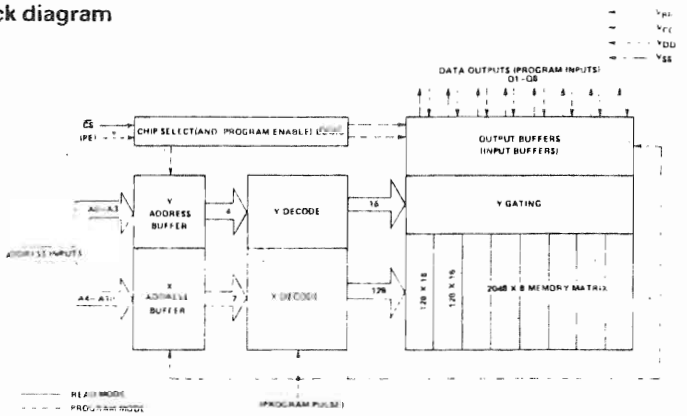
2716 (cont)

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

functional block diagram



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	4.75	−5	5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		$V_{CC}+1$	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max = $V_{IH(PR)}$ − 25 V	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNITS
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			V
		I_{OH} = −1 mA	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10	μA
I_O	Output current (leakage)	$\overline{CS}$ (Program) = 5 V		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high		10	20	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$ (Program) = 5 V		1	8	mA
I_{DD}	Supply current from V_{DD}	For I_{DD} MAX, T_A = 0°C (worst case)		26	45	mA
I_{PE}	Supply current from PE on V_{CC} Pin	V_{PE} = V_{DD}		2	4	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C			540	mW
		T_A = 0°C, $\overline{CS}$ = 0 V		315	595	
		T_A = 0°C, $\overline{CS}$ = +5 V		375	720	

†All typical values are at T_A = 25°C and nominal voltages

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	TYP†	MAX	UNIT
C_i	Input capacitance [except CS (Program)]	4	6	pF
$C_{i(CS)}$	CS (Program) input capacitance	20	30	pF
C_o	Output cpacitance	8	12	pF

†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

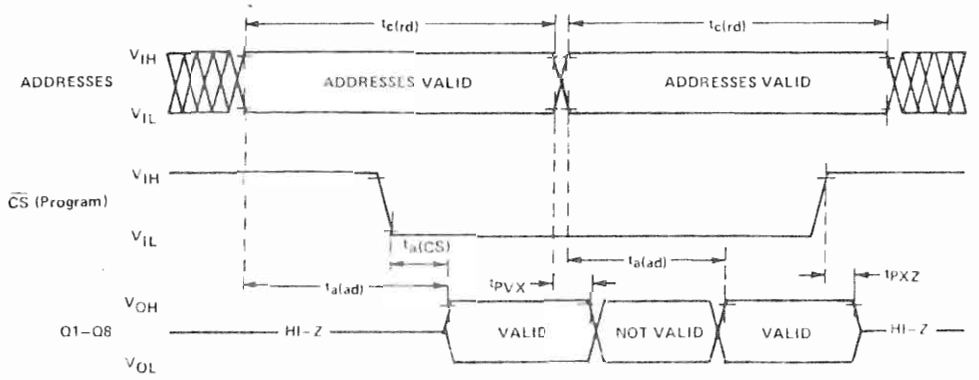
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns		450	ns
$t_{a(CS)}$	Access time from CS			120	ns
t_{PVX}	Output invalid from address change		0		ns
t_{PXZ}	Output disable time		0	120	ns
$t_{c(rd)}$	Read Cycle time		450		ns

T_A = 25°C program characteristics over recommended supply voltage range

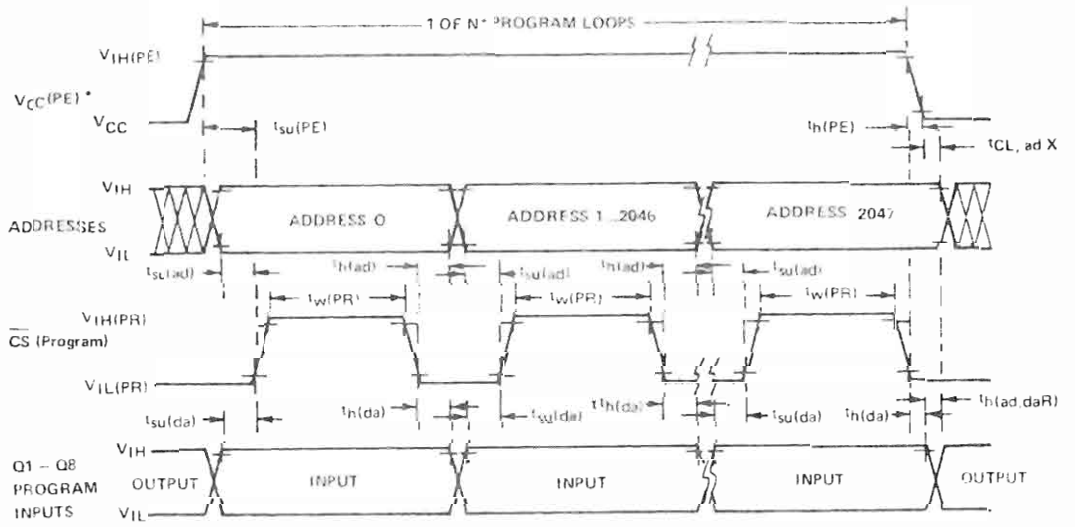
	PARAMETER	MIN	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	50	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,daR)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, CS (Program) low to address change	0		ns

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

read cycle timing



program cycle timing



*V_{CC} (PE) is at 0 V or +12 V through N program loops where N ≥ 100 ms/tw (PR).

NOTE: Q1-Q8 outputs are floating up to 10 usec after programming (V_{CC} (PE) goes low).

... in this data sheet (inputs and outputs) are 90% points.

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2716 (cont)

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

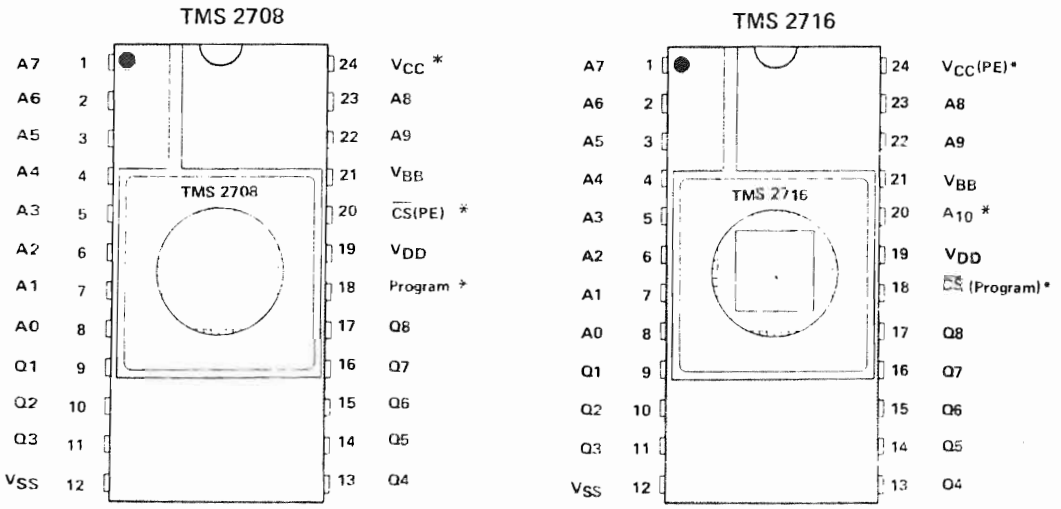
APPLICATIONS INFORMATION

Ease of Conversion From TMS 2708 To TMS 2716

A. The TMS 2716 and TMS 2708 have compatible timing, voltage and current parameters in both modes.

B. The TMS 2716 requires less power than the TMS 2708.

C. The pinouts are compatible. (See below.)



As can be seen from the above diagrams, only three pins* are modified in going from TMS 2708 to TMS 2716:

1. The additional address pin requrired for the 16K EPROM is located on pin 20 which displaces the $\overline{CS}$/PE functions on the TMS 2708.

2. Since the V_{CC} is not required during programming, the PE function shares pin 24 with V_{CC} on the TMS 2716.

3 The $\overline{CS}$ function and program function are mutually exclusive during normal read mode (and are self-actuated complementary during the program/verify mode) and share pin 18 on the TMS 2716.

The diagrams below show how these three pins are actually utilized in the read mode and in the program mode. Only pins 18, 20, and 24 need to be shown, as all other pin connections are identical.

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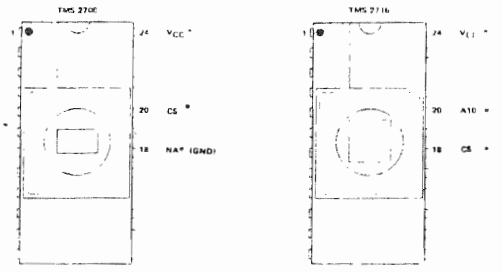
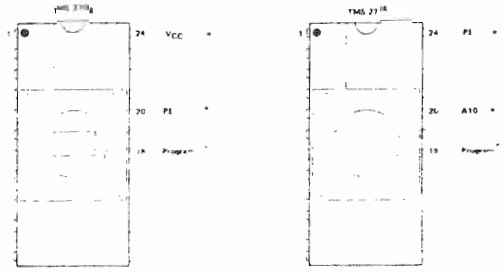
2716 (cont)

2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

Read Mode



Program (Write) Mode



TMS 2716 — Easy Programmability On Existing 2708 Programmers

Existing EPROM Programmers — Upgrading To The TMS 2716

Most of the EPROM manufacturers have implemented field upgrade modifications to allow TMS 2716 programming on current EPROM programmers. This is greatly simplified because the TMS 2716 and the TMS 2708 are programmed in an identical manner. A slight modification to the socket card, an additonal 1K × 8 of RAM, and an extra address signal (A10) are all that is required. All timing and voltage parameters are identical, so the upgrade is easily accomplished. Programmer manufacturers contacted to date on the TMS 2716 include: Data I/O, PRO LOG, Texas Instruments, Technico, CramerKit, Shepardson Micro Systems, Cromenco, MicroPro, Ramtek, Oliver Audio, Inc., etc. Ultraviolet Erasure lights and fixtures are available from Ultraviolet Products, Turner Designs, and others.

NOTE: Information on EPROM programmers and erasurers are provided only for user convenience and do not indicate any preference by TI

PARTS LISTS

CHASSIS

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C1	1500 µF electrolytic	25-857
C2	10 µF electrolytic	25-880
DIODES		
D1	1N4149	56-56
D2	1N4149	56-56
D3	LED	412-616
FUSE		
F1	1 ampere	421-23
RESISTORS		
R1	1000 Ω	6-102-12
R2	1000 Ω	6-102-12
R3 thru R9	10 kΩ	6-103-12
R11 thru R19	10 kΩ	6-103-12
R21 thru R29	10 kΩ	6-103-12
R31 thru R35	100 kΩ	6-104-12
SWITCHES		
SW1	120/240 slide switch	60-54
SW2	NOR/LOW slide switch	60-608
SW3	rocker switch	60-619
TRANSFORMER - YOKE		
T1	Power transformer	54-965
T2	Yoke	58-19
ASSEMBLIES		
	12-key keypad	64-864
	4-key keypad (Off Line, f_1, f_2, f_3)	64-865
	4-key keypad (f_4, f_5, Erase, Blue)	64-866
	4-key keypad (Red, Gray ReSet, Break)	64-872
	Keyboard consisting of:	181-3051
	60-key keypad	64-863
	Circuit board	85-2223-1
	#4 x 3/8" self-tapping screw	250-186

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
BRACKET - PLATE - CLAMP		
	Keyboard bracket	204-2362
	Circuit board mounting bracket	204-2396
	Capacitor support bracket	204-182
	Bezel mounting plate	204-2361
	Latch plate	205-2776-1
	Detent plate	205-1775
	Front panel mounting plate	205-1777
	Connector plate	205-1784-1
	Capacitor mounting clamp	207-86
CABINET PARTS		
	Terminal base	90-1236-1
	Cabinet shell	90-1237-1
	Front panel	90-1239-1
	Keyboard cover	90-1238-1
	Bezel cover	90-1244-1
	Foot	261-6
CONNECTORS - PLUG - SOCKETS - PINS		
	Large spring connector	432-753
	Small spring connector	432-866
	4-hole connector shell	432-954
	3-hole connector shell	432-865
	Socket pin	432-932
	8-hole connector shell	432-1022
	34-pin plug	432-1053
	Terminal pin	432-1078
	40-pin IC socket	434-253
	16-pin IC socket	434-299
HARDWARE		
#4 Hardware		
	4-40 x 3/8" black screw	250-392
	#4 x 3/8" self-tapping screw	250-186
	4-40 nut	252-2
	#4 lockwasher	254-9
	#4 solder lug	259-9

(continued)

Chassis (continued)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
	Hardware (continued)	
	#6 Hardware	
	#6 x 1/4" black sheet metal screw	250-369
	6-32 x 1/4" screw	255-56
	6-32 x 3/8" flat head screw	250-434
	6-32 x 3/8" screw	250-89
	6-32 x 3/8" hex head screw	250-1264
	6-32 x 1/2" screw	250-162
	#6 x 5/8" black self-tapping screw	250-1275
	Detent screw	250-1287
	6-32 nut	252-3
	#6 flat washer	253-96
	#6 lockwasher	254-1
	Brass insert	252-719
	#6 solder lug	259-1
	Spacer	255-753
	#8 Hardware	
	8-32 x 1/2" screw	250-585
	8-32 x 3/4" screw	250-72
	8-32 nut	252-4
	#8 flat washer	253-45
	#8 lockwasher	254-2
	#8 solder lug	259-2
	#10 Hardware	
	10-32 x 1" screw	250-331
	#10 x 1-1/2" self-tapping screw	250-261
	#10 flat washer	253-98
	#10 solder lug	259-5
	Ground connector	432-1077
	Small spring	258-4
	Large spring	258-33
	HARNESS - CABLES - WIRE	
	Line cord	89-54
	Interconnect cable	134-1070
	Flat cable	134-1066
	Harness	134-1067
	10' extension cable	134-1076
	Bare wire	340-8
	Black wire	344-50
	Yellow wire	344-54
	Violet wire	344-57
	Brown wire	344-126
	Green wire	344-155

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
	MISCELLANEOUS	
	CRT	411-838
	Rubber grommet	73-59
	3/4" x 5" foam gasket	73-92
	Line cord strain relief	75-754
	AC chassis	204-2395-1
	Alignment tool blade	205-778
	Video circuit board heat sink	215-632
	Logic circuit board heat sink	215-642
	Hinge	265-36
	Plastic retainer	266-929
	Nylon guide	266-944
	Vibratite	352-33
	Small cable tie	354-5
	Large cable tie	354-7
	Model label	390-1522
	Blue and white label	391-34
	Speaker	401-163
	Fuseholder	423-11
	Alignment tool	490-1
	Nut starter	490-5
	Solder wick	490-185
	IC puller	490-189
	Assembly Manual	595-2191
	Operation Manual	595-2284
	Parts Order Form	597-260
	Test circuit board	85-2341-1

TERMINAL LOGIC CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C401 thru C409	2.2 µF	25-221
C411	47 pF	20-101
C412	.01 µF	21-176
C413	150 pF	20-103
C414	47 µF	25-223
C415	2.2 µF	25-221
C416	.1 µF (104M) 50V	21-192
C417	2.2 µF	25-221
C418	2.2 µF	25-221
C419	.005 µF	21-46
C422 thru C429	.1 µF, 10V	21-95
C431 thru C436	.1 µF, 10V	21-95
C438 thru C440	.1 µF, 10V	21-95
C441 thru C445	.05 µF	21-143
C446 thru C449	.1 µF, 10V	21-95
C451 thru C459	.1 µF, 10V	21-95
C462 thru C469	.1 µF, 10V	21-95
C471 thru C474	.1 µF, 10V	21-95
DIODES		
D401	1N4149	56-56
D402	1N4149	56-56
PLUGS		
P401	10-pin	432-1064
P402	3-pin	432-986
P403	34-pin	432-1052
P404	15-pin	432-1067
TRANSISTOR		
Q401	MPS2369	417-937

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTORS		
R401 thru R403	2200 Ω	6-222-12
R404	560 Ω	6-561-12
R405	560 Ω	6-561-12
R406	330 Ω	6-331-12
R407	10 kΩ	6-103-12
R408	1000 Ω	6-102-12
R409	1000 Ω	6-102-12
R411	220 kΩ	6-224-12
R412	220 kΩ	6-224-12
R413	10 kΩ	6-103-12
R414	100 kΩ	6-104-12
R415 thru R419	10 kΩ	6-103-12
R421 thru R429	10 kΩ	6-103-12
R431 thru R439	10 kΩ	6-103-12
R441 thru R445	10 kΩ	6-103-12
R446	1000 Ω	6-102-12
RP1	220 kΩ resistor network	9-98
RP2	220 kΩ resistor network	9-98
SWITCHES		
S401	Dip switch	60-621
S402	Dip switch	60-621
INTEGRATED CIRCUITS		
U401	7805 5V regulator	442-54
U402	7805 5V regulator	442-54
U403	78M12 +12V regulator	442-663
U404	79M12 -12V regulator	442-664
U405	7905.2 -5.2V regulator	442-630
U411	7404	443-18

(continued)

Terminal Logic Circuit Board (continued)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
Integrated Circuits (continued)		
U412	74LS161	443-757
U413	7492	443-34
U414	14040 or CD4040	443-760
U415	74LS132	443-792
U416	74LS00	443-728
U417	96L02	443-727
U418	74LS138	443-877
U419	74LS138	443-877
U421	Z80	443-881
U422	2716 PROM	444-53
U423	2716 PROM	444-45
U424	2112-2	443-721
U425	2112-2	443-721
U426	74LS293	443-733
U427	74LS02	443-779
U428	74LS74	443-730
U429	74LS32	443-875
U430	2316 ROM	444-29
U431	5740	443-913
U432	74LS74	443-730
U433	74LS244	443-791
U434	74LS244	443-791
U435	7404	443-18
U436	14093	443-778
U437	74LS244	443-791
U451	8250	443-874
U452	1488 or 75188	443-794
U453	1489A or 75189A	443-795
U461	6845	443-906
U462	74LS74	443-730
U463	74LS157	443-799
U464	74LS157	443-799
U465	74LS157	443-799
U466	74LS00	443-728
U467 thru U470	2114 or 40L45	443-764
U471	74LS245	443-885
U472	74LS273	443-805
U473	2316 ROM	444-37
U474	74LS166	443-892
U475	74S86	443-915
U476	74LS273	443-805
U477	74LS08	443-780
U478	74S74	443-900
U479	74LS86	443-891
CRYSTAL		
Y401	12.288 MHz crystal	404-613

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
HARDWARE		
	6-32 x 5/16" screw	250-587
	#6 lockwasher	254-1
	6-32 nut	252-3
SOCKETS		
	40-pin IC socket	434-253
	14-pin IC socket	434-298
	16-pin IC socket	434-299
	24-pin IC socket	434-307
	18-pin IC socket	434-310
	20-pin IC socket	434-311
MISCELLANEOUS		
	Double-stick tape	73-151
	Insulating paper	75-738
	Logic circuit board	85-2237-2

POWER SUPPLY CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C101	10,000 µF electrolytic	25-902
C102	470 µF electrolytic	25-891
C104	470 µF electrolytic	25-891
DIODES		
D101 thru D104	1N4002	57-65
D105 thru D108	3A1	57-42
D109 thru D112	1N4002	57-65

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CONNECTORS		
P101	8-pin connector	432-876
P102	8-pin connector	432-876
MISCELLANEOUS		
	Power supply circuit board	85-2173-1
	Sleeving	346-21

VIDEO CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C201	.001 µF	21-140
C202	10 µF	25-865
C203	.01 µF	21-176
C204	10 µF	25-220
C205	10 µF	25-220
C206	.01 µF	21-176
C207	390 pF	20-106
C208	.01 µF	21-176
C209	47 µF	25-883
C211	.22 µF	27-145
C212	.22 µF	27-145
C213	4.7 µF	25-841
C214	6800 pF	29-32
C215	10 µF	25-865
C216	56 pF	21-121
C217	330 µF	25-890
C218	100 pF	21-75
C219	.01 µF	21-176
C221	4700 pF	29-22
C222	100 pF	21-75
C223	.01 µF	21-176
C224	4700 pF	29-22
C225	.047 µF	27-73
C226	22 µF	25-882
C227	10 µF	25-220
C228	22 µF	25-882
C229	.006 µF	29-56
C231	1.5 µF	25-299
C232	.22 µF	29-57
C233	1 µF	27-206
C234	.005 µF	21-193
C235	22 µF	25-882
C236 thru C238	.02 µF	21-122
CONTROLS		
R216	500 Ω	10-918
R226	20 kΩ	10-390
R228	20 kΩ	10-390
R253	5000 Ω	10-311
R268	100 kΩ	10-941
R271	2 M Ω	10-1049

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
DIODES		
D201	1N4149	56-56
D202	MZ2360	56-73
D203	12.8V zener	56-94
D204	1N4149	56-56
D205	1N709A	56-58
D206	FD333	56-93
D207	1N4149	56-56
D208	MR508	57-614
D209	1N2071	57-27
D211	DRS110	57-64
D212	1N2071	57-27
D213	1N4149	56-56
INDUCTORS - CHOKES		
L201	4.65 µH	45-39
L202	620 µH	40-581
L203	8.75 µH	45-42
L204	19 µH	40-1947
L205	52 µH	40-1948
TRANSISTORS		
Q201	MPU131	417-823
Q202	MPSA65	417-885
Q203	MPSA56	417-822
Q204	MPSA06	417-821
Q205	MPSJ06	417-926
Q206	MPSJ06	417-926
Q207	MJE182	417-932
Q208	MJE172	417-924
Q209	MPSL01	417-811
Q211	MJE172	417-924
Q212	2N3906	417-874
Q213	MJ2841	417-282
Q214	MPSU10	417-834
Q215	2N3904	417-875
Q216	MJE340	417-195
Q217	BU500	417-923
Q218	MPSA93	417-927

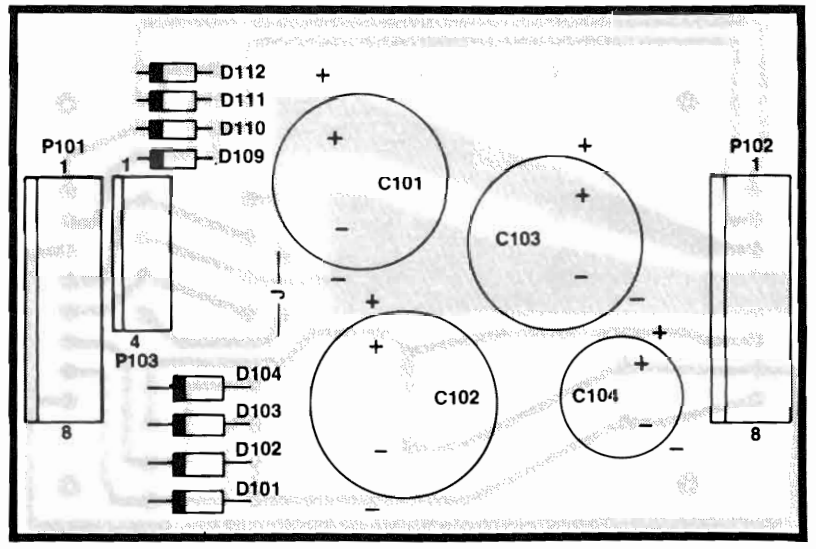
(continued)

Video Circuit Board (continued)

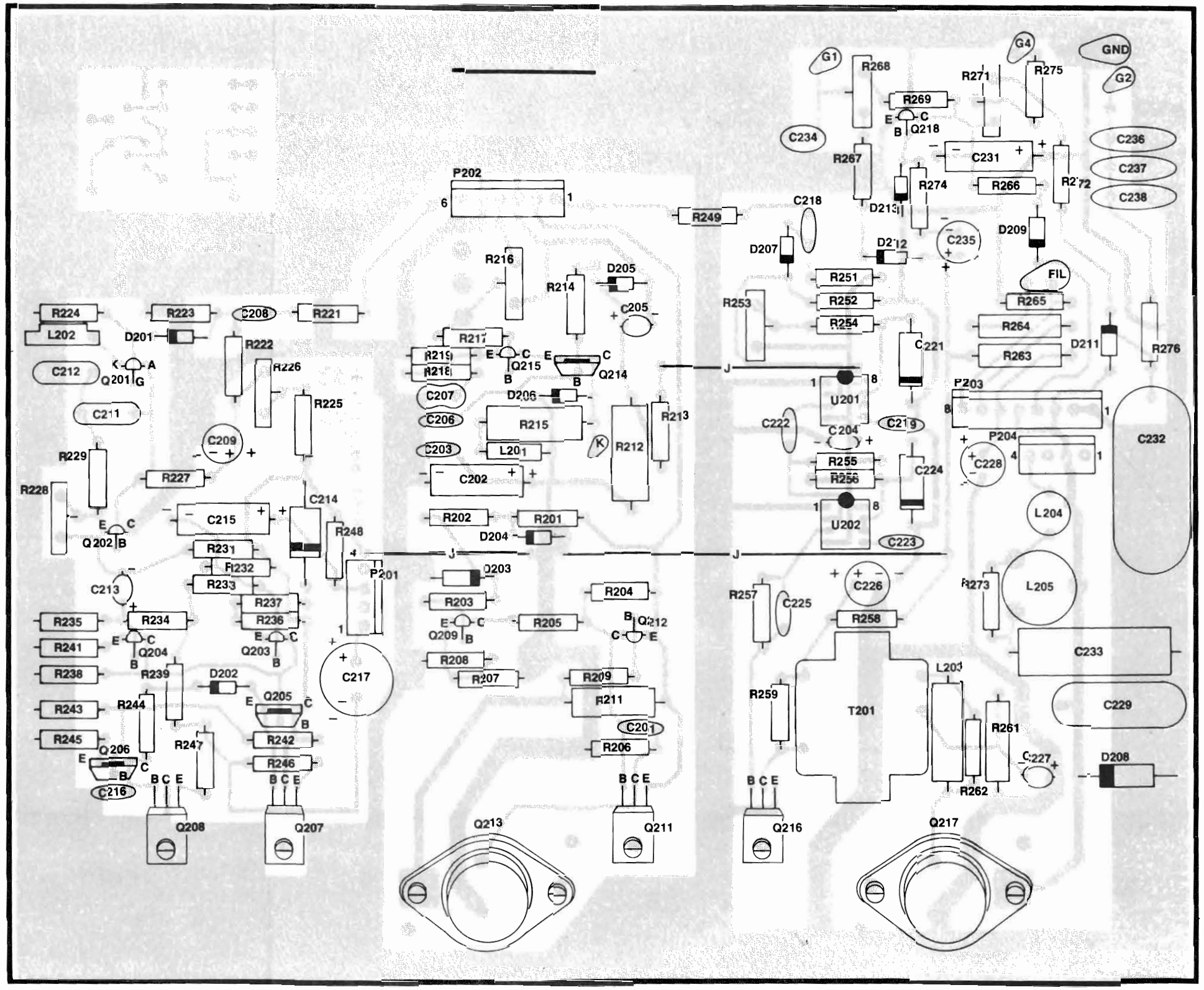
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTORS		
R201	1 MΩ	6-105
R202	4700 Ω	6-472
R203	1000 Ω	6-102
R204	6800 Ω	6-682
R205	4700 Ω	6-472
R206	100 Ω	6-101
R207	6490 Ω,1%	6-6491
R208	1870 Ω, 1/4-watt,1%	6-1871-12
R209	1000 Ω	6-102
R211	.51 Ω, 2-watt	3-6-2
R212	1500 Ω, 2-watt, 10%	1-14-2
R213	47 Ω	6-470
R214	1000 Ω	6-102
R215	820 Ω, 2-watt	1-50-2
R217	75 Ω	6-750
R218	33 Ω	6-330
R219	22 Ω	6-220
R221	470 Ω	6-471
R222	1500 Ω	6-152
R223	3300 Ω	6-332
R224	100 kΩ	6-104
R225	22 kΩ	6-223
R227	220 kΩ	6-224
R229	27 kΩ	6-273
R231	8200 Ω	6-822
R232	10 kΩ	6-103
R233	62 kΩ	6-623
R234	47 kΩ	6-473
R235	10 kΩ	6-103
R236	1200 Ω	6-122
R237	100 Ω	6-101
R238	1 MΩ	6-105
R239	10 kΩ	6-103
R241	1800 Ω	6-182
R242	22 kΩ	6-223
R243	2200 Ω	6-222
R244	15 Ω	6-150
R245	470 Ω	6-471
R246	2.7 Ω	6-279
R247	2.7 Ω	6-279
R248	4.7 Ω	6-479
R249	1000 Ω	6-102
R251	22 kΩ	6-223
R252	27 kΩ	6-273
R254	8200 Ω	6-822
R255	27 kΩ	6-273
R256	3900 Ω	6-392
R257	200 Ω	6-201
R258	47 Ω	6-470
R259	3900 Ω	6-392
R261	1.2 Ω, 2-watt, 10%	3-22-2
R262	100 Ω	6-101
R263	1.2 Ω, 2-watt, 10%	3-22-2
R264	1.2 Ω, 2-watt, 10%	3-22-2
R265	100 kΩ	6-104
R266	330 Ω	6-331
R267	82 kΩ	6-823
R269	82 kΩ	6-823
R272	390 kΩ	6-394
R273	1000 Ω	6-102
R274	4700 Ω	6-472
R275	3.3 MΩ	6-335
R276	3.3 MΩ	6-335

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
TRANSFORMERS		
T201	Driver transformer	51-197
T202	Flyback transformer	51-196
INTEGRATED CIRCUITS		
U201	NE555	442-53
U202	NE555	442-53
CONNECTORS - SOCKETS		
	Push-on connector	432-66
	Spring connector	432-753
	6-pin plug	432-825
	4-pin plug	432-827
	8-pin plug	432-876
	8-hole connector shell	432-1022
	CRT socket with leads	434-326
	8-pin IC socket	434-230
HARDWARE		
	4-40 x 1/2" screw	250-34
	4-40 x 5/8" screw	250-323
	6-32 x 5/16" screw	250-587
	4-40 nut	252-2
	6-32 nut	252-3
	Fiber washer	253-126
	#4 lockwasher	254-9
	#6 lockwasher	254-1
INSULATORS		
	Large transistor insulator	75-140
	Transistor cover	75-142
	Small transistor insulator	75-204
MISCELLANEOUS		
	Black stranded wire	344-15
	Thermal compound	352-31
	Small cable tie	354-5
	DANGER label	390-147
	Video circuit board	85-2165-1

CIRCUIT BOARD X-RAY VIEWS



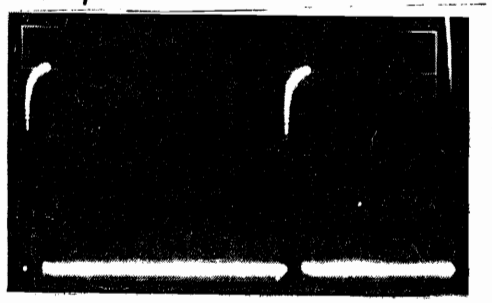
POWER SUPPLY



VIDEO CIRCUIT BOARD

ADDRESS BUS & MISCELLANEOUS WAVEFORMS

H SYNC
10 μS/DIV 1 V/DIV



V SYNC
2 mS/DIV 1 V/DIV



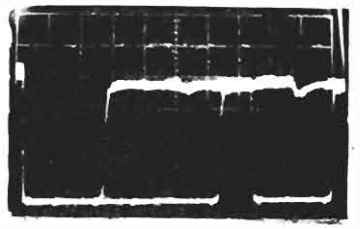
Z80 $\overline{RD}$
0.2 μS/DIV 1 V/DIV



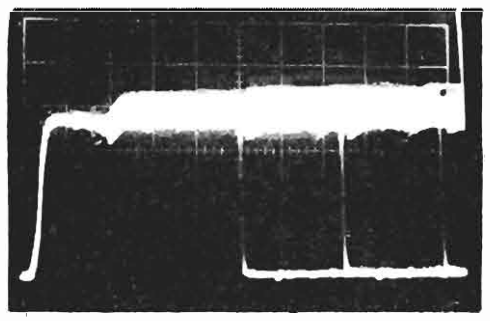
Z80 $\overline{M1}$
0.2 μS/DIV 1 V/DIV



Z80 $\overline{WR}$
0.2 μS/DIV 1 V/DIV

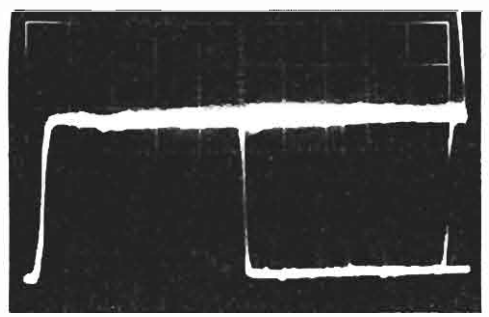


A0



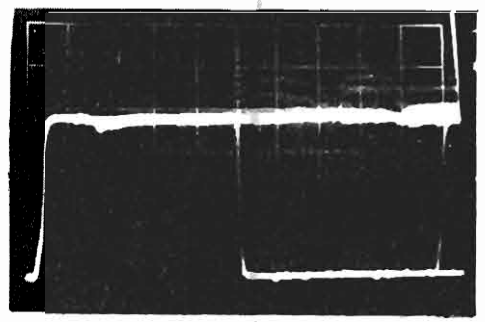
0.2 μS/DIV 1V/DIV

A3



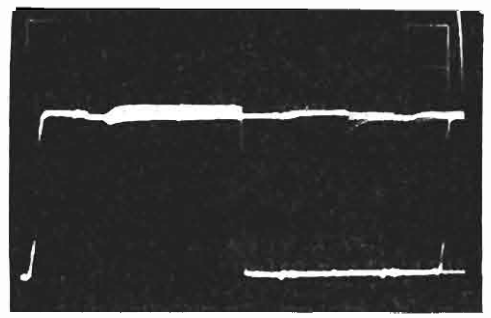
0.2 μS/DIV 1 V/DIV

A6



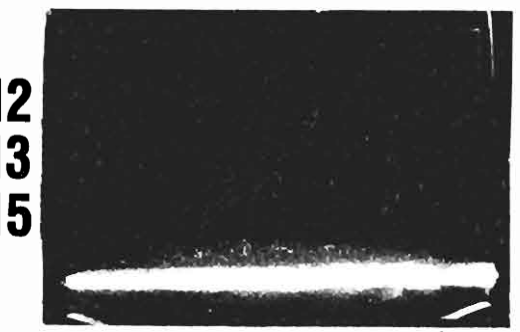
0.2 μS/DIV 1 V/DIV

A9



0.2 μS/DIV 1 V/DIV

A12
A13
A15



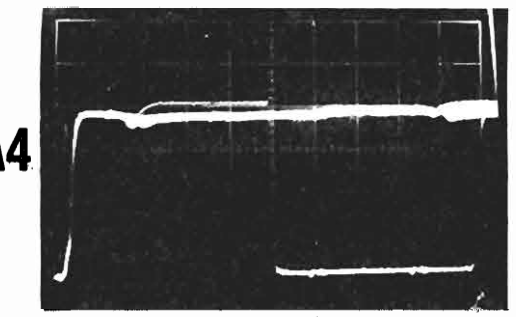
0.5 μS/DIV 1 V/DIV

A1



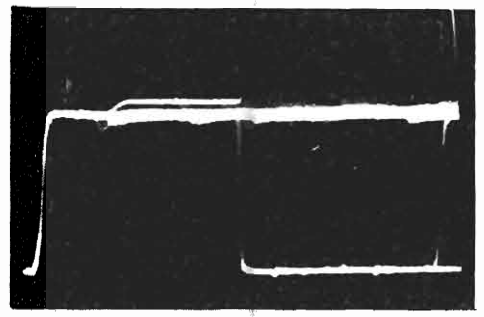
0.2 μS/DIV 1 V/DIV

A4



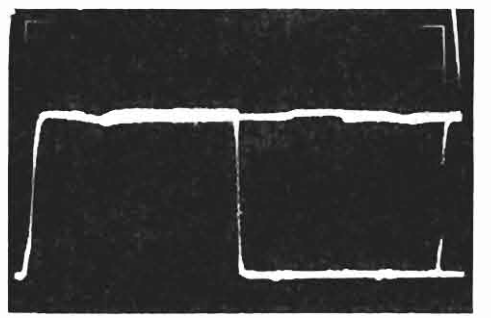
0.2 μS/DIV 1 V/DIV

A7



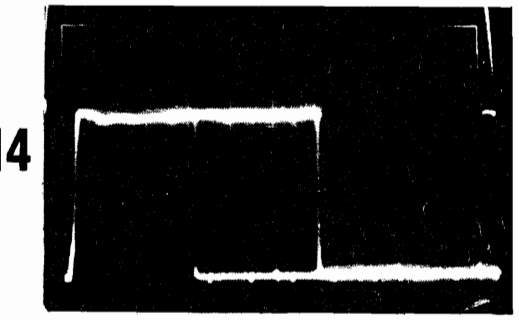
0.2 μS/DIV 1 V/DIV

A10



0.2 μS/DIV 1 V/DIV

A14



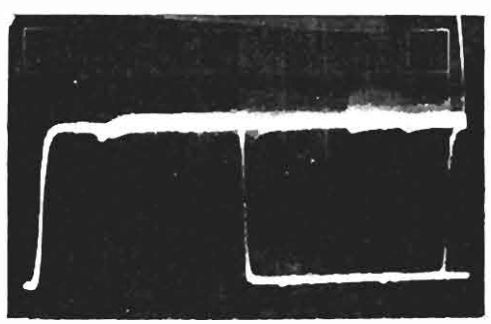
0.5 μS/DIV 1 V/DIV

A2



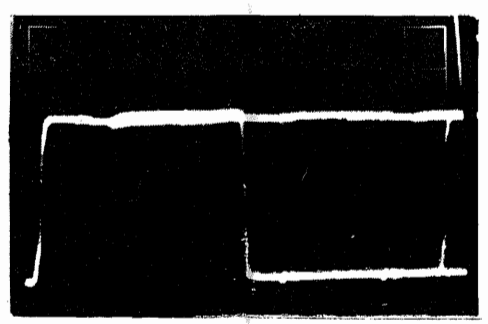
0.2 μS/DIV 1 V/DIV

A5



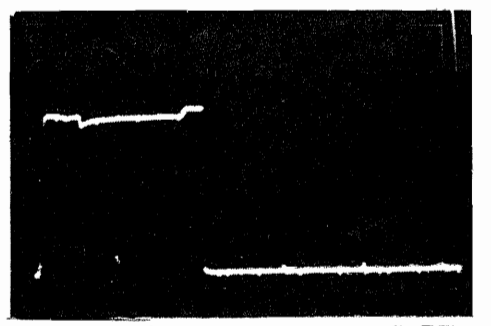
0.2 μS/DIV 1 V/DIV

A8

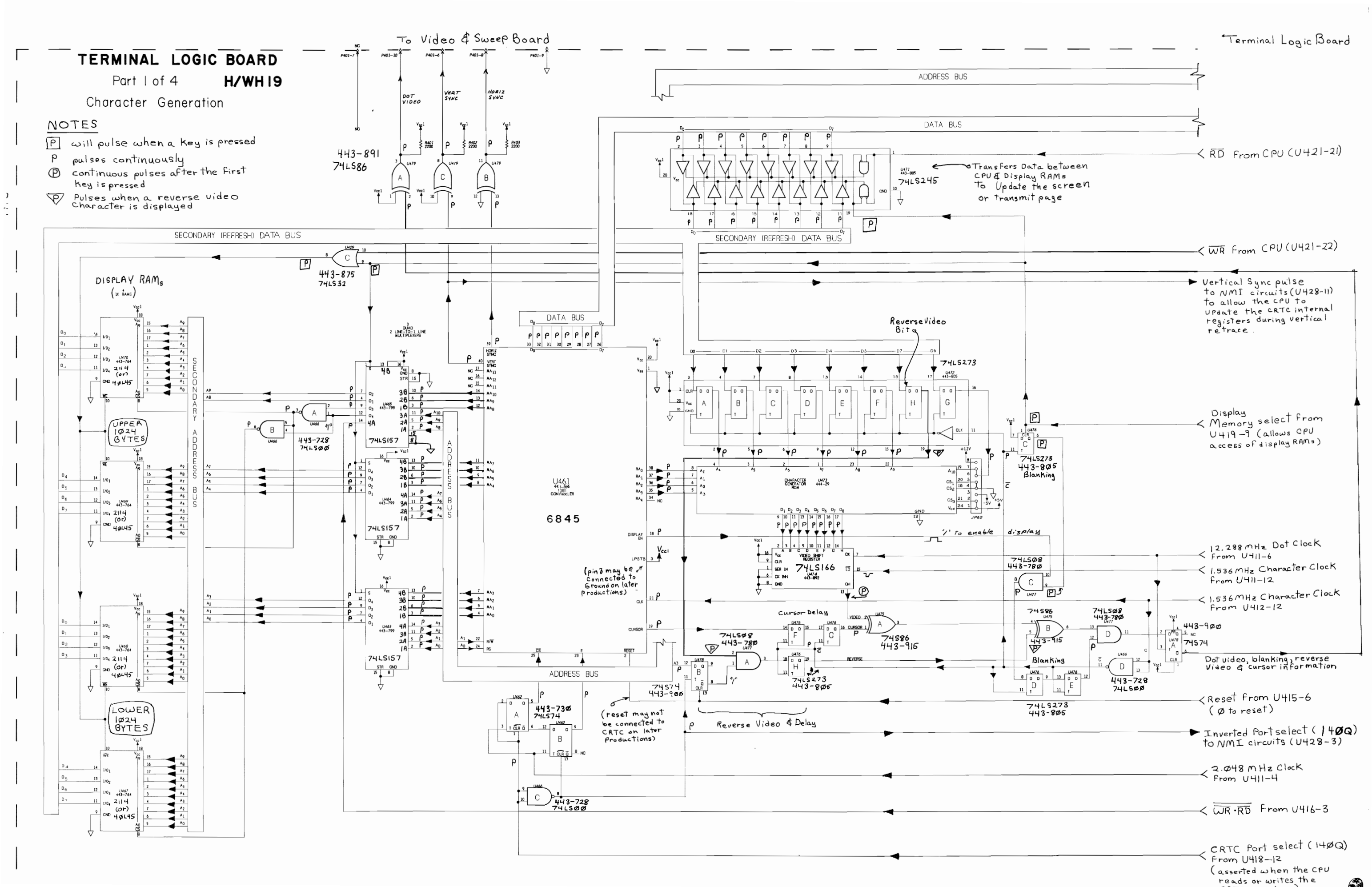


0.2 μS/DIV 1 V/DIV

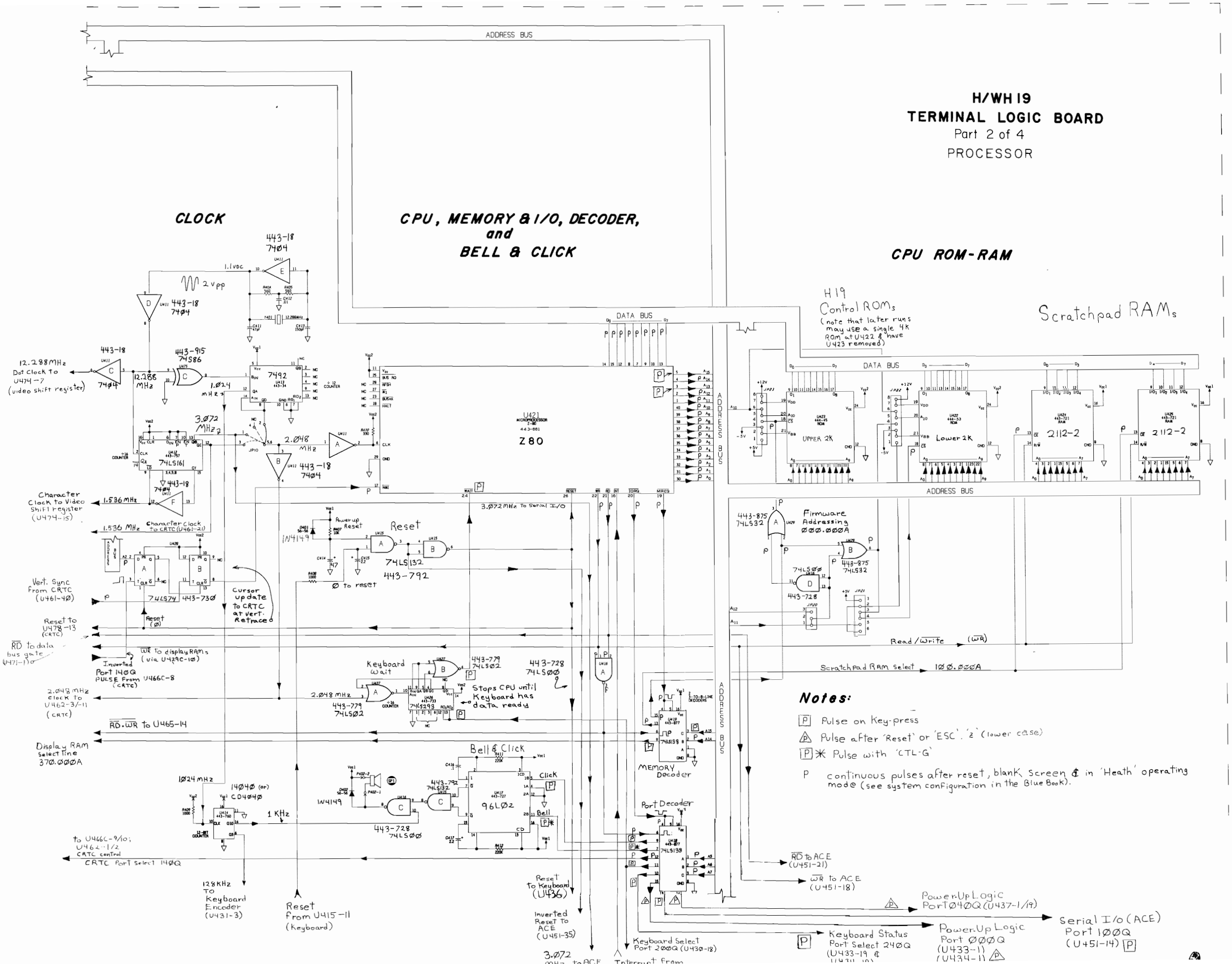
A11



0.5 μS/DIV 1 V/DIV



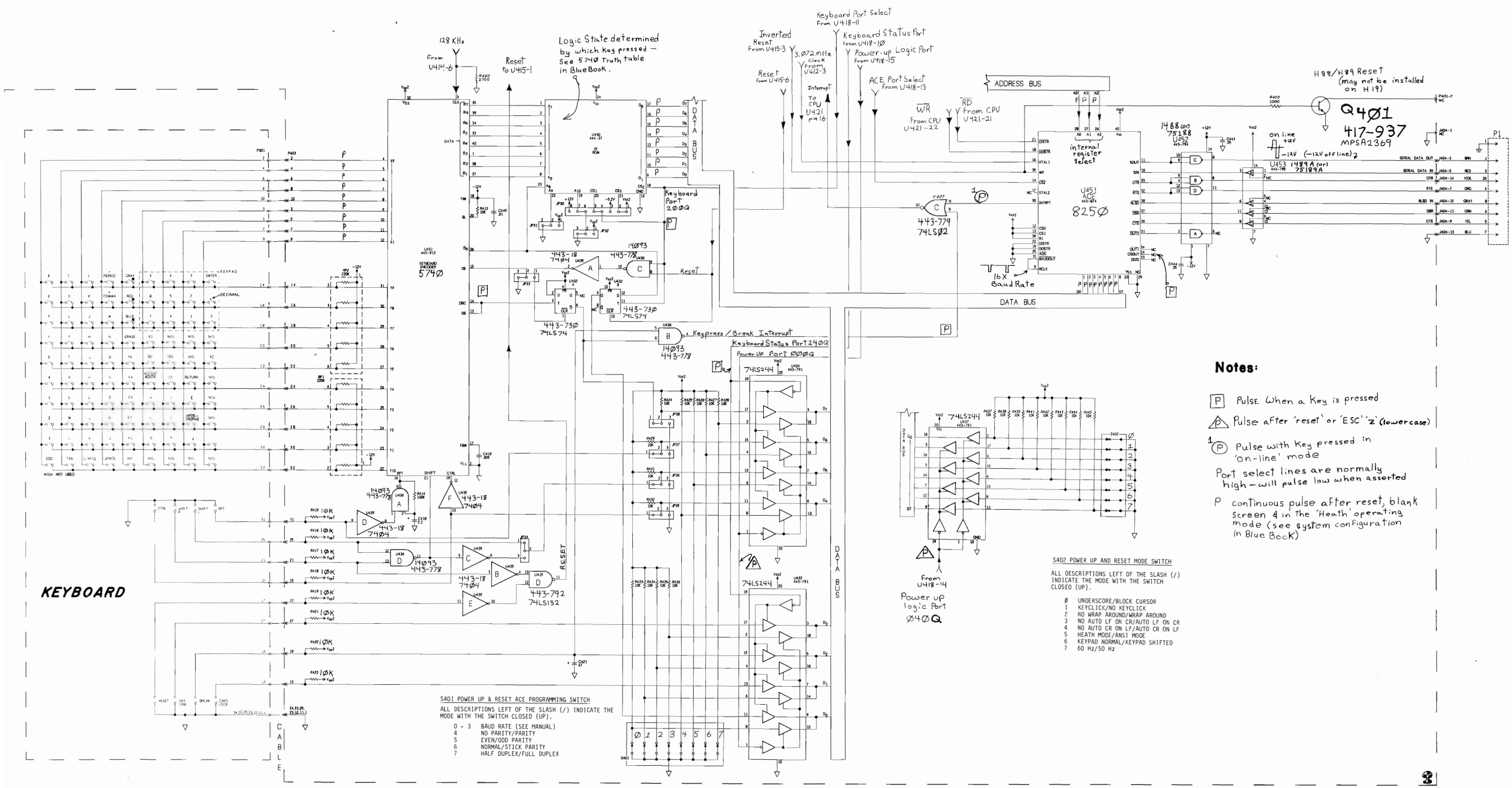
TERMINAL LOGIC BOARD
Part 1 of 4
H/WH19
Character Generation
NOTES
P will pulse when a key is pressed
P pulses continuously
P continuous pulses after the first key is pressed
P Pulses when a reverse video Character is displayed
To Video & Sweep Board
Terminal Logic Board
ADDRESS BUS
DATA BUS
SECONDARY (REFRESH) DATA BUS
DISPLAY RAMs
UPPER 1024 BYTES
LOWER 1024 BYTES
SECONDARY ADDRESS BUS
ADDRESS BUS
DOT VIDEO
VERT SYNC
HORIZ SYNC
443-891
74LS86
443-875
74LS32
443-728
74LS00
74LS157
U461
6845
74LS273
74LS245
Transfers Data between CPU & Display RAMs to Update the screen or transmit page
RD From CPU (U421-21)
WR From CPU (U421-22)
Vertical Sync pulse to NMI circuits (U428-11) to allow the CPU to update the CRTC internal registers during vertical retrace.
Reverse Video Bit
Display Memory select from U419-9 (allows CPU access of display RAMs)
74LS273
443-805
Blanking
'1' to enable display
74LS166
12.288 MHz Dot Clock From U411-6
1.536 MHz Character Clock From U411-12
1.536 MHz Character Clock From U412-12
74LS08
443-780
74S86
443-915
Cursor Delay
74S74
443-900
Dot video, blanking, reverse Video & cursor information
Reset From U415-6 (0 to reset)
Inverted Port select (140Q) to NMI circuits (U428-3)
2.048 MHz Clock From U411-4
WR·RD From U416-3
CRTC Port select (140Q) From U418-12 (asserted when the CPU reads or writes the
(pin 3 may be connected to Ground on later Productions)
(reset may not be connected to CRTC on later Productions)
Reverse Video & Delay
443-730
74LS74


H/WH 19
TERMINAL LOGIC BOARD
Part 2 of 4
PROCESSOR
CLOCK
CPU, MEMORY & I/O, DECODER, and BELL & CLICK
CPU ROM-RAM
ADDRESS BUS
DATA BUS
H19 Control ROMs (note that later runs may use a single 4K ROM at U422 & have U423 removed)
Scratchpad RAMs
Z80
Reset
Keyboard Wait
Bell & Click
Port Decoder
Memory Decoder
Firmware Addressing 000.000A
Read/Write (WR)
Scratchpad RAM Select 100.000A
Notes:
Pulse on Key-press
Pulse after 'Reset' or 'ESC'. 'z' (lower case)
Pulse with 'CTL-G'
P continuous pulses after reset, blank screen & in 'Heath' operating mode (see system configuration in the Blue Book).
Power-Up Logic Port 040Q (U437-1/19)
Serial I/O (ACE) Port 100Q (U451-14)
Keyboard Status Port Select 240Q (U433-19 & U434-19)
Power-Up Logic Port 000Q (U433-1) (U434-1)
Keyboard Select Port 200Q (U430-18)
Reset to Keyboard (U436)
Inverted Reset to ACE (U451-35)
Reset From U415-11 (Keyboard)
128KHz To Keyboard Encoder (U431-3)
to U466C-9/10; U462-1/2 CRTC control
CRTC Port Select 140Q
Display RAM Select line 370.000A
RD·WR to U465-14
2.048 MHz clock to U462-3/-11 (CRTC)
RD to data bus gate (U471-1)
Reset to U478-13 (CRTC)
Vert. Sync From CRTC (U461-40)
Character Clock to Video Shift register (U474-15)
Character Clock to CRTC (U461-21)
Cursor update to CRTC at Vert. Retrace
Inverted Port 140Q PULSE From U466C-8 (CRTC)
Stops CPU until Keyboard has data ready
Power-up Reset
Ø to reset
3.072 MHz to Serial I/O
12.288 MHz Dot Clock to U474-7 (video shift register)
1.536 MHz
1.024 MHz
3.072 MHz
2.048 MHz
1 KHz
2 vpp
1.1 VDC
443-18 7404
443-915 74S86
7492
74LS161
74LS74
443-730
74LS132
443-792
74LS293
443-779 74LS02
443-728 74LS00
96L02
74LS138
74LS139
443-875 74LS32
443-728
U421 MICROPROCESSOR Z-80 443-881
U422 444-45 ROM
U423 444-53 ROM
U424 443-721 RAM
U425 443-721 RAM
UPPER 2K
Lower 2K
2112-2
2112-2

TERMINAL LOGIC BOARD
Part 3 of 4
KEYBOARD ENCODER

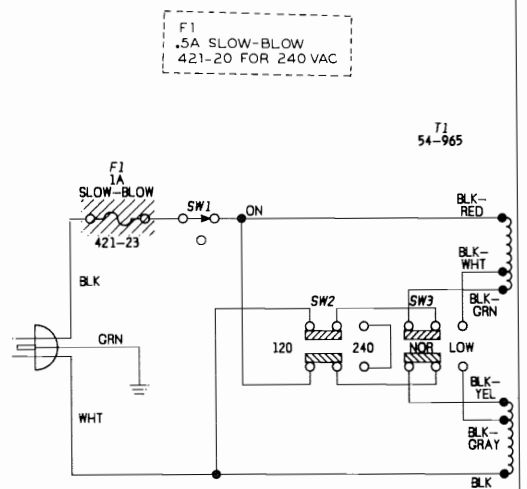
KEYBOARD STATUS & POWER-UP LOGIC

SERIAL I/O



Notes:

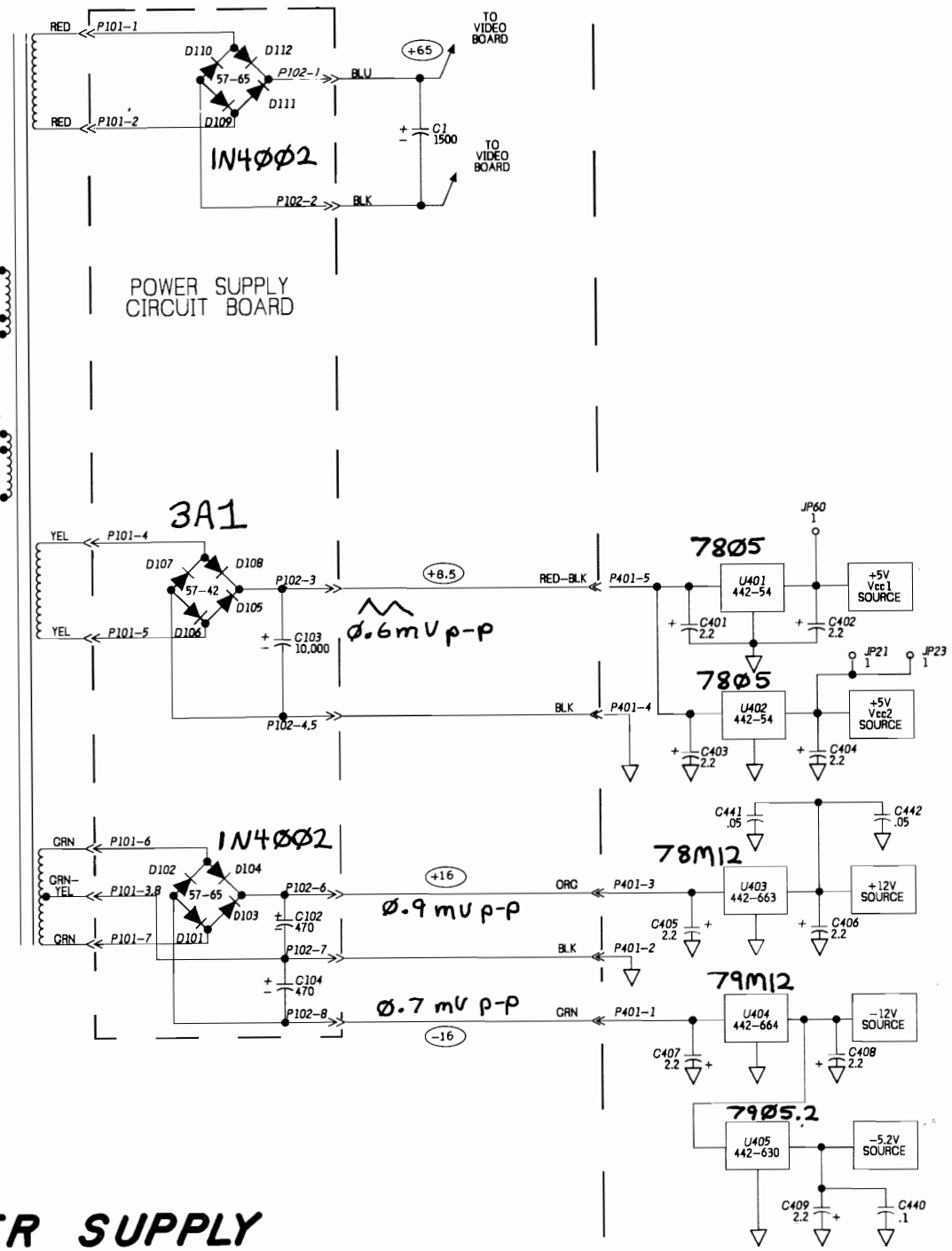
- [P] Pulse When a Key is pressed
- [P] Pulse after 'reset' or 'ESC' 'z' (lowercase)
- [P] Pulse with Key pressed in 'on-line' mode
- Port select lines are normally high — will pulse low when asserted
- P continuous pulse after reset, blank screen & in the 'Heath' operating mode (see system configuration in Blue Book)



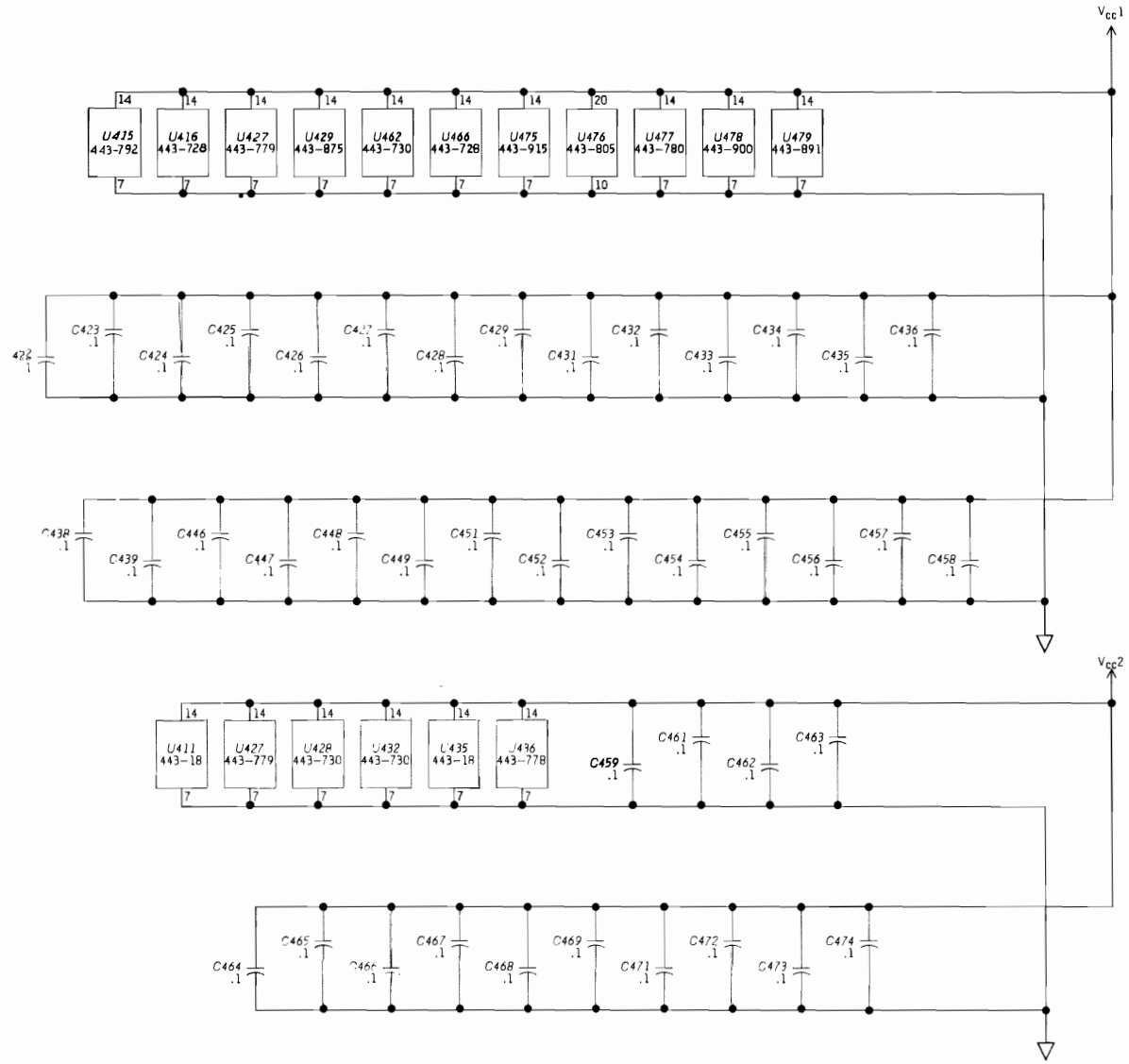
Primary Current:

= .5 Ampere w/blank screen

= .52 Ampere w/screen filled with reverse video spaces



POWER SUPPLY



H/WH19
TERMINAL LOGIC BOARD

Part 4 of 4

POWER SUPPLY

VIDEO TERMINAL
H/WH 19

NOTES:

1. COMPONENT NUMBERS ARE IN THE FOLLOWING GROUPS:
   - 1- 99 PARTS MOUNTED ON THE CHASSIS.
   - 101-199 PARTS MOUNTED ON THE POWER SUPPLY CIRCUIT BOARD.
   - 201-299 PARTS MOUNTED ON THE VIDEO CIRCUIT BOARD.
   - 301-399 PARTS MOUNTED ON THE KEYBOARD CIRCUIT BOARD.
   - 401-499 PARTS MOUNTED ON THE TERMINAL LOGIC CIRCUIT BOARD.

2. RESISTORS MOUNTED ON THE VIDEO CIRCUIT BOARD ARE 1/2-WATT, 5% UNLESS MARKED OTHERWISE. RESISTORS MOUNTED ON THE LOGIC CIRCUIT BOARD ARE 1/4-WATT, 5% UNLESS MARKED OTHERWISE. RESISTOR VALUES ARE IN OHMS (k=1,000; M=1,000,000).

3. ALL CAPACITORS ARE IN µF UNLESS MARKED OTHERWISE.

4. ⏚ THIS SYMBOL INDICATES CHASSIS GROUND.

5. ▽ THIS SYMBOL INDICATES CIRCUIT BOARD GROUND.

6. □ THIS SYMBOL INDICATES WHERE A WIRE CONNECTS TO A CIRCUIT BOARD.

7. →> THIS SYMBOL INDICATES A MECHANICAL CONNECTOR.

8. ⬬ THIS SYMBOL INDICATES A PART THAT IS SHOWN ON A CIRCUIT BOARD, BUT IS ACTUALLY MOUNTED ON THE CHASSIS.

9. THIS SYMBOL INDICATES AN INTERRUPTED LINE. LAY A STRAIGHT EDGE ON THE ARROW TO SEE WHERE IT GOES TO OR COMES FROM.

10. ⬭ THIS SYMBOL INDICATES A DC VOLTAGE TAKEN WITH A HIGH IMPEDANCE VOLTMETER FROM THE POINT INDICATED TO CHASSIS GROUND. VOLTAGES MAY VARY ±20%.

11. FUSE F1 IS CRITICAL FOR CONTINUED SAFETY. REPLACE IT ONLY WITH A PART OF THE SAME RATING OR WITH THE PROPER HEATH PART.

12. Voltages taken with primary voltage set to 120 VAC using an IP-5220 Variable AC power supply.

