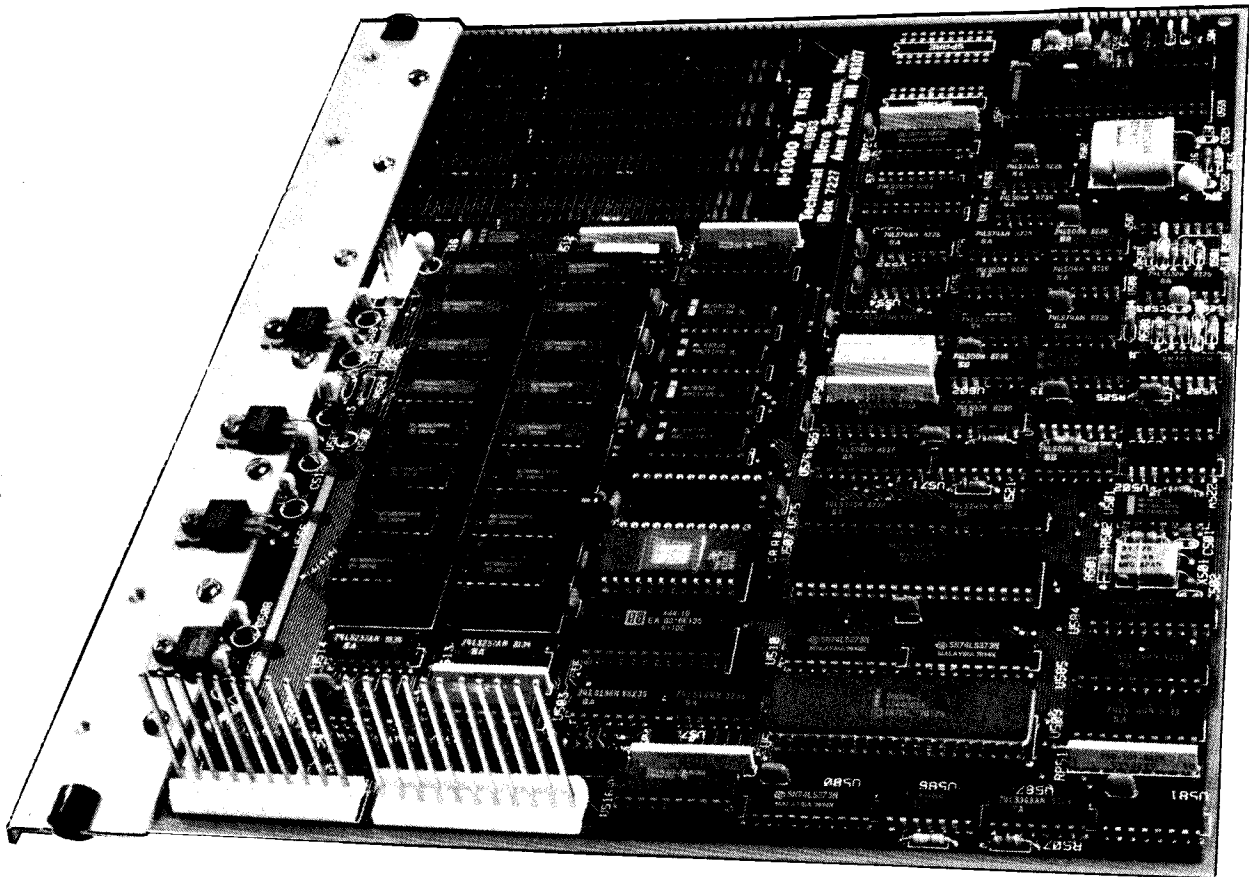

H-1000



Z80/8086 UPGRADE FOR THE H89/Z89

ASSEMBLY AND OPERATION MANUAL

H-1000 SURVEY

We're continuing to develop the H-1000, and need your help. We'd like to know what equipment you have, how you use it, what you like about the H-1000, and what we should do to improve it. Please take a few minutes to answer the following questions.

	HAVE NOW	PLAN TO BUY	NO INTEREST
1. My basic computer is a:			
Heath H88 or H89	[]	[]	[]
Heath H88-A or H89-A	[]	[]	[]
Zenith 289 or 290	[]	[]	[]
Zenith 289-A or 290-A	[]	[]	[]
other _____	[]	[]	[]
2. I have an H-1000 board with:			
128K memory	[]	[]	[]
256K memory	[]	[]	[]
512K memory	[]	[]	[]
1024K memory	[]	[]	[]
3. Disk controllers:			
Heath H17 (5-1/4" hard-sector)	[]	[]	[]
Heath H37 (5-1/4" soft-sector)	[]	[]	[]
Heath H47 (8" floppy)	[]	[]	[]
Heath H67 (8" + Winchester)	[]	[]	[]
CDR FDC-880H (floppy)	[]	[]	[]
Magnolia 77314 (Corvus)	[]	[]	[]
Magnolia 77316 (floppy)	[]	[]	[]
Magnolia 77320 (SASI)	[]	[]	[]
other _____	[]	[]	[]
4. Winchester disk drives:			
5 megabytes	[]	[]	[]
10 megabytes	[]	[]	[]
20 megabytes or more	[]	[]	[]
5. Serial and Parallel I/O boards:			
Heath H-88-3 (3-port serial)	[]	[]	[]
Heath H-88-11 (2 ser., 1 par.)	[]	[]	[]
other _____	[]	[]	[]
6. Graphics boards:			
Cleveland Codonics Imaginator	[]	[]	[]
Northwest Digital Graphics-Plus	[]	[]	[]
other _____	[]	[]	[]
7. Any other accessories (printer, modem, plotter, etc):			
#1 _____	[]	[]	
#2 _____	[]	[]	
#3 _____	[]	[]	
8. Operating Systems I use or am interested in:			
HDOS	[]	[]	[]
CP/M-80 (8-bit)	[]	[]	[]
CP/M-86 (16-bit)	[]	[]	[]
MS-DOS (PC-DOS)	[]	[]	[]
Concurrent DOS	[]	[]	[]
UNIX (KUNIX, VENIX, etc.)	[]	[]	[]

9. Software I am interested in:

#1 _____
#2 _____
#3 _____
#4 _____
#5 _____

HAVE NOW

[]
[]
[]
[]
[]

PLAN TO BUY

[]
[]
[]
[]
[]

10. What feature(s) attracted you to the H-1000 (check all that apply)?

[] speed [] H/Z89 compatibility
[] memory capacity [] H/Z-100 compatibility
[] cost savings [] IBM-PC, H/Z150 compatibility
[] build on current investment
[] other (specify) _____

11. What are your main uses for the H-1000 (check all that apply)?

[] assembly-language programming [] business
[] high-level language programming [] scientific
[] accounting [] spreadsheets
[] database [] word processing
[] educational
[] other _____

12. What features or accessories do you think we should add or improve?

[] Winchester disk system
[] 3rd-part disk controller support (Magnolia, CDR, etc.)
[] additional memory capacity
[] IBM-compatible graphics
[] other _____

13. Your overall rating of the H-1000 would be:

[] excellent [] good [] fair [] poor

14. Do you have any comments on the H-1000, or TMSI in general?

Thank you for your time and consideration. Please fold and seal the survey and return it to TMSI. Be sure to include your return address.

NAME _____

STREET _____

CITY _____ STATE _____ ZIP _____

TO: Technical Micro Systems, Inc.

P.O. Box 7227

Ann Arbor, MI 48107

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Technical Micro Systems, Inc.

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(313) 994-0784

Revision 1.7

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WARRANTY

All Technical Micro Systems Inc. parts and products carry a ninety (90) day limited warranty. If you have any questions or problems with our products, parts, or service, please call or write to us at the address given below, and we'll do our best to help. Sorry, no collect calls.

For a period of ninety (90) days after delivery, Technical Micro Systems Inc. will repair or replace free of charge any part or product found defective in either materials or workmanship. We further warrant that our products will meet the published specifications for a period of ninety (90) days after purchase when assembled and used according to our published instructions. If a defective part or a design error on our part causes a part or product to fail during the warranty period, we will repair or replace it free of charge. Send it to us postpaid and we will reimburse you for the shipping charges.

Our warranty does not cover, and we are not responsible for damage caused by abuse, incorrect assembly, defective tools, or unauthorized modifications. Our warranty does not include reimbursement for inconvenience, loss of use, or customer labor.

This warranty includes only parts and products sold by Technical Micro Systems Inc. and does not cover equipment to which our parts or products may be connected. We are not responsible for incidental or consequential damages. Some states do not allow exclusion of incidental or consequential damages, so this may not apply to you.

Technical Micro Systems, Inc.
P.O. Box 7227
Ann Arbor, MI 48107

(313) 994-0784

INTRODUCTION

The H-1000 is a Z80/8086 upgrade board for the Heath/Zenith H89/Z89 and Z90 series computers. Features of the H-1000 include compatibility with all Heath/Zenith 89-series hardware and software, up to 1 Megabyte of memory, an 8086 with an 8 MHz clock, and a software-selectable 2 or 4 MHz clock for the Z80. Two additional I/O slots also have been added. This manual covers operation, configuration, installation and service.

Chapter 1 tells you how to install the H-1000 in your H/Z89 computer. Only simple hand tools are used, and no technical training or soldering is required.

Chapter 2 provides help in case you have trouble getting your H-1000 to work. It is in "flowchart" form to help zero in on the source of the problem quickly and easily.

Chapter 3 is a description of how the board works from a software point of view. It describes the memory and I/O maps, selecting which CPU is used, and the various modes of operation. Read this chapter if you are interested in writing programs that make use of the special features of the H-1000.

Chapter 4 describes the H-1000 from a hardware point of view. It describes each circuit, and how it works. Read this chapter if you are planning to design or build hardware accessory boards for the H-1000.

Chapter 5 is a complete set of schematics and parts list for the board. You should keep it up to date with any changes or modifications made.

Chapter 6 describes the various jumpers and user-selectable options on the H-1000. Refer to this chapter if you are installing special program ROMs.

Appendix A thru G provide data sheets and technical specifications. See the table of contents for more details.

We believe this manual to be up-to-date and correct, but should any updates or additions be made they will be forwarded to you. If you find any errors or have any suggestions on the manual, we would be happy to hear from you.

CHAPTER 1

INSTALLATION

This chapter describes the installation of the H-1000 in a standard Heath H89- or Zenith Z89-series computer. The H-1000 is not hard to install, but it must be done carefully to avoid costly mistakes. We recommend that you take 15 or 20 minutes to read completely through this chapter BEFORE you begin. This will give you a good idea of what is involved. If you don't feel confident about doing the job yourself, seek the help of someone you trust.

1.01 UNPACKING INSTRUCTIONS

Check to see that you have received all the necessary parts. As you find each item, check it off against the following list. Keep the H-1000 board itself in its protective bag. Besides this manual, you should find:

- () H-1000 board
- () Dr.T Diagnostic disk (hard-sector only)
- () I/O board mounting bracket
- () 11-pin power cable
- () "H-1000" nameplate

If you ordered any memory options, they will come installed on the H-1000 board. If you ordered software with your H-1000, it will be packaged separately with its own packing list. If anything appears to be damaged or missing, please contact us for a replacement at the address or phone number below:

TMSI, c/o Lee Hart
P.O. Box 134
Kalamazoo, MI 48105

Phone (616) 345-2960

1.02 NECESSARY TOOLS AND TEST EQUIPMENT

Installation of an H-1000 requires only simple tools, and no soldering is required. You will need the following:

- Regular 1/4" blade screwdriver
- Regular 1/8" blade screwdriver
- Phillips screwdriver
- 1/4" nut driver, or a small pair of pliers

While not required, it is useful to have the Heath/Zenith manuals handy for your H/Z89 and its I/O boards. An IC extraction tool, and a voltmeter will also be helpful at several stages of the assembly.

1.03 ASSEMBLY NOTES

When you are ready to begin, follow the step-by-step instructions. Read each step completely before you do it. Then perform the tasks indicated, and place a check mark (X) in the space provided. Occasionally, a step will refer to a drawing or diagram to help clarify a particular operation. All such figures are in this book, located as close as possible to the steps that refer to them.

Heath and Zenith have used many different model numbers to describe the various H88/H89 and Z89/Z90 models. For the purpose of this manual they are all the same, so we will simply refer to them all as the H/Z89.

1.04 H/Z89 CHECKOUT

When modifying a piece of equipment, it is important to be sure that it is working properly BEFORE making changes. If you have at least one H17 hard-sector drive, the Dr.T Diagnostics will check out your system before the H-1000 is installed, and again after installation to be sure everything is working correctly.

- () Open the Dr.T diagnostic package and remove the instructions.
- () Follow the instructions for testing your H/Z89.
- () When the tests have run successfully, go to section 1.05. If a test fails, there is either an unusual condition present (non-standard configuration or custom modifications), or something is wrong with your H/Z89. You should:
 - A. Check the instructions that came with the Dr.T diagnostics to see if there are any limitations that would prevent it from working in your system (insufficient memory, wrong disk format, etc.).
 - B. Check for any non - Heath/Zenith accessories in your H/Z89 (disk controllers, special ROMs, 4MHz modifications, etc.). If so, try removing them and running the diagnostics again.
 - C. Consult the trouble-shooting section of your Heath/Zenith Manuals.
 - D. Contact your local Heath store or Zenith service center.
 - E. Finally, if you think your H/Z89 is working and the Dr.T diagnostic says it's not, contact the TMSI Customer Service department.

| DO NOT INSTALL THE H-1000 IN A SYSTEM |
THAT IS NOT WORKING CORRECTLY!

CAUTION!

Hazardous voltages are present in the computer. Be sure the line cord is unplugged whenever the cabinet is open. A high voltage charge may be present on the flyback transformer and picture tube even if unplugged. DON'T TOUCH THESE AREAS!

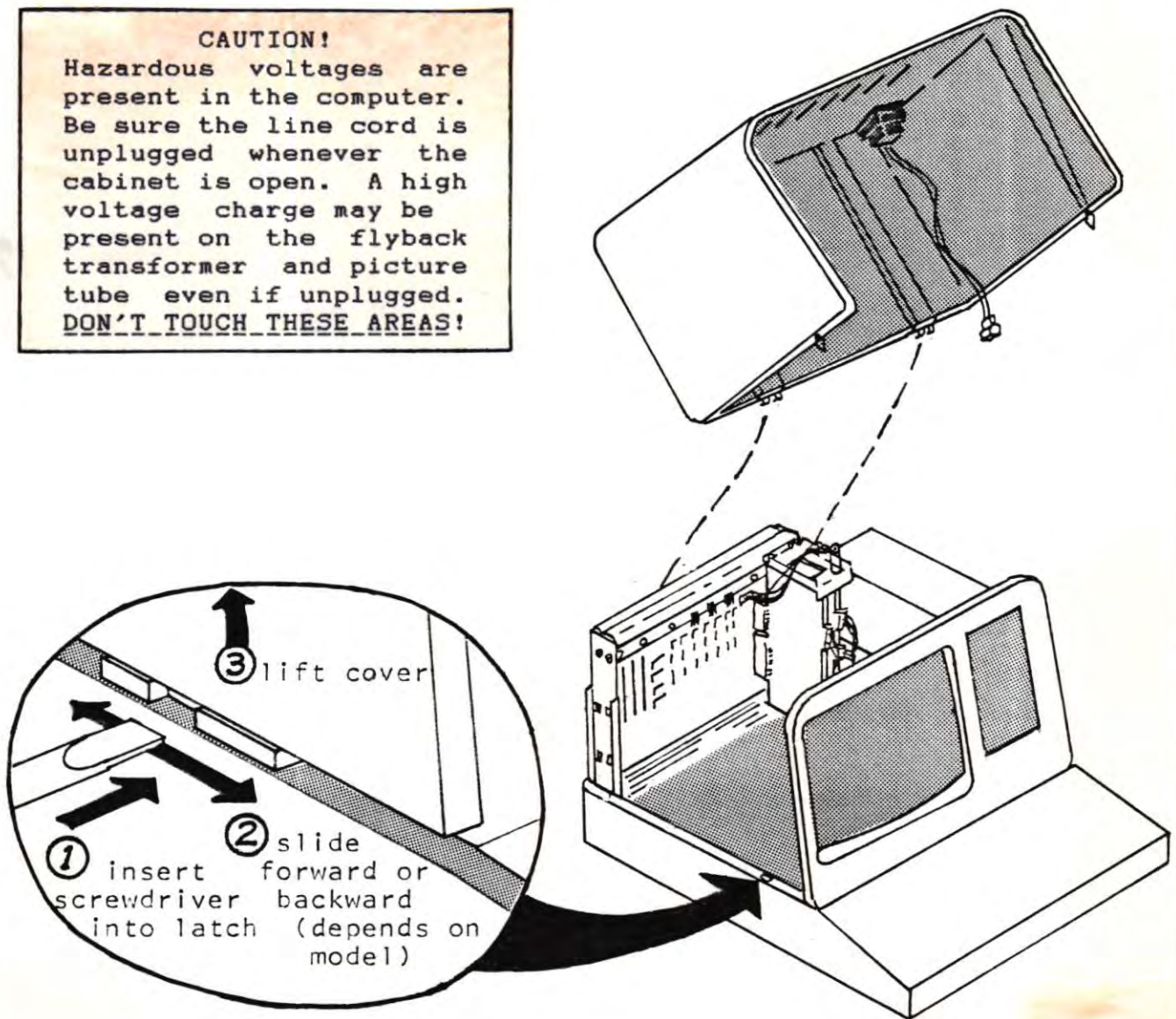


FIG. 1-1 OPENING THE CABINET

1.05 OPENING THE H/Z89 CABINET

- () Turn the machine off and unplug the power cord from the outlet.
- () Locate the two latches on either side of cover (fig. 1-1).
- () Insert a screwdriver blade into the notch on the sliding latch plate, and move it either forward or backward to release the cabinet cover (the direction varies depending on version of H/Z89). Repeat this process with the latch on the other side of the cabinet.
- () Tilt the cover back, and disconnect the fan's power connector.
- () Slide the cover off the machine and set it aside.

1.06 HEAT SINK UPGRADE (OPTIONAL)

Two different heat sink assemblies have been used in H/Z89s. The older assembly is less reliable and should be upgraded. To see which version you have, look at the heat sink assembly in the rear right-hand corner of the cabinet. If it has the black finned heatsinks and a 78H05 regulator at U101 (fig. 1-2) then you have the new assembly; skip ahead to section 1.07. Otherwise, perform the following steps to upgrade the heat sink assembly.

- () Contact your Heath/Zenith dealer or TMSI and request the following parts:
 - 3 black finned heatsinks (Heath 215-685)
 - 78H05 regulator (Heath 442-651)
 - packet of thermal compound (Heath 352-31)
- () Unplug the cable connectors from the power supply board. Note their positions carefully so they can be replaced later.
- () Remove the four screws holding the power supply board. Then remove the board and set it aside.
- () Remove the 4 hex spacers holding the regulator mounting bracket.
- () Position the bracket so you can work on both sides of it. Do not pull it so far that you put any strain on the connecting cables.
- () Remove the two screws holding regulator U102 and set them aside. Then remove U102 from its socket.

| CAUTION: You will be using Dow Corning 340 thermal compound in |
| the following steps. It is not caustic but may cause temporary |
| discomfort if it gets in your eyes. If this should happen, |
| rinse your eyes with warm water. If it gets on your clothing, |
| professional cleaning may be needed. The compound contains |
zinc oxides, silicon dioxides, and traces of carbon dioxide.

- () Coat the mating surfaces of the regulator, a finned heatsink, and the mounting bracket with a THIN coat of thermal compound.
- () Re-install U102 with a finned heatsink between the regulator and bracket as shown in fig. 1-2. Use the original mounting screws.
- () Similarly, install a finned heatsink at U103 (fig. 1-2).
- () Remove the regulator at U101 and set it aside; it won't be used. Replace it with the new 78H05 regulator. Mount the regulator with a finned heatsink and thermal compound as above.
- () Replace the regulator mounting bracket in its original position, and secure it with the four hex spacers.
- () Replace the power supply board and secure it with its 4 screws.
- () Plug the cable connectors back onto the power supply board exactly as they were. WARNING: Be sure none of the power supply connectors are reversed or offset by a pin. This can cause serious damage.

- () Make sure your H/Z89 is turned off; then plug it in.
- () If you have a DC voltmeter, set it to measure +5 volts DC. Connect the negative lead to the regulator mounting bracket, and the positive lead to test point TP1 (see fig. 1-2).
- () Turn the H/Z89 "on". The voltmeter should read between +4.75 and +5.25 volts DC, and the H/Z89 should "beep" one or two times. If it does not, turn the machine "off".
- () If this is successful and you get the "H:", rerun the "DR.T" diagnostic tests. The test should run exactly as before. If the test fails, consult Chapter 2, "In Case of Trouble".

If you have a problem, recheck the heatsink upgrade installation. Be sure each of the regulators is in the correct position and that the connectors on the power supply board are all plugged in properly. If the problem can't be found, consult Chapter 2 "In Case Of Trouble".

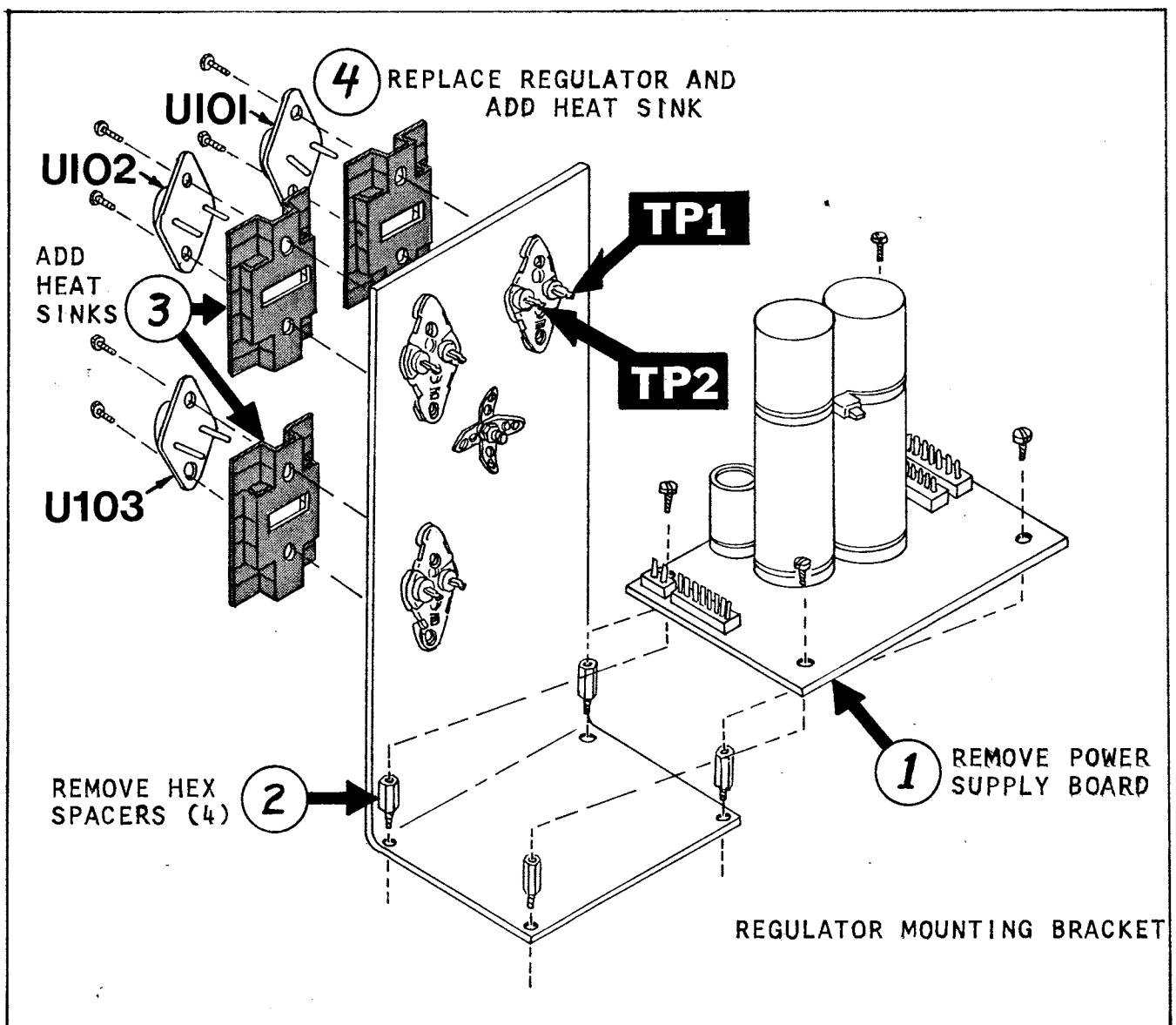


FIG. 1-2 HEAT SINK UPGRADE

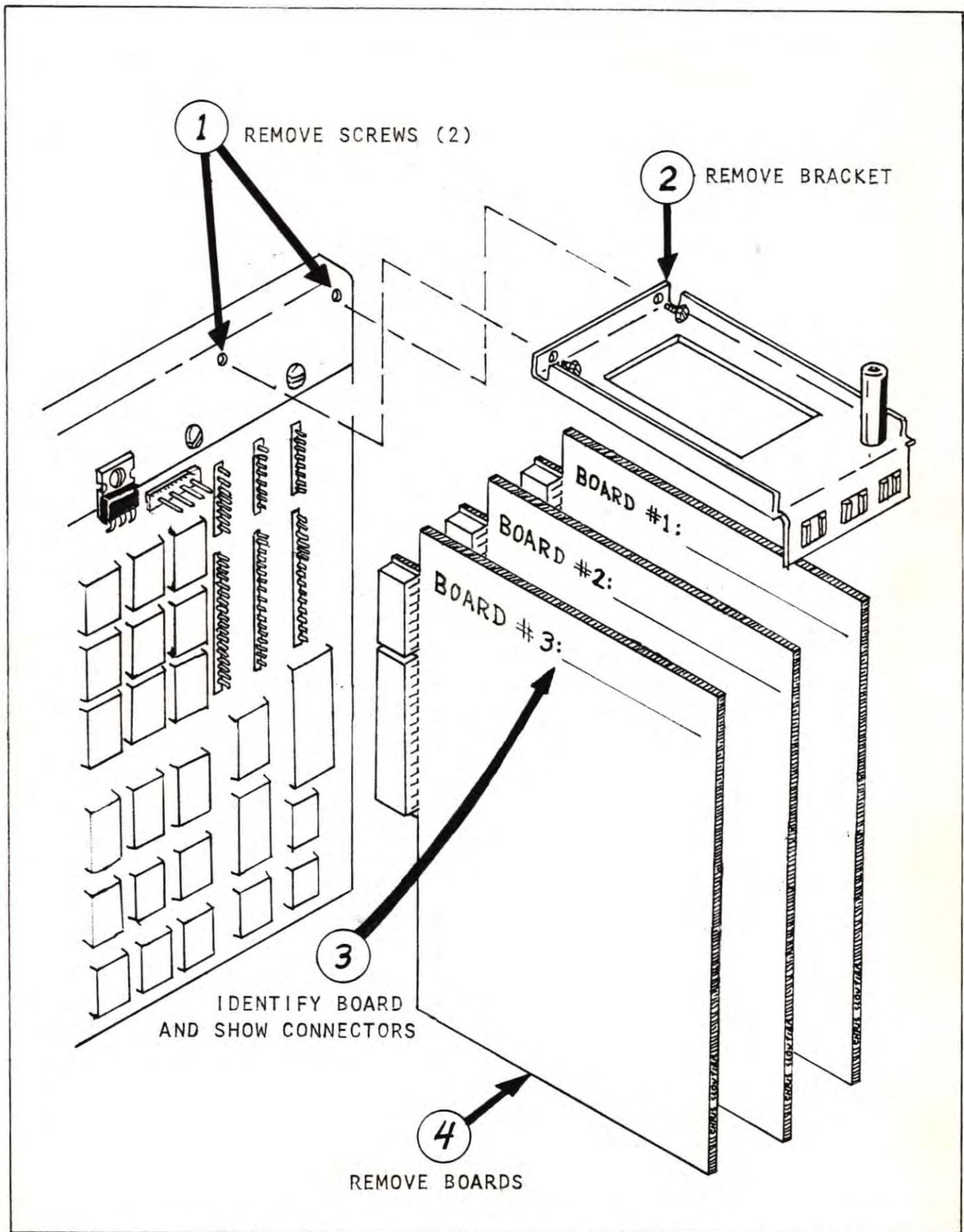


FIG. 1-3 ACCESSORY BOARDS

1.07 ACCESSORY BOARD REMOVAL

In the following steps you will unplug the I/O boards. It is not usually necessary to remove the boards completely from the machine; only that they be unplugged from the CPU board. Heath and Zenith boards present no special problems. If you have any other manufacturer's I/O boards installed, check the manuals that came with them for any special instructions on their removal or installation.

- () Turn the machine "off", and unplug it.
- () Remove the two screws holding the right-hand I/O board mounting bracket (see fig. 1-3). Be careful not to drop the screws inside the machine. Set the screws and bracket aside.
- () Use fig. 1-3 to sketch the accessory board in each I/O slot, and how its cable connections are made. In particular, note where each cable plugs in and the orientation of any colored wires or stripes ("blue stripe up" or "brown wire on top", etc.). Your sketch will be useful later to help re-install the boards correctly.
- () Unplug any board in I/O slot "3" (the leftmost slot). Be sure to record the cable connections in fig. 1-3.
- () Similarly, unplug any board in I/O slot 2 (center).
- () Likewise, unplug any board from I/O slot 1 (rightmost).
- () If any I/O boards have a separate cable connection to the CPU board (such as the Heath H37 soft-sector 5-1/4" disk controller), carefully unplug the cable from the I/O board end. Be sure to note its position and orientation on fig. 1-3.
- () If any of the I/O boards have a cable that runs over the top of the CPU board, unplug it or move it aside. Note its position in fig. 1-3.

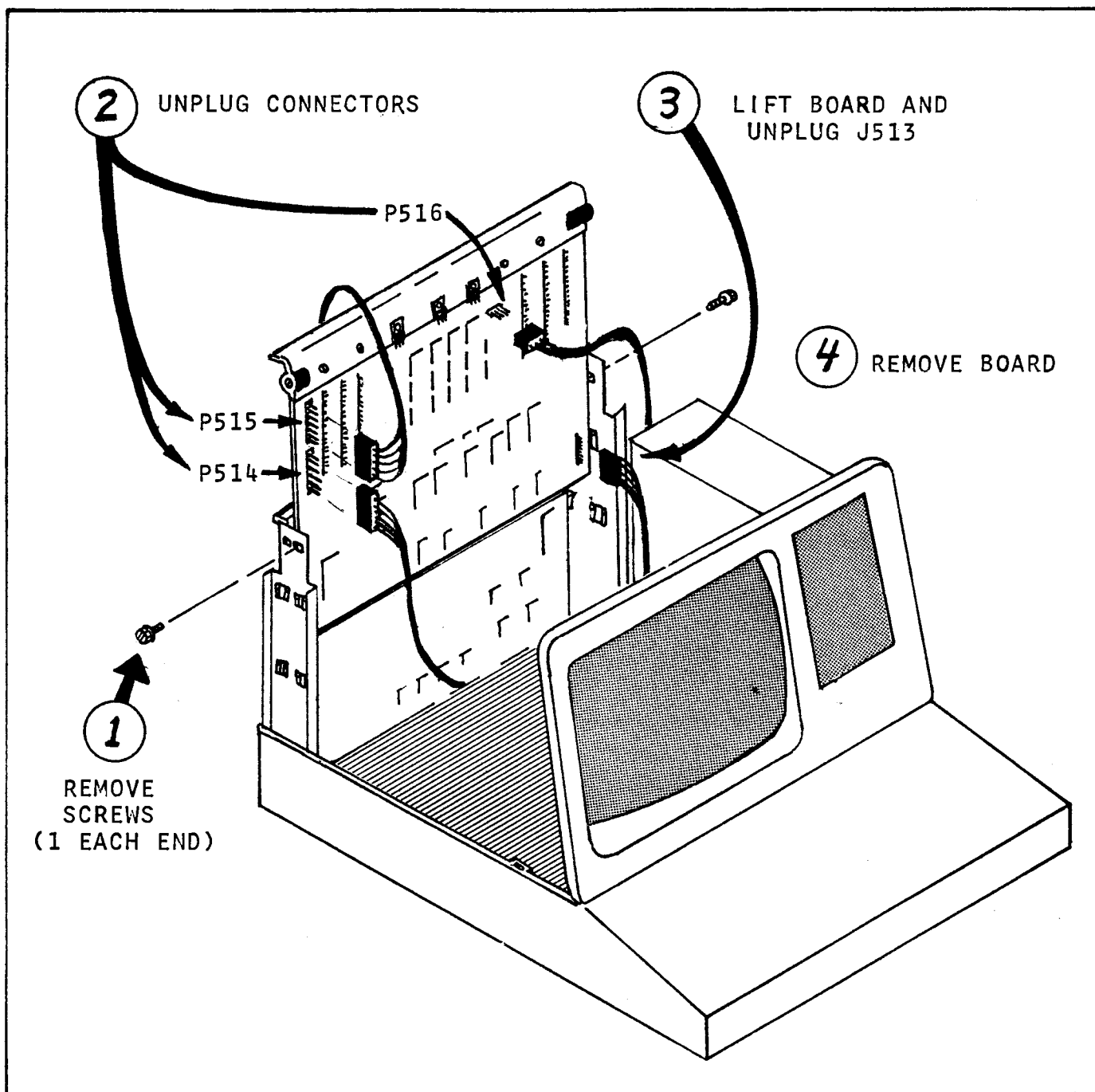


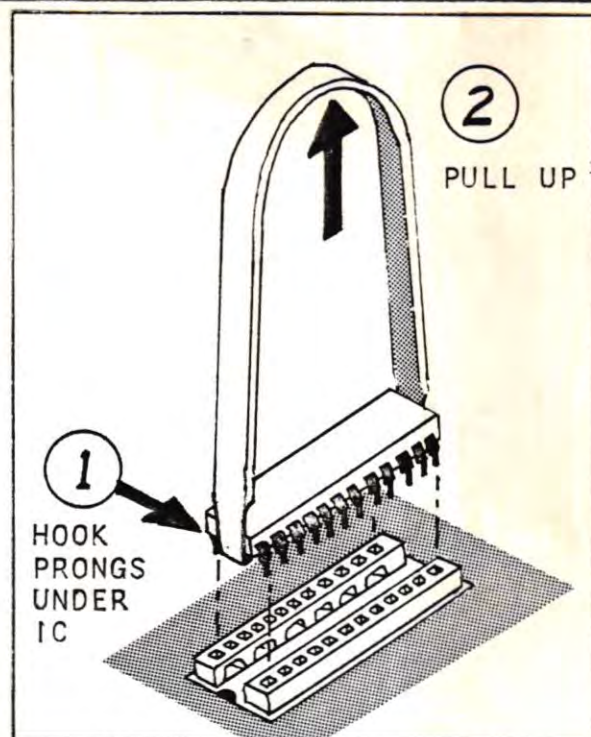
FIG. 1-4 CPU BOARD REMOVAL

1.08 REMOVING THE CPU BOARD

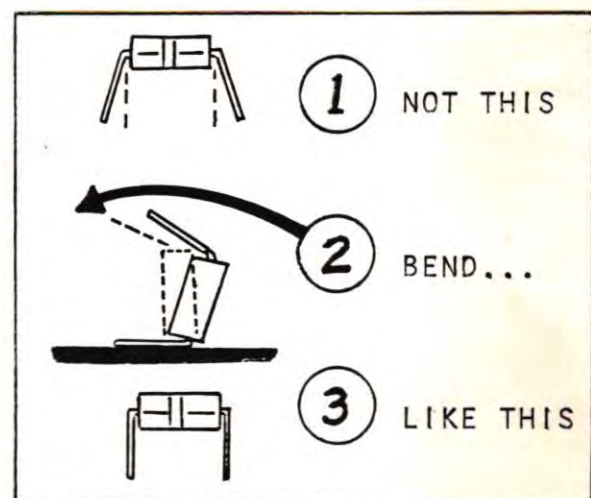
- () Remove the two screws holding the CPU board in place (fig. 1-4).
- () Disconnect the cable connectors from P514, P515 and P516.
- () Carefully slide the CPU board up in the card guides of the support brackets, until you can reach and disconnect the remaining cable connector at P513.
- () Remove the CPU board and set it aside on a flat work area.

Integrated circuits (ICs) are rugged and reliable components, but they can be easily damaged by static electricity or improper handling. Use the following procedures when installing or removing ICs:

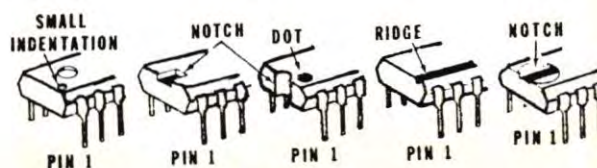
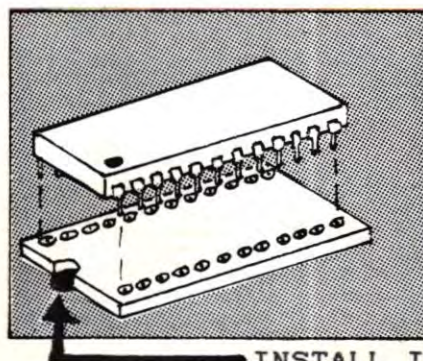
1. Remove the IC with the IC extraction tool provided. Hook the tool over the ends of the IC and pull straight up, rocking slightly from end to end.
2. Hold on to the IC until it is either replaced on a board or stored safely. ICs can be safely stored in special IC tubes, black conductive foam, or wrapped in aluminum foil.
3. Straighten any bent pins on the IC. The pins should be parallel to each other and at right angles to the case. Some ICs may have their pins spread out slightly (see illustration). If so, align the pins by gently pressing against a table top and bending as shown.
4. When installing the IC, align the notch and/or dot with the index mark on the board (see below). Be sure all the pins enter the holes of the socket, and then press the IC into its socket.



REMOVE THE IC



STRAIGHTEN THE LEADS



INSTALL IC WITH PIN 1 END AT INDEX MARK

FIG. 1-5 INTEGRATED CIRCUIT HANDLING

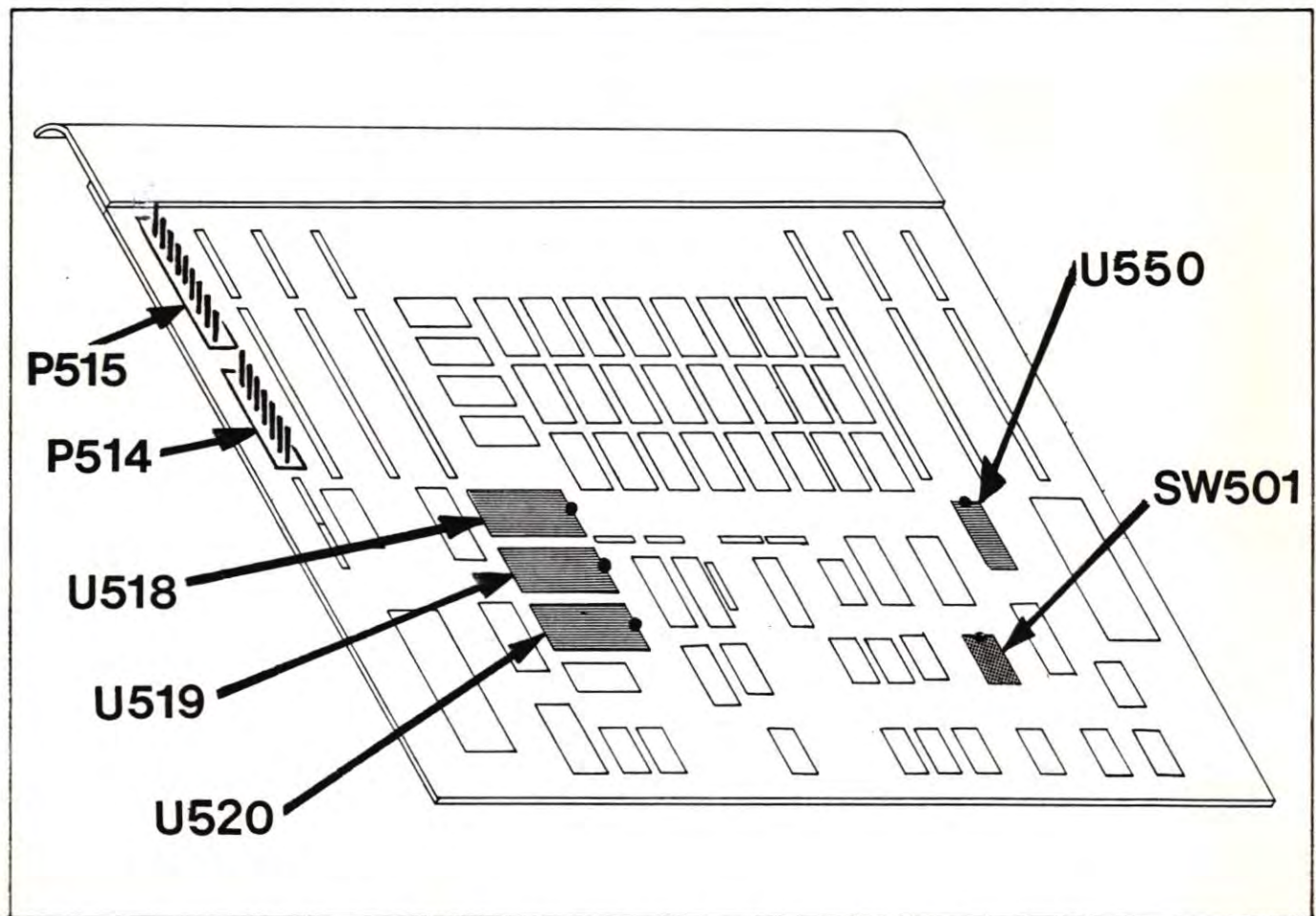


FIG. 1-6 H/Z89 BOARD ROM LOCATIONS

1.09 ROM EXCHANGE

H/Z89s use many different ROM ICs to support different disk controllers and other accessories. In the following steps, you will move ROMs U518, U519, U520, and U550 from your old CPU board to the H-1000. This insures that the H-1000 will be compatible with your present system. Observe the IC handling instructions in fig. 1-5.

- () Unpack the H-1000 board from its protective packaging.
- () Place the old CPU board and the H-1000 board side-by-side on a flat, clean surface, component side up.
- () Remove the ROM in socket U518 of the old CPU board (fig. 1-6).
- () Re-install the ROM in socket U518 on the H-1000 board (see fig. 1-7). Be sure pin 1 is in the correct location, and that all pins go into the holes in the socket.
- () If there is an IC in socket U519 of the old CPU board, remove it and install it on the H-1000 at U519. (Most H/Z89s will not have an IC in this socket.)
- () Remove the ROM in U520 of the old CPU board, and re-install it in socket U520 on the H-1000 board.
- () Remove the ROM in U550 of the old CPU board, and re-install it at U550 on the H-1000.

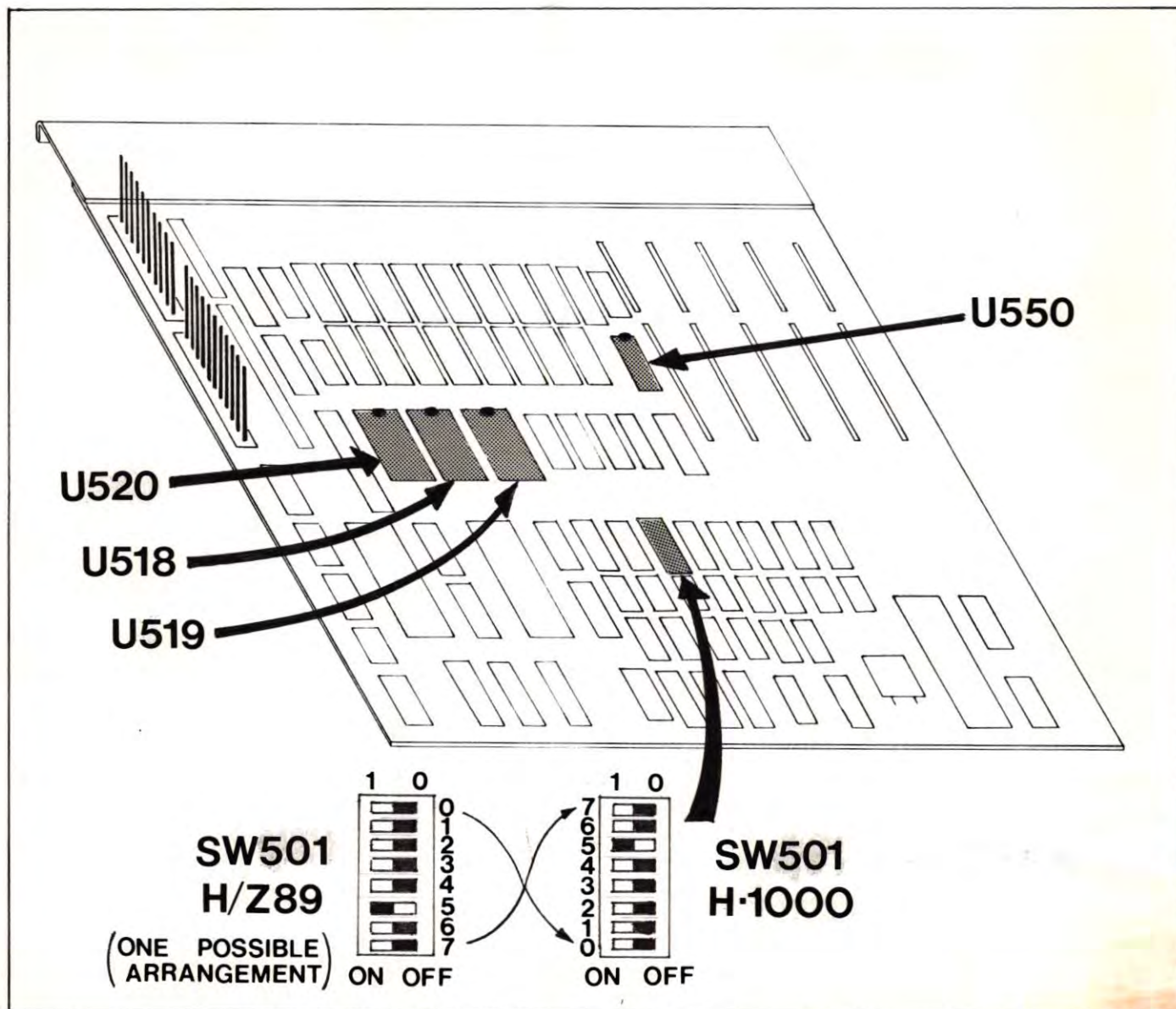


FIG. 1-7 H-1000 BOARD ROM LOCATIONS

1.10 DIP SWITCH SETTINGS

The DIP switch SW501 on the H-1000 is functionally identical to SW501 on the old CPU board; however, the switch positions (0-7) are reversed top-to-bottom on the H-1000 due to layout restrictions. Set the DIP switch positions on the H-1000 to match your old CPU board as follows (see fig. 1-7):

- () Set the bottom DIP switch position (#0) on the H-1000 to match the top DIP switch position (#0) on your old CPU board (i.e. if the old CPU board's switch #0 is positioned to the right, set the H-1000's switch #0 to the right).
- () Similarly, set switch #1 through #7 on the H-1000 to match the corresponding switches on the old CPU board.

1.11 DETERMINING YOUR H/Z89 MODEL

Heath/Zenith computers have used two different types of CPU boards. In order to install the H-1000 it is ESSENTIAL that you know which type of CPU board your machine has: The H-1000 will not work and may be seriously damaged if the wrong cable and jumper configuration is used.

- () Locate connector P515 in the upper left-hand corner of your old CPU board (see fig. 1-6).
- () Count the pins at P515, including any that have been cut or removed (a gap counts as a pin). Then do ONE of the following:
 - If P515 has 10 pins, then CONTINUE to SECTION 1.12 --
 - IF P515 has 11 pins, then GO to SECTION 1.14 --

1.12 JUMPER POSITIONS FOR OLDER H/Z89s

Use these instructions for older H/Z89s (with 10-pin connectors at P514 and P515). Jumpers JJ504-9 will be set in the following steps (fig. 1-8 and 1-9). "Jumpers" are small connectors that can be put in several positions to configure the board for various systems. When we tell you to set a jumper "the same" as your old board, set it to the SAME NUMBER OR LETTER even if the pin arrangement is different. To set a jumper, pull it off by hand and plug it back on in the correct position. Note the jumper numbers carefully -- they are NOT the same for the H89 and the H-1000.

- () On the old CPU board, there may be a resistor between pins 1 and 12 of P512 when no I/O board was installed in the first (rightmost) I/O slot. This resistor is not needed with the H-1000, and should not be moved.
- () Disregard any jumper wire on JJ503 of your old board; this wire isn't needed on the H-1000.
- () Ignore jumpers JJ501, JJ502, JJ503, and JJ504 on your old CPU board; they are not used on the H-1000.

- () Set JJ504 on the H-1000 to the same number ("1" or "0") as JJ505 on your old CPU board.
- () JJ505 on the H-1000 has three positions: "0", "1" or "2". To determine the correct position, look at JJ506 on your old CPU board. There are three possibilities:
 - () If JJ506 on your old CPU board is set at "1", set JJ505 on the H-1000 to "1".
 - () If JJ506 on your old CPU board is set at "0", set JJ505 on the H-1000 to "0".
 - () If JJ506 on your old CPU board has a jumper wire from its center pin to the memory expansion connector, then set jumper JJ505 on the H-1000 to "2".
- () Set JJ506 on the H-1000 to the same number ("1" or "0") as JJ507 on your old CPU board.
- () JJ507 on the H-1000 has three positions: "A", "B", and "C". To determine the correct position, look at JJ506 and JJ508 on your old CPU board. Then perform ONE of the following:
 - () If JJ506 on your old CPU board has a jumper wire from its center pin to the memory expansion connector, then set JJ507 on the H-1000 to "C".
 - () If there is no jumper wire on JJ506 of your old CPU board AND jumper JJ508 on your old board is in position "A", then set jumper JJ507 on the H-1000 to "A".
 - () If there is no jumper wire on JJ506 of your old CPU board AND jumper JJ508 on your old board is in position "B", then set jumper JJ507 on the H-1000 to "B".
- () Set JJ508 on the H-1000 to "C" if JJ507 on the H-1000 is set to "C"; otherwise, set JJ508 to "AB".
- () Set JJ509 on the H-1000 to the "1" position.

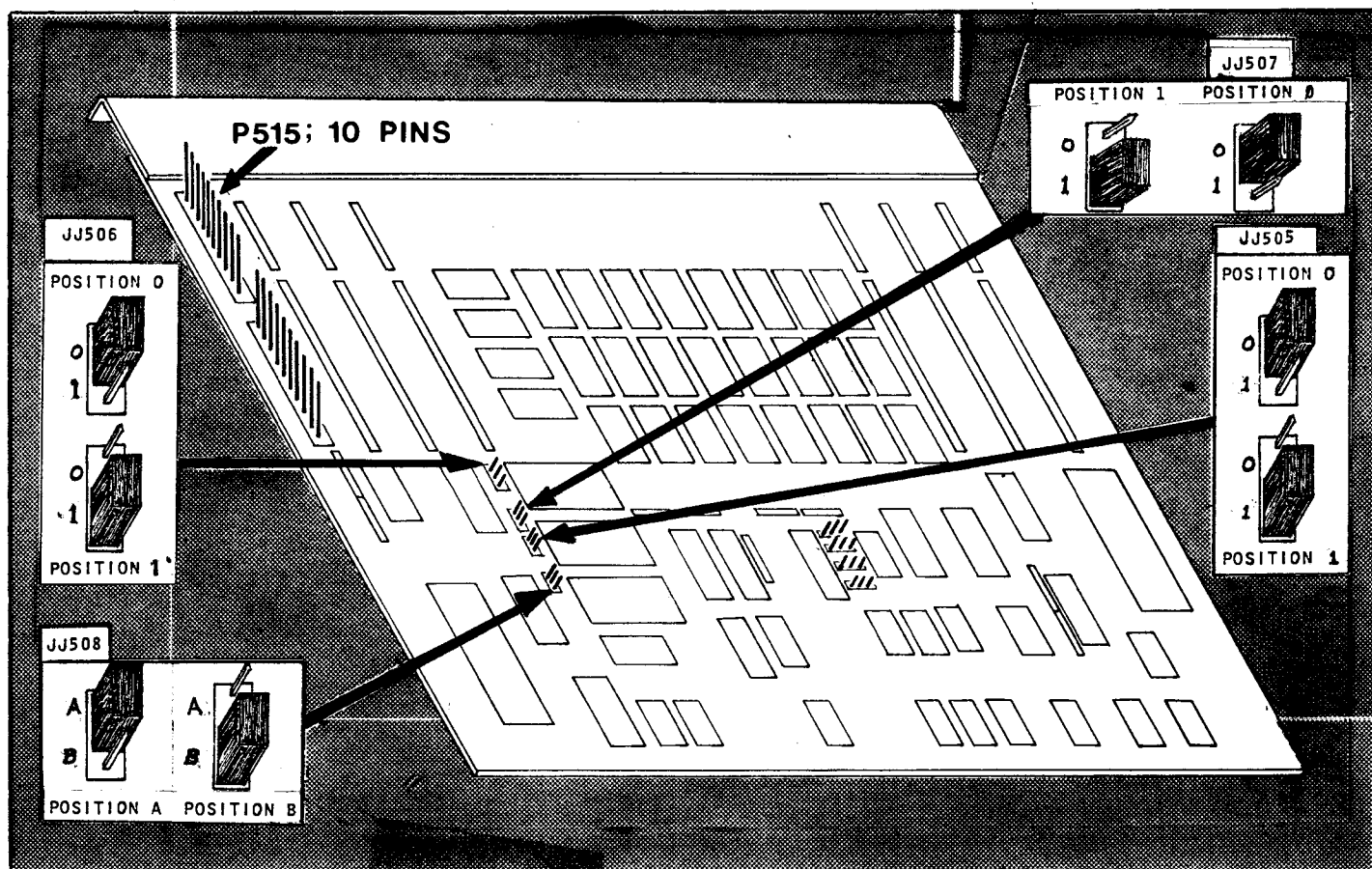


FIG. 1-8 OLDER H/Z89 JUMPER LOCATIONS

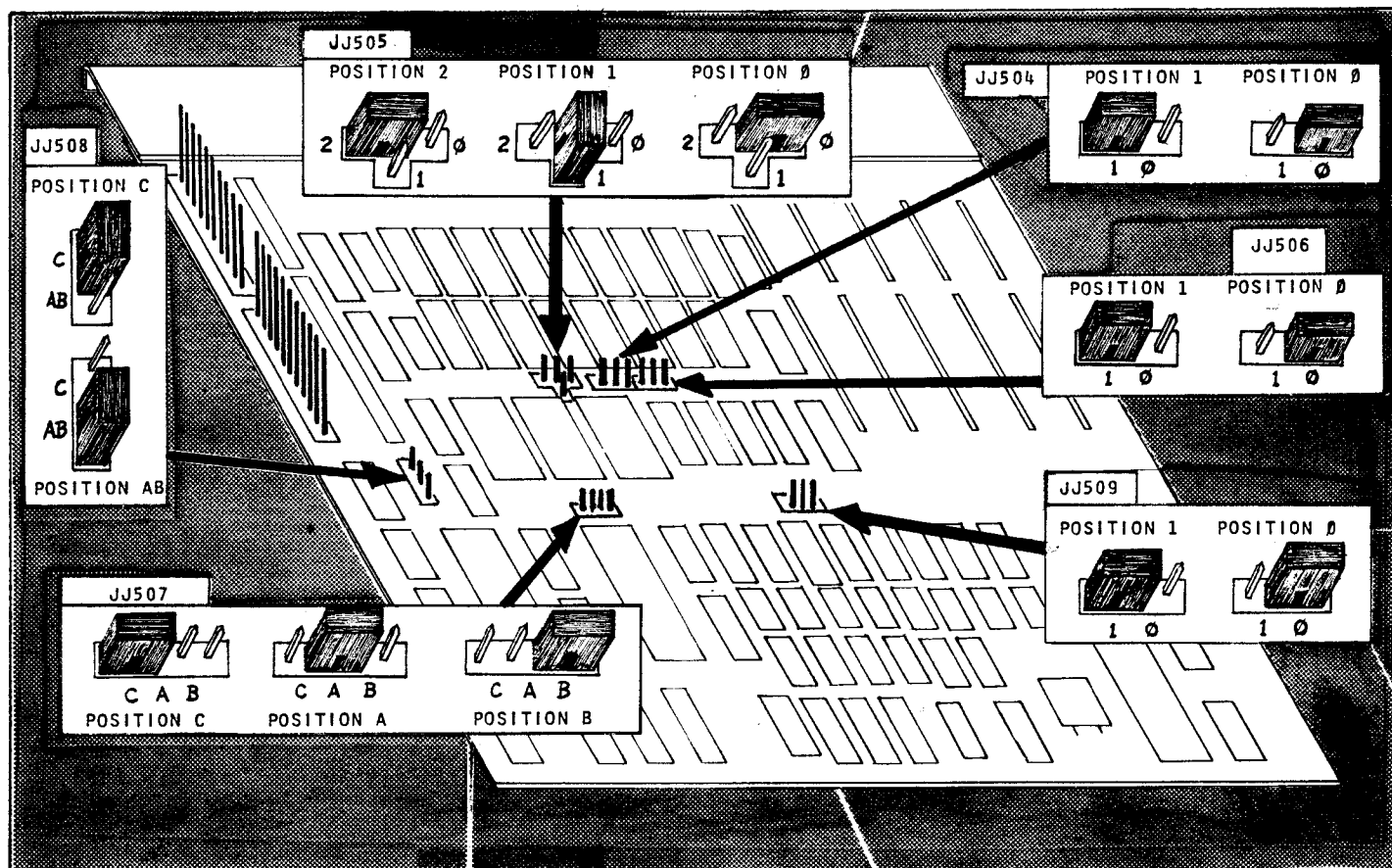


FIG. 1-9 H-1000 JUMPER LOCATIONS

1.13 INSTALLING THE H-1000 IN OLDER H/Z89s

CAUTION

In the following steps you will connect the power and terminal logic board connectors to the H-1000. Be careful not to plug in a cable backwards, or offset it by one or more pins. Doing so can cause serious damage to your machine! The H-1000's connectors have been "keyed" by removing certain pins to help prevent this, but your machine may not be keyed the same way. Beware if one of your connectors has a "key" that blocks a hole where the H-1000 has a pin. Recheck your work carefully, and only remove the key or cut a pin when you are SURE you are right.

- () Refer to fig. 1-10, and slide the H-1000 about halfway into the card guides. Locate connector J513 (at the end of the cable from the Terminal Logic Board), and plug it into P513 on the H-1000 (in the lower right-hand corner). Be sure that the slotted side of J513 faces toward the right.
- () Slide the H-1000 the rest of the way into the machine. Install a screw at each end to fasten it in place.
- () Plug the short 10-pin connector from the Terminal Logic Board (J515) into P515 on the H-1000. Push it all the way down so the long pins extend through the back. Be sure not to offset it by a pin, and that the slotted side faces toward the right.
- () Plug the 10-pin power supply connector (J514) onto P515 on the H-1000 board, on top of the connector already there (Don't use P514). The wire colors should match. Be sure not to offset it up or down by a pin, and that the slotted side faces toward the right.
- () Plug the 4-pin connector from the regulator mounting bracket into P516.
- () Plug the unit in and turn it on.
- () If the computer does not beep once or twice, turn it off and unplug it. Double-check the wiring of the connectors and check to see if all the cables are plugged in correctly. If you can find nothing wrong, consult Chapter 2, "In Case of Trouble".
- () If the computer "beeps" once or twice, wait for it to warm up. The "H:" prompt should appear. The monitor functions should all work normally (including memory tests), although of course it can't boot a disk without any I/O boards installed.

If no "H:" appears, turn the machine off and unplug it. Check the connector wiring and make sure all connectors are plugged in correctly. If nothing is found, consult Chapter 2 "In Case of Trouble".

-- NOW GO TO SECTION 1.16 --

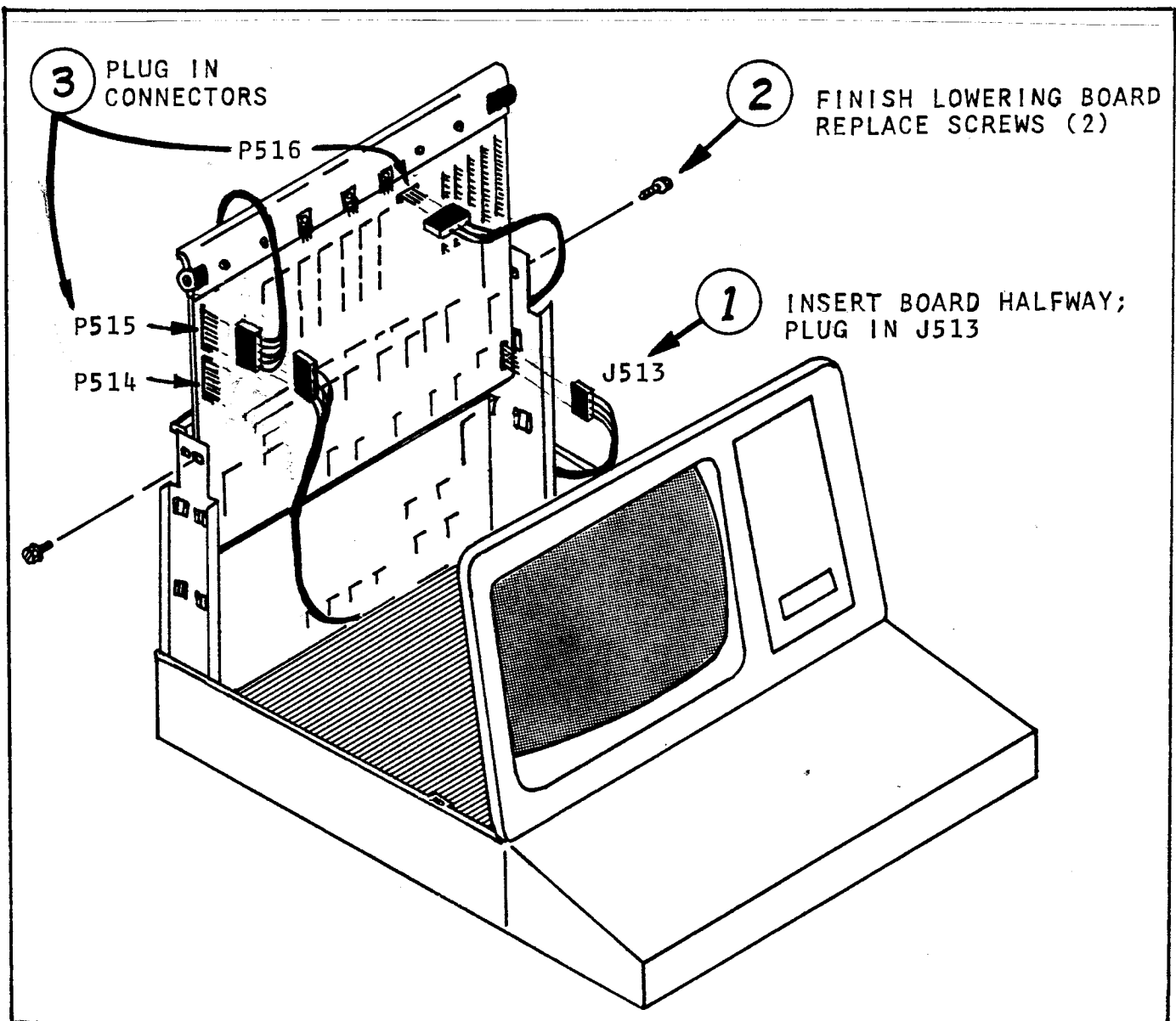


FIG. 1-10 INSTALLING THE H-1000 IN OLDER H/289s

1.14 JUMPER POSITIONS FOR NEWER H/289-Aa

Use these instructions for newer H/289-Aa (with 11-pin connectors at P514 and P515). Jumpers JJ504-9 will be set in the following steps (fig. 1-11 and 1-12). "Jumpers" are small connectors that can be put in several positions to configure the board for various systems. When we tell you to set a jumper "the same" as your old board, set it to the SAME NUMBER OR LETTER even if the pin arrangement is different. To set a jumper, pull it off by hand and plug it back on in the correct position.

The H-1000 has the same jumper designations as the newer H/Z89-A. But there are a few changes and additions, so read the following directions CAREFULLY.

- () Disregard the positions of jumpers JJ501, JJ502, and JJ503 on the old CPU board; they are not needed on the H-1000.
- () Set JJ504 on the H-1000 to the same number ("1" or "0") as JJ504 on your old CPU board.
- () JJ505 on the H-1000 has three positions: "0", "1" or "2". To determine the correct position, look at JJ505 on your old CPU board. There are three possibilities:
 - () If JJ505 on your old CPU board is set to "1", set JJ505 on the H-1000 to "1".
 - () If JJ505 on your old CPU board is set to "0", set JJ505 on the H-1000 to "0".
 - () If JJ505 on your old CPU board has a jumper wire from its center pin to the memory expansion connector, then set JJ505 on the H-1000 to "2".
- () Set JJ506 on the H-1000 to the same number ("1" or "0") as JJ506 on your old CPU board.
- () JJ507 on the H-1000 has three positions: "A", "B", and "C" (see fig. 1-12). To determine the correct position, look at JJ505 and JJ507 on your old CPU board. Then do ONE of the following:
 - () If JJ505 on your old CPU board has a jumper wire from its center pin to the memory expansion bus, then set JJ507 on the H-1000 to "C".
 - () If there is no jumper wire on JJ505 of your old CPU board AND JJ507 on your old CPU board is set to "A", then set JJ507 on the H-1000 to "A".
 - () If there is no jumper wire on JJ505 of your old CPU board AND JJ507 on your old CPU board is set to "B", then set JJ507 on the H-1000 to "B".
- () Set JJ508 on the H-1000 to "C" if JJ507 on the H-1000 is set to "C"; otherwise, set JJ508 to "AB".
- () Set JJ509 on the H-1000 to the "1" position.
- () On your old CPU board, there may be a resistor between pins 1 and 12 of P512 if no I/O board was installed in the first (rightmost) I/O slot. This resistor is not needed on the H-1000, and should not be used.

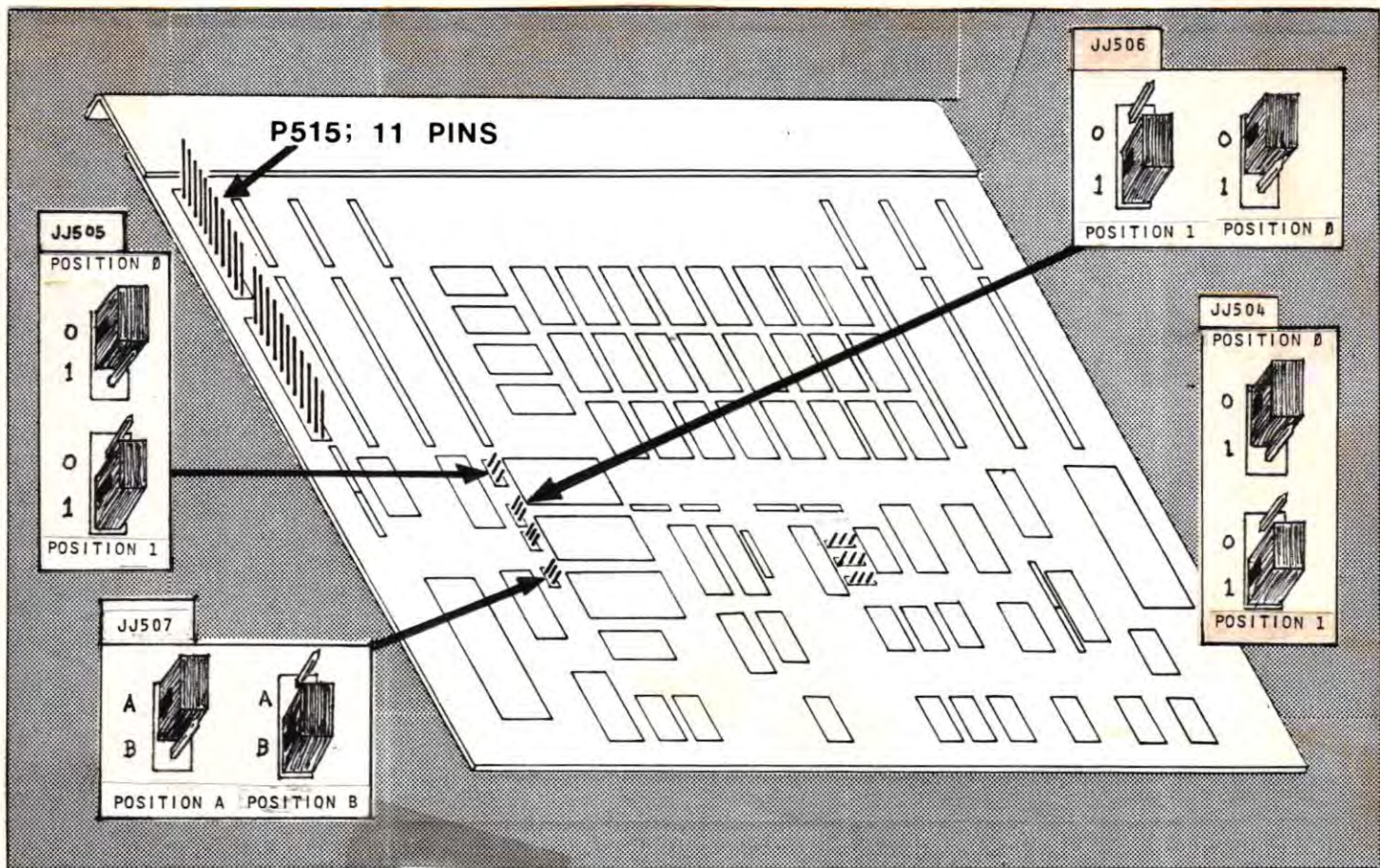


FIG. 1-11 NEWER H/Z89 JUMPER LOCATIONS

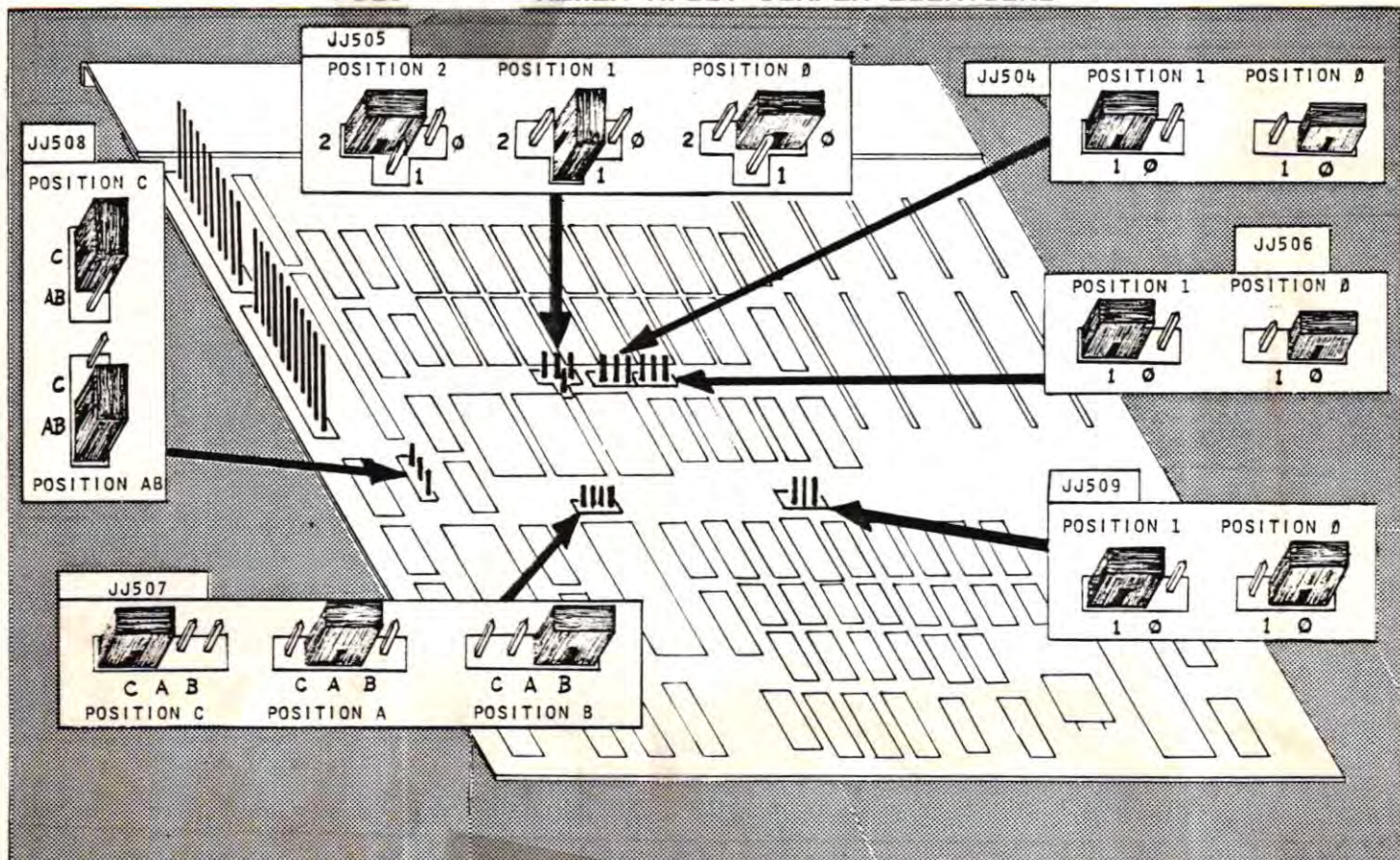


FIG. 1-12 H-1000 JUMPER LOCATIONS

1.15 INSTALLING THE H-1000 IN NEWER H/289-As

CAUTION

In the following steps you will connect the power and terminal logic board connectors to the H-1000. Be careful not to plug in a cable backwards, or offset it by one or more pins. Doing so can cause serious damage to your machine! The H-1000's connectors have been "keyed" by removing certain pins to help prevent this, but your machine may not be keyed the same way. Beware if one of your connectors has a "key" that blocks a hole where the H-1000 has a pin. Recheck your work carefully, and only remove the key or cut a pin when you are SURE you are right.

In the following steps you will replace the short "jumper" cable on J401 of the Terminal Logic Board with a new longer cable (supplied with the H-1000). The new cable is exactly like the original one, only longer.

- () Unplug the short "jumper" cable from connector J401 in the upper left corner of the Terminal Logic Board. There are two possibilities:
 - If the old cable is still attached to the computer by a shielded wire in pin 11, remove this wire from the connector as shown in fig. 1-13. The old cable is now free of the machine; set it aside. Remove the yellow wire from pin 11 of both ends of the new cable. Plug the shielded wire into pin 11 of one end of the new cable. The new cable should now be exactly like the original one, only longer.
 - If the old cable is free of the machine as soon as it is unplugged from J401, the new cable can be used without change.
- () Plug the new longer cable onto J401 of the Terminal Logic Board. The end with the shielded wire (if present) should be on J401 as it was originally.
- () Refer to fig. 1-14, and slide the H-1000 about halfway into the card guides. Locate connector J513 (at the end of the cable from the Terminal Logic Board), and plug it into P513 on the H-1000 (in the lower right-hand corner). Be sure that the slotted side of J513 faces toward the right.
- () Slide the H-1000 the rest of the way into the machine. Install a screw at each end to fasten it in place.
- () Plug the 11-pin "jumper" cable from the Terminal Logic Board (J515) onto P514 on the H-1000 (don't use P515). Push it all the way down so the long pins extend out through the back. Be sure it is not offset by a pin, and that the slotted side faces toward the left.

- () Plug the 11-pin power supply connector (J514) onto P514 on the H-1000 board, on top of the connector already there. The wire colors should match. Be sure not to offset it up or down by a pin, and that the slotted side faces toward the left.
- () Plug the 4-pin connector from the regulator mounting bracket into P516.
- () Plug the unit in and turn it on.
- () If the computer does not beep once or twice, turn it off and unplug it. Double-check the wiring of the connectors and check to see if all the cables are plugged in correctly. If you can find nothing wrong, consult Chapter 2, "In Case of Trouble".

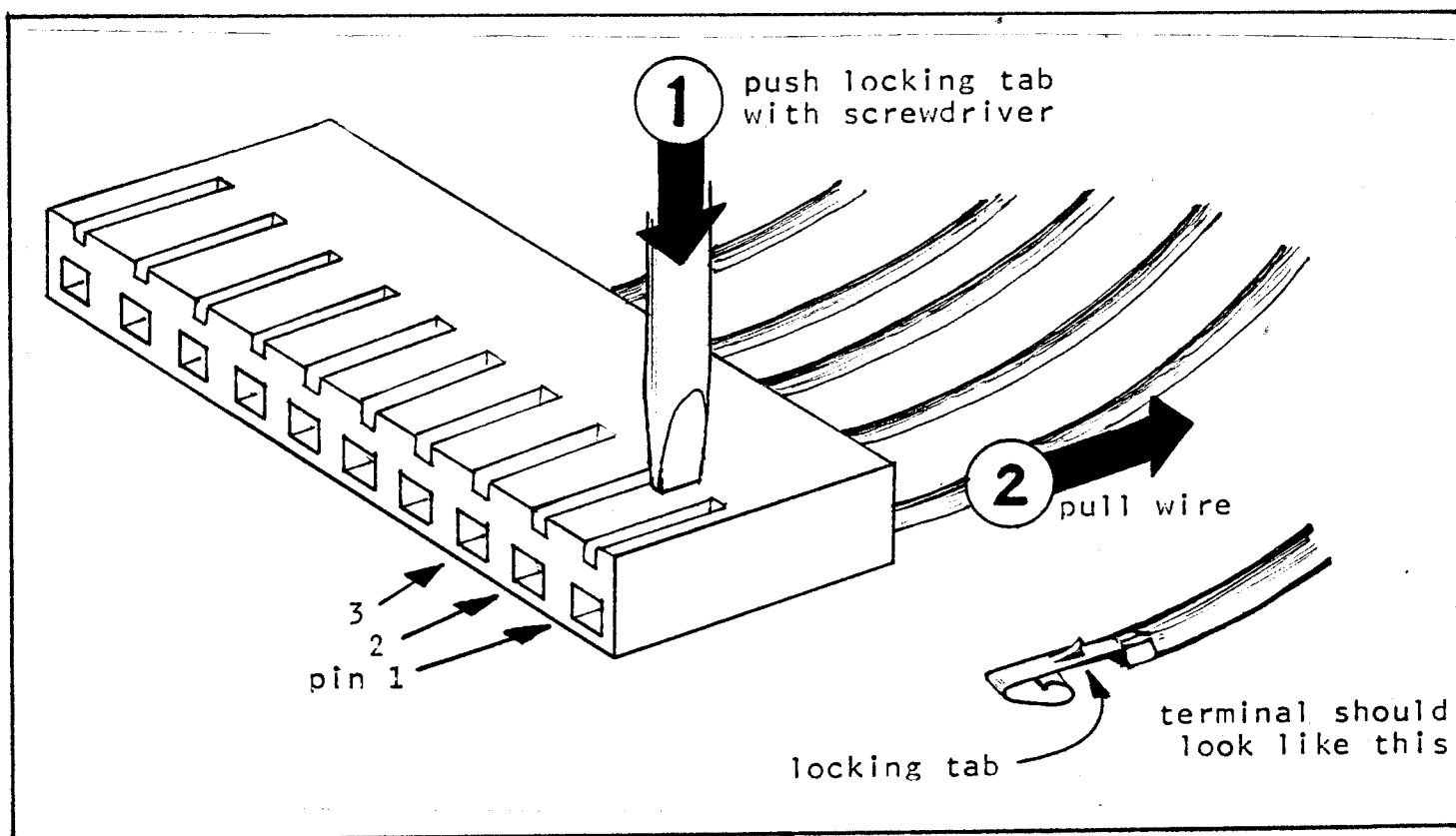


FIG. 1-13 REMOVING A WIRE FROM J401

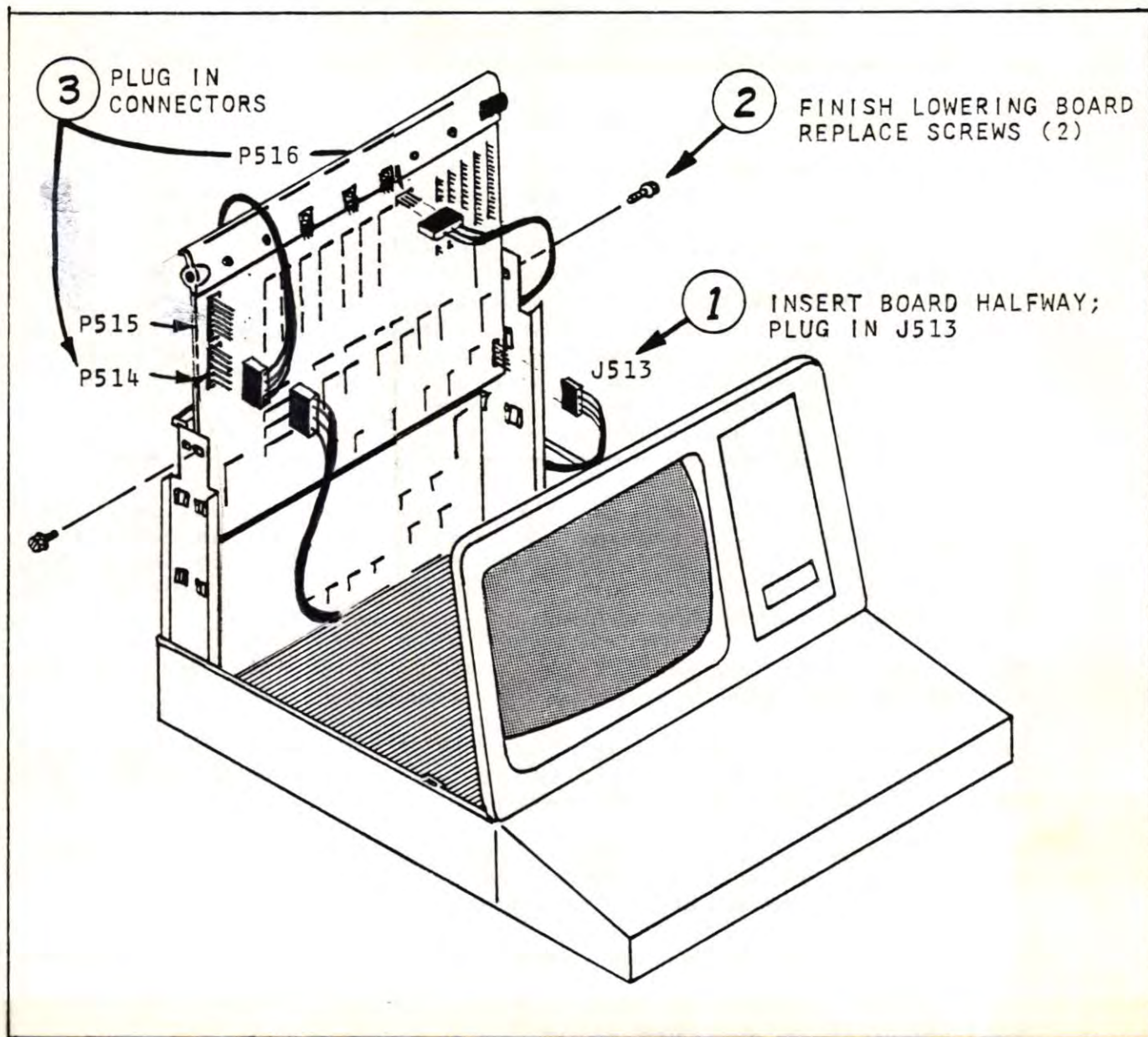


FIG. 1-14 INSTALLING THE H-1000 IN NEWER H/Z89-Aa

1.16 INSTALLING ACCESSORY BOARDS

The H-1000 has five accessory slots instead of the three provided on the H/Z89. The three rightmost I/O slots (1 thru 3) on the H-1000 are identical to the three slots on the H/Z89; all Heath/Zenith (and most other) I/O boards are installed in these slot exactly the same as for an H/Z89.

The two new I/O slots (4 and 5) are identical to slots 2 and 3, except that they are assigned to new I/O addresses. We recommend that you do not use them until you have installed your original I/O boards and have them working normally. See Chapter 3, "How to Program the H-1000" for more details.

- () Heath Z-89-37 Soft-Sector Disk Controller Board: Perform the following steps ONLY if you will be using this board on the H-1000:
 - () Remove ICs U557 and U558 from the H-1000 board with the IC extraction tool.
 - () Remove the jumper plug from U558 on your old CPU board, and install it in socket U558 on the H-1000 board.
 - () Refer to your notes on fig. 1-3, and re-install the I/O board removed from slot one (right-most). Also re-connect any cables that were disconnected from it earlier. Be very careful it is not installed either 1 pin too high or low, or considerable damage can result.
- NOTE: The H-1000 positions the right-most I/O board closer to the internal disk drive than an H/Z89. There may be a flat ribbon cable with a black sleeve running through this area. If the sleeve makes the cable too thick, you may have to remove the sleeve or re-position the cable to fit.
- () Similarly, re-install any board that may have been in slot 2.
 - () Re-install any board that may have been in slot 3.
 - () Heath Soft-Sector Disk Controller board (Z-89-37): If you have this board, plug the jumper cable from it (that used to connect to U557 on your old CPU board) into IC socket U557 on the H-1000 board.
 - () Install the new I/O board mounting bracket, using the two screws from the original bracket. Be sure to place the I/O boards in the card guides before tightening the screws.
 - () Replace the cover and reconnect the fan.
 - () Plug the machine in and turn it "on".
 - () The machine should beep once or twice and the "H:" prompt should appear. If this does not happen turn the machine "off" and unplug it. Check the installation of the accessory boards and their cables. If nothing can be found, go to Chapter 2, "In Case of Trouble".
 - () Run the "DR.T" diagnostic tests again, and follow the directions for testing an H-1000.
 - () If you have any problem with the tests, proceed to Chapter 2, "In Case of Trouble".

**This completes Installation
of the H-1000!**

CHAPTER 2

IN CASE OF TROUBLE

This chapter is divided into two sections. The first is on general troubleshooting, which covers problems in the installation. The second section is a flow chart to help you find defective parts from the problems they cause.

2.01 GENERAL TROUBLESHOOTING

1. GENERAL

Don't do too many things at once (i.e. install new I/O boards at the same time as the H-1000). Wait until the H-1000 is installed and working correctly before adding other accessories.

Have a friend check your installation. Someone who has not seen it before may notice something you have overlooked.

2. NON-STANDARD ACCESSORIES

If you have any non - Heath/Zenith accessories in your machine, they should be removed before installing the H-1000 unless you are sure they are compatible with it. If you aren't sure, call us at TMSI first.

3. H/Z89 PROBLEMS

If your H/Z89 doesn't pass the DR.T diagnostics, check for the following conditions. The DR.T rev. 1.0 requires:

- 64K of RAM memory.
- Heath/Zenith H17 5-1/4" hard-sector disk drive and controller.
- Standard Terminal Logic Board configuration (9600 baud, etc).
- Standard 2 MHz CPU clock.

Certain non - Heath/Zenith accessories will also prevent one or more tests from running successfully. For example, the Magnolia disk controller causes the 2 mSec. clock test to fail.

4. HEAT SINK UPGRADE

Check to see that the correct regulators are installed in U101, U102, and U103. Be sure the regulator's pins do not touch the regulator mounting bracket (the regulator sockets have a ridge around the edges of their holes to help prevent this). Check that the four connectors to the power supply board are plugged in correctly.

Heavily loaded H/Z89's tend to overheat the center pins of connector P101 (the rear-most connector on the power supply board). The symptoms of this problem are discoloration around the yellow wires on P101, and/or a dark horizontal band on the screen that moves slowly upward. Heath's solution to this problem is to remove the yellow wires from P101, and solder them directly to bridge rectifier BR1, on the regulator mounting bracket. Ask your Heath or Zenith service center for details.

5. H-1000 INSTALLATION

If the computer doesn't "beep" once or twice with the H-1000 installed, go back over the installation instructions and check your work. Be particularly watchful for the following:

- Connectors plugged in backwards, or offset by one or more pins.
- ROM ICs installed wrong (see below).
- Connectors that were accidentally unplugged or knocked loose.
- Accidentally changing the switches on the Terminal Logic Board.

Check the ROMs you installed on the H-1000. Make sure they are in the correct sockets, and have pin 1 at the correct end (see fig. 1-10 or 1-13). The following ROMs are acceptable. If you have a non - Heath/Zenith disk controller board, some of these ROMs may be different.

H-1000 socket	Acceptable part numbers
U518	Heath# 444-40, 444-62, 444-84 (obsolete), 444-142 CDR# 90L1
U519	(empty in all Heath systems)
U520	Heath# 444-19
U550	Heath# 444-43, 444-61 CDR# CDR86

6. ACCESSORY BOARD INSTALLATION

If plugging in the Accessory boards causes the "H:" to go away, check for an accessory board installed in the wrong socket, or offset up or down by a pin. Also be sure the cables to the accessory board are installed exactly as you removed them (see fig. 1-3).

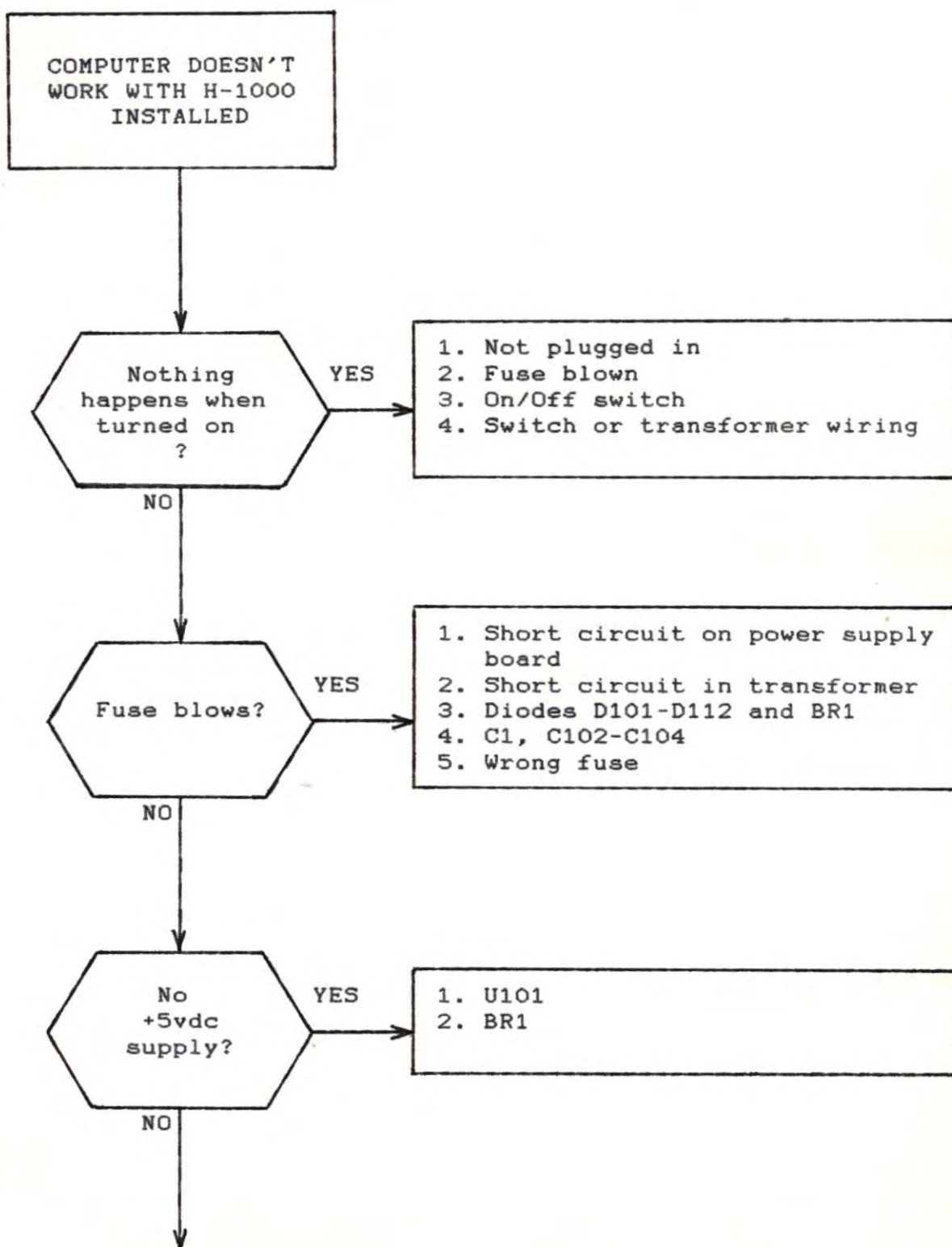
7. IT WORKS, BUT...

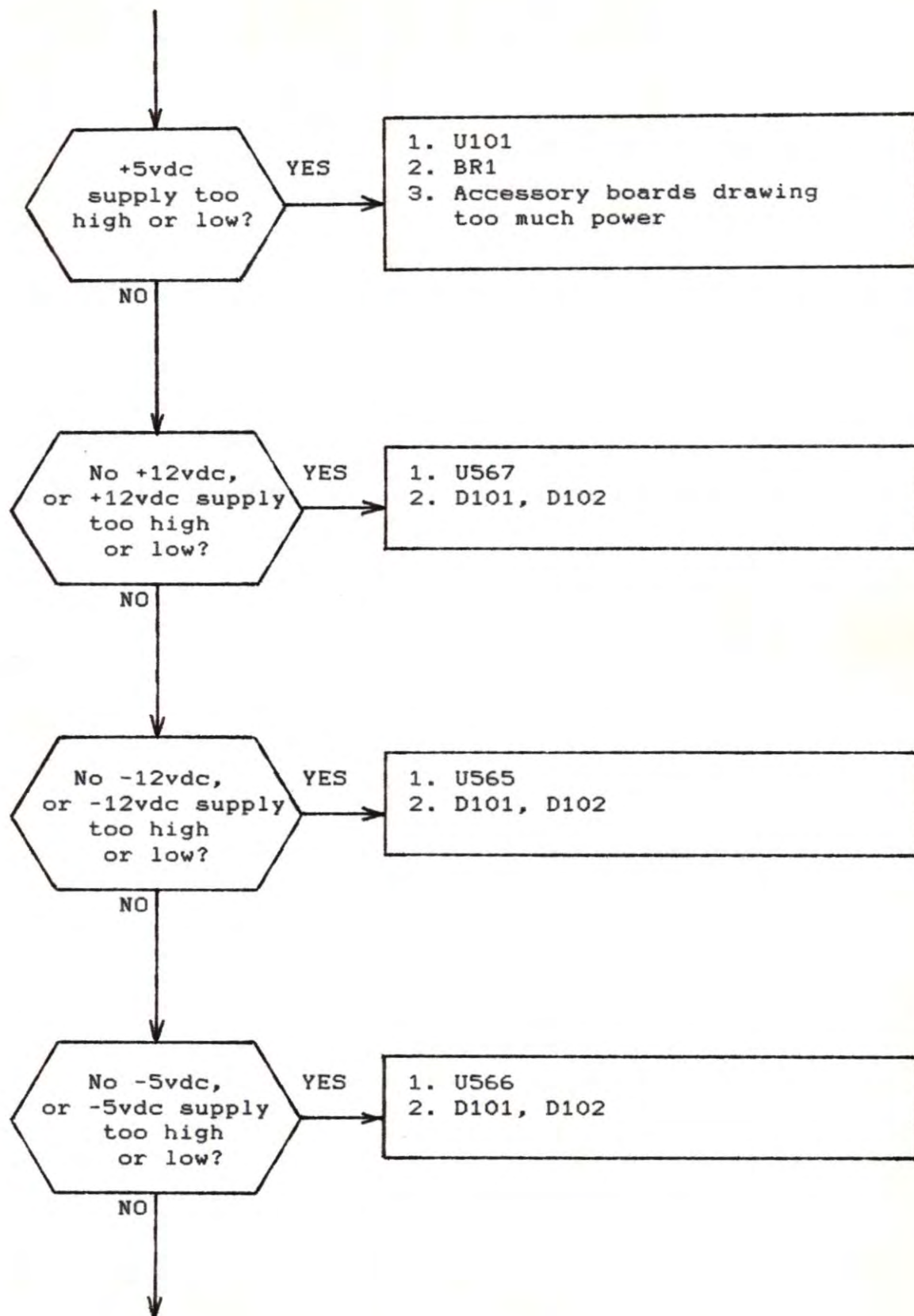
If you have turned on the machine with a regulator or power connector installed wrong, check bridge rectifier BR1 (located on the regulator mounting bracket). It is possible for 1 or more of the diodes in it to fail, and yet the machine still seems to work. Symptoms of this problem are random program "crashes" and generally unreliable operation. You will need a Volt-Ohm Meter to make the following tests. Perform the tests with the machine fully warmed up.

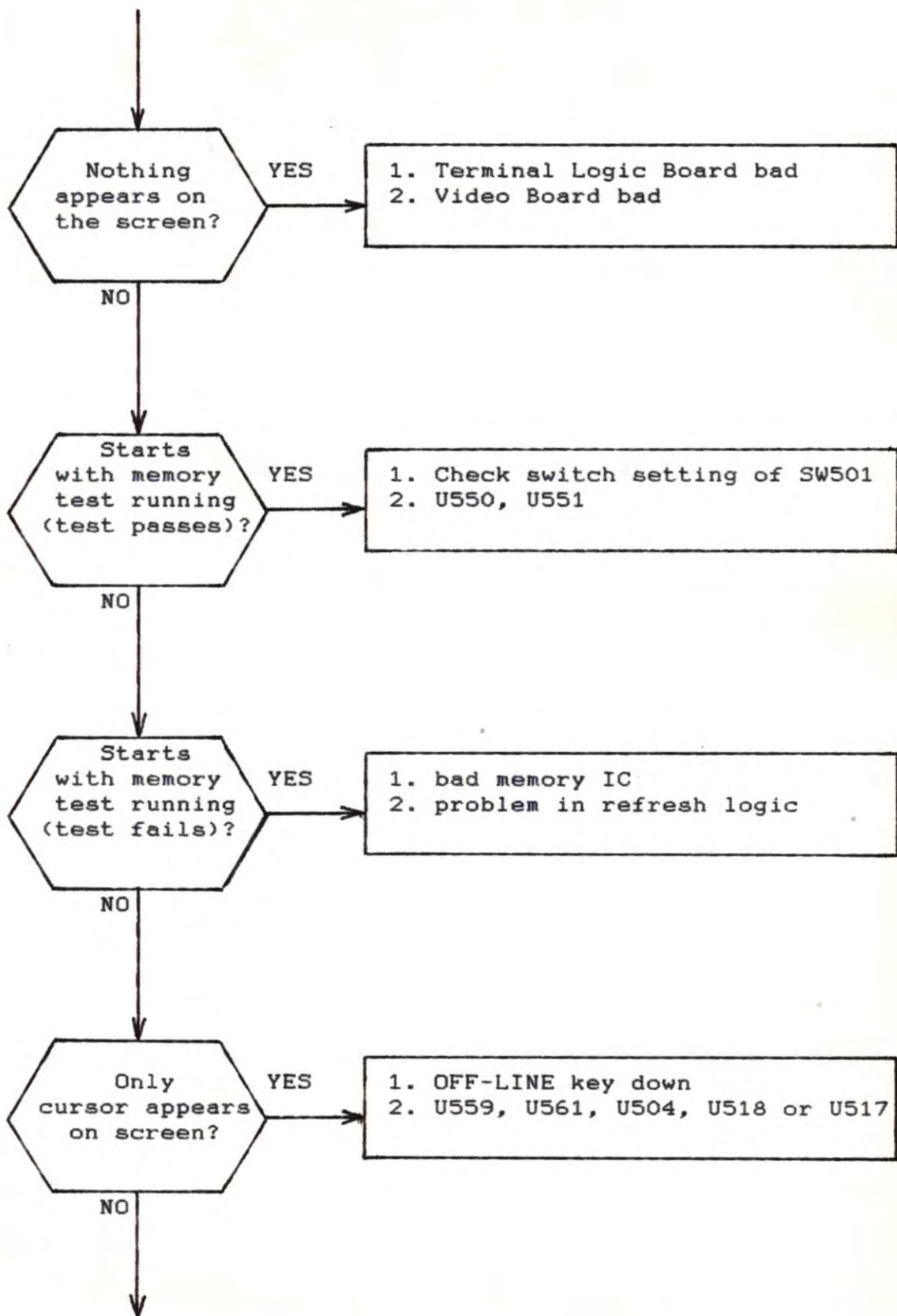
- Turn the machine on, and measure the AC voltage between TP1 and ground (see fig. 1-2 on page 1-5). This is the amount of ripple on the +5 VDC supply, and should measure less than 10 mVAC.
- Measure the voltage between TP2 and ground (fig. 1-2). It should be between 8.2 and 9.5 VDC.

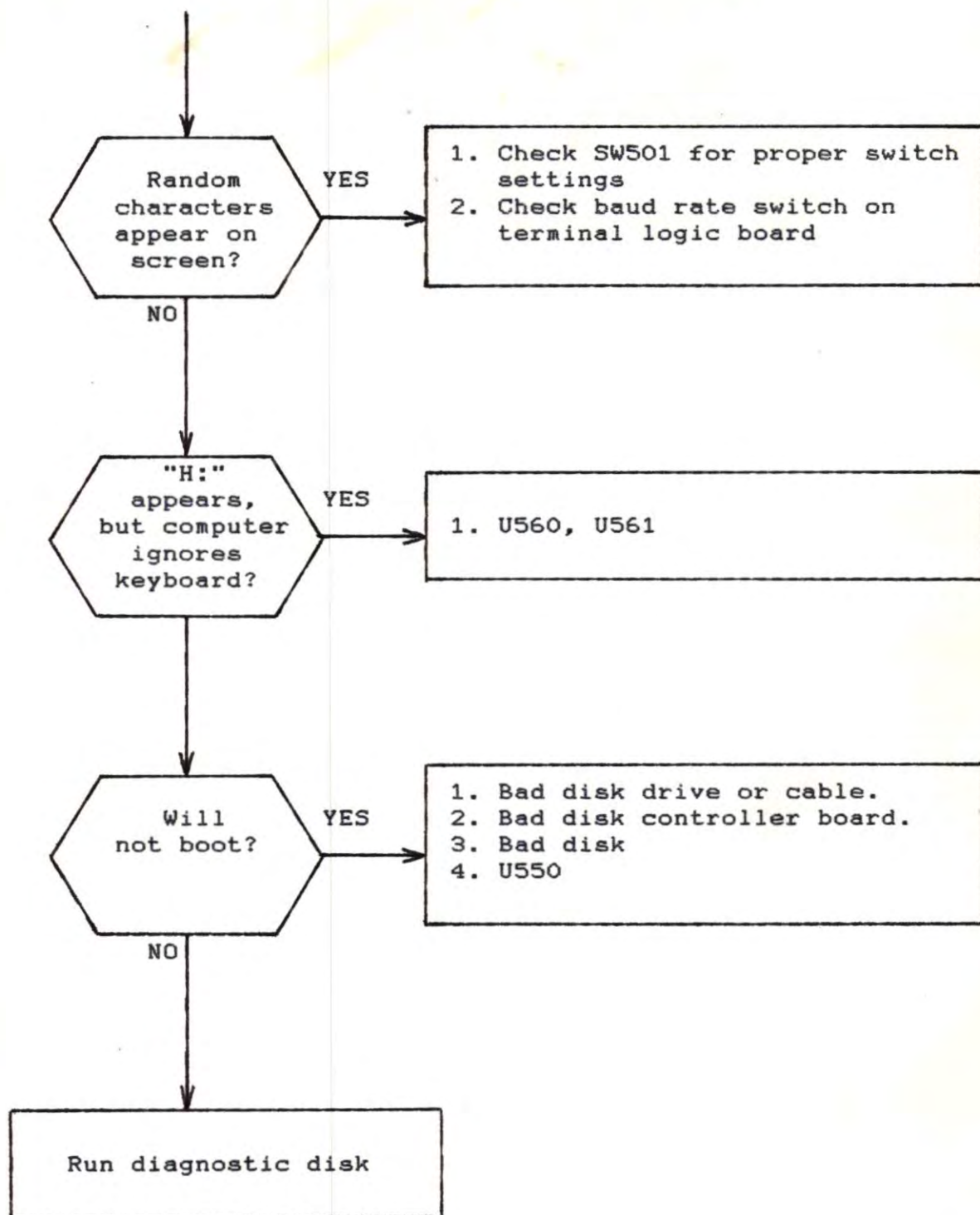
If both of the above tests fail, then BR1 is probably defective.

2.02 TROUBLE FLOWCHARTS









2.03 Last Resort

If none of these steps corrects the problem, TMSI Technical Consultation can be reached at (313) 994-0784. This number is good for consultation on all TMSI hardware or software. Should you need to return your H-1000 for warranty or repair, call TMSI and get a Returned Materials Authorization (RMA) number and shipping instructions. This number must be on the box or we can't accept it. Repair parts are also available through TMSI.

CHAPTER 3

HOW TO PROGRAM THE H-1000

3.00 INTRODUCTION

Many H-1000 users will spend most of their time running high-level languages or using software that was purchased complete and running. However, you may also be doing assembly language programming, or find some applications that require direct access to resources at the machine-language level. In this chapter we will discuss the hardware features of the H-1000 from the programmer's point of view, and how to use them. We will begin with a review of the standard H/Z89's CPU board features, and how the H-1000 differs from it. We'll then discuss each feature in detail (memory, I/O, etc.).

3.01 H/Z89 CPU BOARD REVIEW

The original CPU board of the H/Z89 includes a Z80 microprocessor running at 2 MHz; up to 48K bytes of dynamic RAM, up to 6K bytes of ROM/EPROM, and 1k bytes of static RAM. The static RAM can be write protected. There are six expansion connectors; three for additional memory boards, and three for I/O boards. The memory board connectors provide for 8K of memory each, but can also be used with a 16K expansion board for a total maximum of 64K of RAM. Two of the three I/O connectors are normally occupied by a disk drive controller and a 3-port serial I/O board, leaving one free for a second disk controller or other use. The board has an 8-level priority interrupt controller, and uses the 8080 mode of interrupt handling. A 2 mS real-time clock interrupt is provided. There is also a single-step circuit to generate an interrupt after each instruction, useful for machine-level debugging and a holdover for compatibility with the earlier Heath H8 computer.

Physically, the H/Z89 board measures 9-3/4 x 11". It requires a total of 8.6 watts: +5vdc at 1 amp (regulated), +18vdc at 150mA, and -18vdc at 50mA. On-board regulators provide +12, -12, and -5vdc, and are mounted to a metal heatsink along the top edge of the board. The memory and I/O expansion boards plug into the CPU board at right angles via connectors with 0.025" square posts.

3.02 DESCRIPTION OF THE H-1000

The H-1000 is a high-performance replacement for the H/Z89's existing CPU board. It is physically and functionally interchangeable in all respects to the present board, but adds a 4 MHz clock for the Z80; additional RAM (up to 1 megabyte); and a second CPU, the 16-bit 8086. The H-1000 is of particular interest to users who would benefit from greater speed and more memory for their H/Z89 applications, or who are seeking better performance than the IBM PC or Zenith Z100 series at a lower cost.

The Z80 portion of the H-1000 follows the design of the original board as closely as possible, and is fully compatible with all H/Z89 hardware and software. The 2 mSec real-time clock, single-step logic, memory page select, and write-protected 1K RAM block are all retained. The Z80's clock speed is software selectable, to run software that depends on a 2 MHz clock. The existing I/O port assignments are unchanged, except for a new general-purpose port to control CPU selection (Z80 or 8086), Z80 clock speed, and the additional address lines for the 1 megabyte address space.

The H-1000's 8086 CPU uses the same address, data, and control busses as the Z80, so both CPUs share the same memory and I/O maps. A true 16-bit data bus is used for maximum performance. Only one CPU runs at a time; the other one is halted and remains ready to resume execution where it left off when a CPU swap occurs. The H-1000 uses either 64K or 256K dynamic RAMs, and can be configured for 128K, 256K, 512K or 1 megabyte on-board. During Z80 operation, refresh is performed by the Z80's normal automatic memory refresh, but with an external refresh address counter. During 8086 operation, refresh is performed by a software interrupt handler using the 2 mSec clock.

The H-1000 is installed in place of the existing CPU board, and works with all standard Heath/Zenith boards, peripherals, and accessories (with the sole exception of the 16K memory expansion board, which cannot be used). Power consumption is the same as the original (8.6 watts), but is distributed differently: +5vdc at 1.3 amps (regulated), +8vdc at 150mA, and +/-18vdc at 25mA. Two additional I/O connectors have been added on the right side of the board, for a total of five. The three original memory expansion connectors on the left side of the board have been replaced by a single two-row connector. One row of this connector is identical to the H/Z89 and works with existing jumper wires, memory-mapped I/O boards, etc. The second row provides additional address, data, and control signals for future high-performance expansions (DMA controllers, video graphics, etc.).

3.03 THE MEMORY MAP

All H-1000 memory lies within a 1 megabyte memory space (1,048,576 bytes). It is a byte-oriented system, so every byte in memory has its own address, and is selected by a unique combination of the 20 address lines AO-A19. It is most convenient to describe these addresses in hexadecimal (trying to use doubly-split octal will just hurt your head). So for the following discussion we will use hex exclusively. Thus, we can describe the memory space as going from 00000 to FFFFF hex.

The majority of H-1000 memory is composed of dynamic RAM (called "system RAM" by Heath). The actual amount of RAM available will depend on your particular H-1000; standard memory sizes are 128K, 256K, 512K, and 1 megabyte. In each case, RAM begins at 00000 and extends upward in one contiguous block. The memory is fully decoded, so trying to read a non-existent location will return only "air", i.e. a random value. Thus you can determine the size of memory by testing the read/write performance of each of the four possible upper RAM boundaries (1FFFF for 128K, 3FFFF for 256K, 7FFFF for 512K, and FFFFF for 1 megabyte).

An all-RAM system is fine, but it must first be initialized. Heath provided a special bank of memory called "Bank 0" for this purpose, and this same method is used in the H-1000. Bank 0 is enabled following power-up or reset, and replaces the lowest 8K of system RAM with 6K of ROM (read-only memory) and 2K of static RAM. The ROMs contain a machine-level monitor and the software necessary to bring in an operating system from disk. The static RAM (called "floppy RAM" by Heath) provides a minimal amount of RAM for this software, and has some special characteristics as described below.

3.04 BANK 0 MEMORY

Bank 0 is controlled by bit 5 of General Purpose Port A (GPA) at port address F2 (hex). Setting this bit low enables Bank 0; setting it high disables Bank 0 and removes it from the memory map. Following power-up or reset GPA is cleared, so Bank 0 is enabled. The remaining bits in GPA do other interesting things; they are described under "General Purpose Port A", section 3.06. For now it is sufficient to know that clearing GPA also enables the Z80 CPU with a 2 MHz clock.

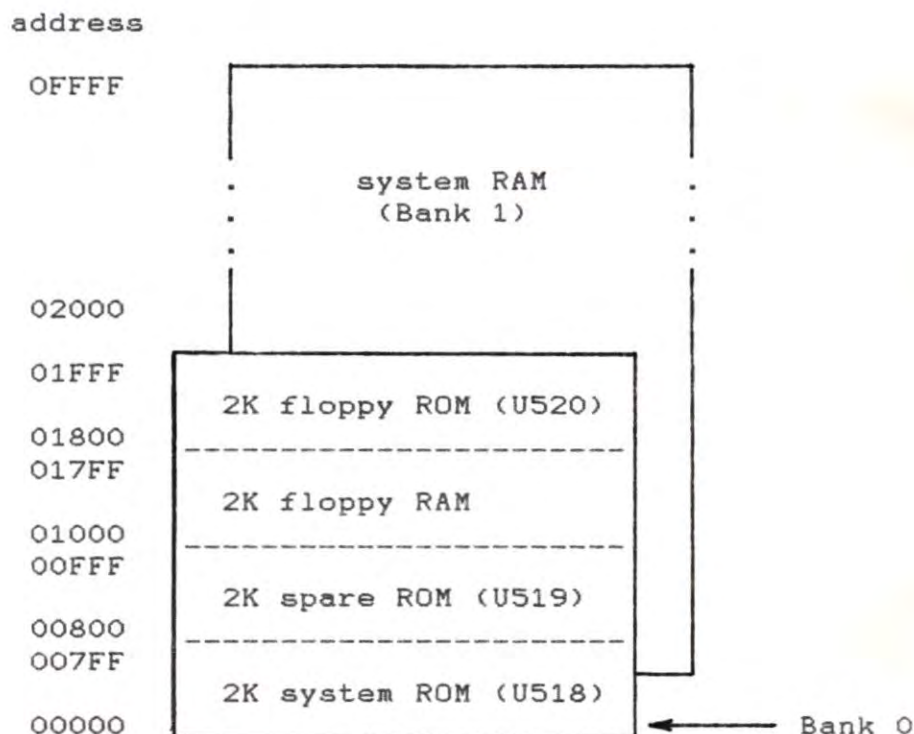


Fig. 3-1 Z80 Segment 0 Memory Map with Bank 0 Enabled

Figure 3-1 shows the Z80's memory map with Bank 0 enabled. The lowest 8K of system RAM has been replaced by Bank 0 and is no longer accessible. U518 is the system ROM, and typically contains Heath's MTR-90 or other equivalent machine-level monitor ROM. Since the Z80 begins execution at address 00000, the system ROM will be the first thing executed after a power-on or reset. If the monitor program needs more than 2K, either 2 ROMs are used (U518 and U519) or a single 4K ROM is placed at U518. The remaining ROM socket (U520) normally contains the disk read routines to boot an operating system from the H/Z89's H17 or equivalent disk drive.

Figure 3-2 shows the 8086 memory map with Bank 0 enabled. The 8086 begins execution at address FFFF0 following reset, so Bank 0 is relocated to the top of memory instead of the bottom. Also notice that the floppy RAM and ROM have been rearranged. This is because the ROMs contain Z80 code which cannot be executed by the 8086. Therefore the floppy RAM is placed at the very top of the memory map. This is the same Bank 0 RAM that appears at address 01000-017FF for the Z80. Since the Z80 is always selected following reset, it can load a program for the 8086 into system memory, then load an 8086 jump instruction (JMP) to that program into the floppy RAM. You can then switch to the 8086 and it will execute the desired program. More details are given on CPU swapping in section 3.18.

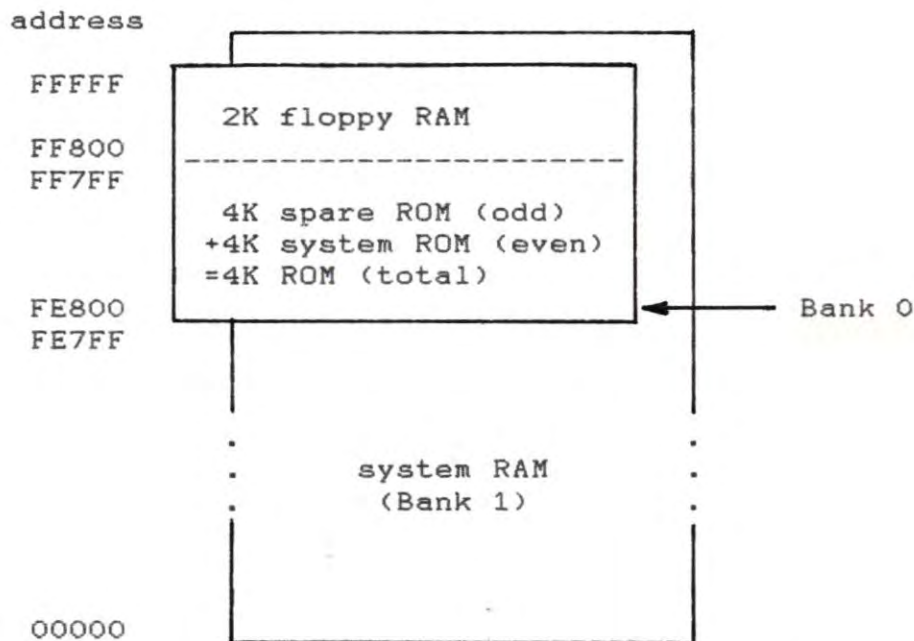


Fig. 3-2 8086 Memory Map with Bank 0 Enabled

The Bank 0 static RAM has one more unique feature. It can be write protected under software control. This can be useful during debugging since a program in write-protected RAM won't be damaged by a program crash. The H-1000 provides a jumper option at JJ509 to control this feature. If JJ509 is in the "1" position (normal Heath mode) and you have installed the Heath H17 hard-sector 5-1/4" disk controller (standard with most H/Z89's), the floppy RAM will be write protected following power-up or reset. The write protect is then controlled by bit 7 of port 7F (on the disk controller board). To enable writing to the floppy RAM, write hex 80 to port 7F (i.e. set bit 7); to write protect the RAM, write 00 to port 7F. If JJ509 is in the "1" position and you do not have the H17 controller, writing to the floppy RAM will always be enabled. If you place jumper JJ509 in the "0" position, the write protect will be controlled by bit 3 of General Purpose Port A. Again, the floppy RAM will be write protected following power-on or reset. To enable writing to the floppy RAM, set bit 3 of GPA. See sections 3.06 and 3.14 for details on using the General Purpose Ports A and B.

The Bank 0 ROMs normally contain Z80 code, and so are not executable by the 8086. However, the 8086 can read U518 (the system ROM) and U519 (the spare ROM). You can thus use special EPROMs containing both Z80 and 8086 code. The 8086 expects to read 16 bits at a time, so U518 and U519 are both read at once: U518 supplies the even bytes (bytes with an even address), and U519 supplies the odd bytes (with an odd address). A consequence of this is that the 8086 can read only 1/2 the bytes in each ROM. A pair of 4K ROMs in U518 and U519 occupy only 4K in the 8086 memory map; the odd bytes of U518 and the even bytes of U519 are inaccessible.

3.05 SYSTEM RAM

The_Z80_Map -- The Z80 processor has 16 address lines, and so can only address 64K directly (0000 to FFFF). Therefore the H-1000 has a segment register which supplies the remaining four bits needed to cover the full megabyte. This register is General Purpose Port B, at port address F3 (hex). Its upper four bits become the most significant hex byte of the 1-megabyte address for the Z80. The port is cleared by a power-up or reset, so the upper four bits are all 0's. Thus the Z80 will initially address the lowest 64K segment of memory, from 00000 to 0FFFF. The Z80 views each 64K segment the same, and can operate in any segment number. To find out which segment the Z80 is currently using, you can read General Purpose Port B; the most significant four bits defines the current segment number.

```

READSEGMENT: IN  OF3H      ; read General Purpose Port B
                ;
                ;           7 6 5 4 3 2 1 0
                ; REGISTER A = [ 0 0 0 0 0 x x x x ]
                ;
                ; A19  ↑
                ; segment A18  ↑
                ; number  A17  ↑
                ; is 0:  A16  ↑

```

To change the segment number, write the new value to the upper 4 bits of GPB taking care to leave the lower four bits as they were. The Z80 will immediately switch to the new segment after completion of the OUT instruction. Warning: This will change the Z80's entire memory map at once. You must have a valid program in the new segment being selected or the Z80 will crash! In effect, the next Z80 instruction will be fetched from the address [program counter + (segment# * 10000hex)]. For example, to switch from segment 0 to segment 2:

```

WRITESEGMENT: MVI  A,020H  ; load register A with 20 hex
                OUT  OF3H   ; write to General Purpose Port B
                (JMP $+20000H) ; (an implied jump is performed)

```


Notice that there is a "Catch 22" here. Since the Z80 can only access memory in its current segment, it cannot initialize the memory in a different segment. But it can't switch to a segment that isn't already initialized. This problem is solved with the 8086. It can address the entire 1 megabyte memory space directly, and can initialize the various memory segments for Z80 use. Thanks to the speed of the 8086, even block moves can be done quickly (under 0.1 second for 64K). Thus elaborate memory management systems can be set up for the Z80 by using the 8086 as a memory manager. See the section on switching CPUs for more details.

The_8086_Map -- The Z80 and 8086 are actually quite similar architecturally. They both address memory on byte boundaries, and share the same 1 megabyte memory space. Thus every byte has a unique address, which is the same for both processors. Data can be passed between CPUs in RAM, and programs that are translated from one CPU to the other do not require address translation.

Like the Z80, the 8086 has a 16-bit program counter, stack pointer, data registers, etc. Thus it too handles its memory in 64K segments. But in contrast to the H-1000's single 4-bit segment selector for the Z80, the 8086 has a sophisticated set of memory segmentation registers. There are four 16-bit segment registers; one each for the code, stack, data, and extra segments. These registers hold the base address used to calculate the physical memory address. They provide the 8086 with true memory management capability, essential in implementing multi-user and multi-tasking operating systems.

The 8086 can access either one or two bytes of memory at a time. This is accomplished by splitting RAM memory into an odd half and an even half, and giving each half its own select line. The 8086 preferentially accesses both odd and even halves simultaneously -- thus it can fetch its programs and data up to twice as fast as the Z80 (or even the 8088) even at the same clock rate. Actually, all of this is handled automatically by the 8086 itself: For a complete explanation of the 8086's memory usage, please refer to the 8086 data sheet in Appendix E, the "iAPX86 User's Manual" by Intel Corporation, or "The 8086 Book" by Russel Rector and George Alexy.

3.06 GENERAL PURPOSE PORT A

General Purpose Port A (or GPA for short) is an 8-bit parallel I/O port, and is functionally identical to the general purpose port on the H/Z89. Reading GPA will return the switch settings of DIP switch SW501. This is usually done by the monitor program (Heath's MTR-90, etc.) to determine system configuration. Figure 3-3 shows the switch settings for MTR-90. For other ROMs refer to your monitor's documentation for switch position definitions.

SWITCH #								SWITCH DESCRIPTION	
7	6	5	4	3	2	1	0	(0 = on, 1 = off)	
-----								-----	
.	0	0	primary =	hard-sector 5-1/4" (H17)
.	0	1	primary =	8" floppy (H47)
.	1	0	primary =	8" hard/floppy (H67)
.	1	1	no device	
.	.	.	.	0	0	.	.	secondary =	soft-sector 5-1/4" (H37)
.	.	.	.	0	1	.	.	secondary =	8" floppy (H47)
.	.	.	.	1	0	.	.	secondary =	8" hard/floppy (H67)
.	.	.	.	1	1	.	.	no device	
.	.	.	0	boot from	primary device
.	.	.	1	boot from	secondary device
.	.	0	test memory	upon power-up
.	.	1	normal	
.	0	set console	baud rate to 9600
.	1	set console	baud rate to 19200
0	normal	
1	auto-boot upon power-up	

Fig. 3-3 DIP Switch SW501 Settings with MTR-90

The GPA port address is F2 hex (or 362 octal). Any Z80 input instruction can be used to read port F2 and place its value in the designated CPU register. Similarly, the 8086 instruction "IN AL,F2H" or its equivalent will read GPA and load the value into the low byte of register A. Note that an 8086 8-bit input instruction must be used: A 16-bit input instruction will read port F3 (hex) instead.

As with the H/Z89, OUTputting a byte to GPA controls various hardware features of the H-1000 as defined in figure 3-4. Note that you cannot read what you have written to GPA (you'll get the status of switch SW501 instead). It is therefore a good practice to save a copy of the output in RAM so you can read it later. This will be necessary in case you need to alter one bit while leaving the rest alone. Heath's HDOS and CP/M operating systems both have defined locations for such a byte. See your manuals for further information.

To write to GPA with the Z80, simply load the selected register with the byte to be output. Then use the appropriate output instruction to send it to port F2 (hex). Similarly, use an 8086 8-bit output instruction to port F2 ("OUT F2H,AL", etc.). Do not use a 16-bit output from the 8086 to GPA, or you will write to port F3 (hex) instead.

BIT #								DESCRIPTION
7	6	5	4	3	2	1	0	
.	(any write) clears 2 mSec clock interrupt
.	0	Z80 single-step disable
.	1	Z80 single-step enable
.	0	2 mSec clock interrupt disable
.	1	2 mSec clock interrupt enable
.	0	MEM1 disable (low)
.	1	MEM1 enable (high)
.	0	LED on (or: floppy RAM write-protect)
.	1	LED off (or: floppy RAM write enabled)
.	0	MEM0 disable (low)
.	1	MEM0 enable (high)
.	0	Bank 0 memory enable
.	1	Bank 0 memory disable
.	0	I/O0 disable (or: disk side 1 select)
.	1	I/O0 enable (or: disk side 2 select)
0	I/O1 disable (low)
1	I/O1 enable (high)

Fig. 3-4 General Purpose Output Port A (port F2)

3.07 Z80 SINGLE STEP

The Z80 single-step circuit is a debugging aid to allow tracing a program's execution one instruction at a time. It does not actually single-step the Z80. Instead, it lets the Z80 execute exactly one instruction of the user's program and then generates a level 2 interrupt. The interrupt causes a return to a debugging program such as Heath's DEBUG. This is similar to the more common approach which uses a software interrupt in memory, but has the advantage that it can trace even programs in ROM.

The single-step circuit is enabled by setting bit 0 of GPA high. It then waits for execution of the Z80 Enable Interrupt instruction (EI, hex FB). When it occurs, the circuit lets two more instructions be executed, and then generates a level 2 interrupt. This returns control to the debugger program, which can examine or change registers, memory, etc. or return to the user's program to single-step the next instruction.

To better understand how the single-step circuit works, study the following example. Assume that you are debugging the following program and that the "MVI A,01H" was the last instruction executed:

```

                MVI    A,01H
LOOP:          DCR     A
                CPI     0

```

Your debugging program will have to perform the following steps:

1. Push the address of LOOP (the instruction to be single-stepped) onto the Z80's stack.
2. Turn on the single-step circuit by writing a "1" to bit 0 of GPA.
3. Execute an EI (enable interrupt) instruction [starts the single-step circuit instruction counter at "1"].
4. Execute an RTI (return from interrupt) instruction. This pops the address of LOOP from the stack and places it in the program counter. [single-step circuit now counts "2" instructions].
5. The Z80 now executes the "DCR A" instruction at LOOP. [single-step circuit counts "3" instructions, and generates a level 2 interrupt].
6. Control now returns to your debugging routine via the interrupt. The Z80 program counter (pointing at the "CPI 0" instruction) will have been pushed onto the stack by the interrupt.

Your program can then examine and display register contents, etc. before repeating the procedure for the next instruction to be single-stepped.

The Z80 single-step circuit has no effect during 8086 execution. If the Z80 single-steps a CPU swap instruction (OUTput a "1" to bit 3 of GPB), the 8086 will also see the level 2 interrupt and must be prepared to respond to it.

3.08 2 mSEC CLOCK

When enabled, the 2 mSec clock generates a level 1 interrupt every 2 milliseconds (RST 1 on the Z80 or type 207 on the 8086). The interrupt will remain until the CPU clears it by writing to General Purpose Port A (GPA). Since you cannot read GPA, a copy of its contents should be maintained in memory (see section 3.06). Writing this copy to the port will thus not change any of its bits. For timing functions, the interrupt handler will usually increment a counter and then clear the interrupt before returning control to the interrupted program. Also, the first interrupt after turning it on will vary in length from 0 to 2 mSec since you may be beginning anywhere in the cycle.

3.09 MEMO, MEM1 CONTROL LINES

MEMO and MEM1 are two control lines going to the memory expansion connector. MEMO is controlled by bit 4 in GPA, and MEM1 by bit 2 in GPA. Writing a 0 to them will put them at a TTL "0" level; writing a 1 to them will put them at a TTL "1" level. MEMO is connected to pin 16, and MEM1 is connected to pin 17 of the memory expansion connector.

3.10 ON-BOARD LED

Bit 3 of GPA was unused in the H/Z89. We have added an LED to show its status, which can be used for test purposes, etc. Programming this bit low will turn the LED on; programming it high will turn it off. This signal is also routed to jumper JJ509: If you are not using an H17 hard-sector disk controller and wish to use the write protect feature of the floppy RAM, this bit may be used to control it. See section 3.04 for details.

3.11 BANK 0 MEMORY DISABLE

Setting bit 5 of GPA disables the 6k ROM and 2k static RAM from the memory map, and replaces it with dynamic RAM. The operation of the Bank 0 memory is described in more detail in section 3.04.

3.12 I/O0, I/O1 CONTROL LINES

I/O0 and I/O1 are two control lines going to the I/O expansion connector. I/O0 is controlled by bit 6 in GPA, and I/O1 by bit 7 in GPA. Writing a 0 to them will put them at a TTL "0" level; writing a 1 to them will put them at a TTL "1" level. The I/O0 line is reserved for disk side select when the H17 hard sector controller is used with double-sided drives. I/O0 is connected to pin 16, and I/O1 is connected to pin 17 of the I/O bus.

3.13 CONSOLE PORT

The H-1000 console port is an 8250 ACE as in the H/Z89, and is located at the same group of I/O addresses (E8-ED hex, 350-355 octal). The ports are defined below. Refer to Appendix E for more details on using the ACE.

<u>hex</u>	<u>octal</u>	<u>8250 Register Definition</u>
E8	351	Data transmit and receive register
E9	351	interrupt enable register
EA	352	line control register
EB	353	MODEM control register
EC	354	line status register
ED	355	MODEM status register

3.14 GENERAL PURPOSE PORT B

Figure 3-5 shows the bit assignments for General Purpose Port B (or GPB for short). This port is new on the H-1000 and controls many of its features. Unlike GPA, it is a bidirectional port; reading GPB will show you what the current status of all the control bits are. Thus, the preferred means of using GPB is to read it, mask the desired bits high or low, and write it back out. GPB is located at address F3 hex, 363 octal. It is cleared to all zero's upon power-up or a system reset.

RESET: Bits 0 and 1 control the reset lines to the two CPUs. This is useful for putting a CPU in a known state before switching to it. Leaving these bits either high or low has no effect, but a high-to-low transition will cause the chosen CPU to be reset. Reset thus requires two output instructions; the first to set the bit high, and the second to set it low. The "Reset" and "CPU Select" bits operate independently, so the second output instruction can reset and select a CPU at the same time.

A quirk in the design of the 8086 causes it to "seize" the bus when it is reset. Therefore, you should only reset the 8086 at the same time that you switch to it. If it is absolutely necessary for the Z80 to reset the 8086 without selecting it, add 3 NOPs (no-op instructions) following the last Z80 output instruction so it is doing nothing important when the 8086 grabs the bus.

If both CPUs are reset at the same time, a System Reset is performed. This resets the entire computer and all I/O boards (as if you pressed the right "shift" and "reset" keys simultaneously). Only the Terminal Logic Board is unaffected by this reset.

BIT #								DESCRIPTION
7	6	5	4	3	2	1	0	
-----								-----
.	1	1	no action; prepare to reset
.	0	Reset 8086 on 1-to-0 transition
.	0	.	Reset Z80 on 1-to-0 transition
.	0	0	System Reset on simultaneous 1-to-0 transition
.	0	.	.	Z80 clock at 2 MHz
.	1	.	.	Z80 clock at 4 MHz
.	.	.	.	0	.	.	.	select Z80 active; 8086 halted
.	.	.	.	1	.	.	.	select 8086 active; Z80 halted
X	X	X	X	Z80 memory bank select
								- bit 4 = A16
								- bit 5 = A17
								- bit 6 = A18
								- bit 7 = A19

Fig. 3-5 General Purpose Port B Bit Assignments (port F3)

Z80 CLOCK: On power-up or reset, this bit is low and the Z80 clock is set to 2 MHz. Setting this bit high sets the Z80 clock to 4 MHz. For hardware and software compatibility reasons, the Z80 clock is automatically reduced to 2 MHz during I/O instructions and accesses to Bank 0 memory (ROM and static RAM). The Z80 CLOCK bit is unaffected by this, and the Z80 returns to 4 MHz as soon as these special cycles are over. The Z80 CLOCK bit has no effect on 8086 operation.

CPU SELECT: This bit controls which CPU is active. When set to 0, the Z80 is active and the 8086 is halted. When set to 1, the 8086 is active and the Z80 is halted.

Z80 BANK SELECT: These bits supply the upper four address bits (A16-A19) to determine which of sixteen banks of RAM the Z80 will operate in. Using these lines, the Z80 can address up to 1 megabyte of memory. At power-up, these bits are all set to 0, so the Z80 operates in the first 64K of memory. Before changing banks, the new bank must be initialized by the 8086 so there is a program there for the Z80 to execute. These bits have no effect on 8086 operation.

3.15 STATIC RAM WRITE PROTECT

The hard sector (H17) disk controller board normally controls the write protect line to the disk RAM in Bank 0, which must contain the startup code for the 8086. AT POWER-UP THE DISK RAM IS WRITE-PROTECTED. To disable the write protect, write 80 (hex) to port 7F (hex). If the hard sector board is not installed, the RAM will always be writable unless JJ509 is set to zero: In this case, bit 3 of General Purpose Port B (GPB) will control it.

3.16 3-PORT TYPE BOARDS (SERIAL/PARALLEL PORTS)

Six I/O ports are available for 3-port type boards. Since each board has 3 ports, you can install two 3-port boards for a total of six serial and/or parallel ports. Each of the six ports decodes a block of eight consecutive I/O addresses as follows:

3-port board at:	P504+P510, P505+P511 (normal or 1st board)		P502+P508, P503+P509 (optional 2nd board)	
I/O port address:	hex	octal	hex	octal
-----	-----	-----	-----	-----
label on back: "LP"	E0-E7	340-347	60-67	140-147
"DTE"	D8-DF	330-337	68-6F	150-157
"DCE"	D0-D7	320-327	70-77	160-167

Note that Heath 8-bit software won't expect a second 3-port board, so will ignore it unless you write your own program or modify and reassemble the BIOS. The 16-bit software for the H-1000 does not have this problem, and can be configured to use these ports without reassembly.

3.17 DISK TYPE BOARDS (DISK CONTROLLERS)

Three I/O ports are available for disk controller boards. This allows up to three disk controller boards to be installed at once. Each port decodes a block of either four or eight consecutive I/O addresses as follows:

Controller board at:	P506+P512	P504+P510	P502+P508
		P505+P511	P503+P509
I/O port address:	hex octal	hex octal	hex octal
	-----	-----	-----
	7C-7F 174-177	78-7B 170-173	50-57 130-137

The Heath H17 hard-sector controller board can only be installed at P506+P512, because it controls the Floppy RAM write protect. The other Heath disk controllers (H37 5-1/4" soft-sector, H47 8" floppy, and H67 8" Winchester) all provide jumpers to allow them to be installed in any location.

Note: Heath 8-bit software won't expect a disk controller board in either of the two new I/O slots. The Heath BIOS only supports two controllers at once, and restricts the I/O addresses they can be at (without modifying and reassembling the BIOS).

3.18 USING THE 8086

System start-up for the Z80 is quite straightforward. The Z80 is automatically selected following power-up or a system reset, and begins program execution at address 00000. Since a reset also enables Bank 0, there will be ROM memory at this address. The program in this ROM contains Heath's MTR-90 monitor or its equivalent. It sets up the Z80 side of the H-1000, and prints the familiar "H:" prompt. From there, you can use the monitor's built-in commands, or "boot" additional software from the disk.

Things on the 8086 side are more complicated. Before enabling the 8086, there must be a program in memory for it to execute, and the 8086 must be initialized to find it. The simplest 8086 initialization is a reset, which causes it to begin execution at address FFFF0 (hex). There is RAM at this address, so the Z80 must be used to put a program there for the 8086 to find. This program is called the "Start Vector", because it is usually just a "JUMP" instruction to where the real program begins.

The Z80 is initially stuck in the first 64K of memory, and so can't reach address FFFF0 directly. The H-1000 uses the 2K of write-protectable static RAM (called "Floppy RAM" by Heath) to get around this problem. The address of this RAM changes depending on which CPU is running (see fig. 3-6). When the Z80 is active, this RAM is at address 01000-017FF. When the 8086 is active, the RAM moves to address FF800-FFFFFF. Thus, the Z80 can load an 8086 Start Vector (or other program) into the Floppy RAM, and the 8086 will find it when it begins execution. Once the Start Vector is loaded, and assuming the Z80 is running in the lowest 64K with Bank 0 enabled:


```

SWITCH: MVI  A,080H ; (optional) if H17 hard-sector controller is
        OUT  07FH ; installed, write-enable Floppy RAM
                ; (note: doesn't save port contents)
                ;
        MVI  A,008H ; (optional) if JJ509 is in position "0",
        OUT  0F2H ; write-enable Floppy RAM (note:
                ; doesn't save contents of GPA)
                ;
        MVI  A,01H ; Set Reset bit for 8086 (see section 3.14)
        OUT  0F3H ;
                ;
        MVI  A,08H ; Select and reset 8086 (see section 3.14)
        OUT  0F3H ;
                ;
        --- ; (8086 executes next instruction at FFFF0)
                ;
        XXX ; (Z80 will resume here if enabled by 8086)

```

3.19 8086 SOFTWARE REFRESH

The H-1000 uses dynamic RAM for system memory. The data in this type of memory must be refreshed every 2 mSec or it will be lost. The Z80 performs this refresh function automatically, but the 8086 requires special provisions to do it. In the H-1000, the 2 mSec clock generates an interrupt every 2 mSec. An interrupt handler program then performs the actual memory refresh. This method takes a minimum of hardware, is quite flexible, and can minimize refresh overhead.

Each memory IC requires that you do a "read" or "write" cycle to any 128 consecutive locations (rows) every 2 mSec, or 256 locations every 4 mSec (see data sheets in Appendix E). Being a 16-bit CPU, the 8086 can refresh 1 row of 16 ICs per memory cycle. With a full set of 32 RAM ICs, refresh thus requires $128 \times 2 = 256$ memory cycles every 2 mSec, or $256 \times 2 = 512$ cycles every 4 mSec. At 500 nSec per memory cycle, refresh overhead is thus $(256 \times 500 \text{ nSec}) / 2 \text{ mSec} = 6.5\%$.

The actual refresh program can be quite simple. For an H-1000 with 128K or 512K (16 RAMs), executing any 256-byte program every 2 mSec (or 512 bytes every 4 mSec) takes care of it. The program can be 256 "NO-OP"s, 128 fast 2-byte instruction like "MOV AX,AX", or a program to perform some special function every 2 mSec that only incidentally takes 256 bytes. An H-1000 with 256K or 1024K (32 RAMs) is a little more complex. Here, the refresh program must do 256 cycles in each bank of 16 RAMs. This could be done by a string comparison instruction (REP, CMPS), where the two strings are in different blocks.

In some cases the 2 mSec clock must be disabled (during H37 disk transfers, for example). Such programs must then perform memory refresh themselves. For more information on refresh handlers, refer to the software source listings supplied with your H-1000.

3.20 H-1000 INTERRUPTS

INTERRUPT	Z80	8086	FUNCTION
Level 0	RST 0	TYPE 199	unused
Level 1	RST 1	TYPE 207	2ms clock (8086 REFRESH)
Level 2	RST 2	TYPE 215	Z80 single step
Level 3	RST 3	TYPE 223	I/O boards and console
Level 4	RST 4	TYPE 231	I/O boards
Level 5	RST 5	TYPE 239	I/O boards
Level 6	RST 6	TYPE 247	unused
Level 7	RST 7	TYPE 255	unused

3.21 8086 I/O

The 8086 is a 16-bit CPU, and has both 16-bit and 8-bit I/O instructions. However, all I/O ports in the H/Z89 (and thus the H-1000, for compatibility) are only 8-bits wide.

If the 8086 tries to input or output 16 bits to an 8-bit device, half the data will be lost. For example, you can't initialize both bytes of the 8250's baud rate divisor with a single 16-bit output instruction; the 8250's data bus is only 8 bits wide, and the upper byte is lost.

Therefore, use the following procedures with the 8086 to talk to any H/Z89 I/O devices:

Odd I/O port address:

Use only 16-bit 8086 I/O instructions, and subtract one from the desired port address (making it an even number). The data will be exchanged with the low byte of the A register (AL).

Disregard the upper 8 bits of the data; it is "air" from the non-existent upper half of the data bus.

Even I/O port address:

Use only 8-bit 8086 I/O instructions. The data will be exchanged with the low byte of the A register (AL).

Disregard the upper 8 bits of the data; it is "air" from the non-existent upper half of the data bus.

OCTAL ADDRESS -----		HEX ADDRESS -----
377	-----	FF
373	-----	FA
372	NMI (Z80 only)	F9
364	-----	F4
363	GENERAL PURPOSE PORT B *	F3
362	GENERAL PURPOSE PORT A	F2
361	-----	F1
360	NMI (Z80 only)	F0
350	-----	E8
340	LP SERIAL I/O	E0
330	DTE SERIAL I/O	D8
320	DCE SERIAL I/O	D0
200	SYSTEM RESERVED	80
174	RIGHT DISK CONTROLLER	7C
170	LEFT DISK CONTROLLER	78
160	I/O PORT 4 *	70
150	I/O PORT 5 *	68
140	I/O PORT 6 *	60
130	I/O PORT 7 *	58
0	-----	0

(* = ADDED FOR THE H-1000)

Fig. 3-5 H-1000 I/O Map

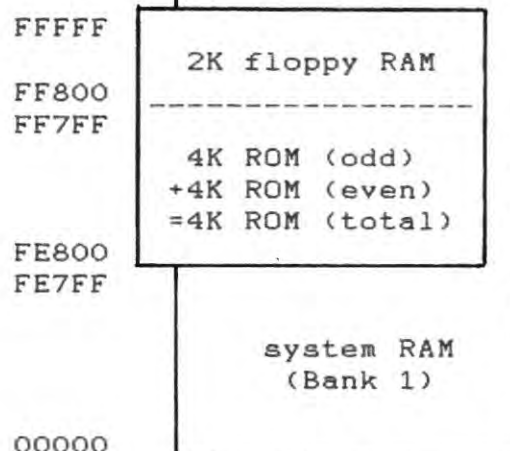
Bank 1 RAM (Z80 and 8086)
with bank 0 disabled

address

FFFFF	F
F0000	
FFFFF	E
E0000	
FFFFF	D
D0000	
FFFFF	C
C0000	
FFFFF	B
B0000	
FFFFF	A
A0000	
9FFFF	9
90000	
8FFFF	8
80000	
7FFFF	7
70000	
6FFFF	6
60000	
5FFFF	5
50000	
4FFFF	4
40000	
3FFFF	3
30000	
2FFFF	2
20000	
1FFFF	1
10000	
0FFFF	0
00000	

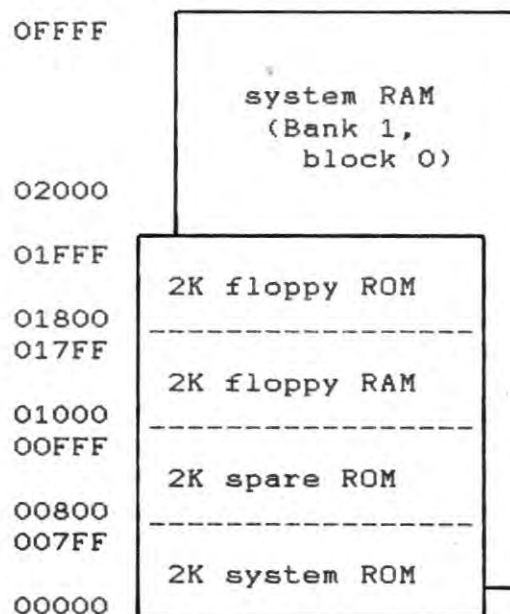
Bank 1 RAM (8086) with
bank 0 enabled

address



Bank 1 RAM (Z80) with lowest 64K
selected and Bank 0 enabled

address



- When Bank 0 is disabled, the static RAM and ROM disappear from the memory map, leaving an all-RAM system.
- When Bank 0 is enabled, the static RAM and ROM replace the system RAM in the memory map as shown above.

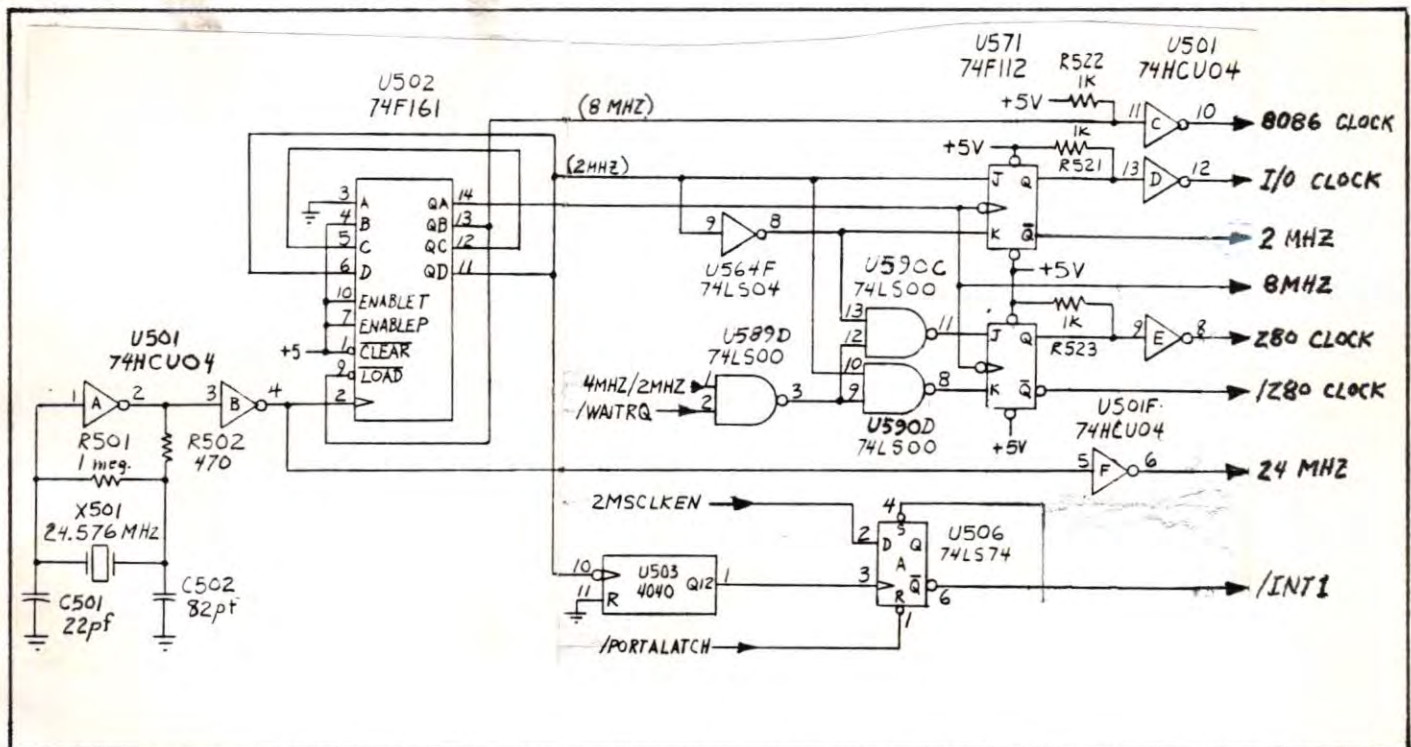
Fig. 3-6 H-1000 Memory Map

CHAPTER 4

CIRCUIT DESCRIPTION

4.00 INTRODUCTION

The following is a description of the H-1000 circuit operation. To make them easier to understand, the circuit diagrams here are somewhat simplified; see Chapter 5 for a complete set of circuit diagrams. Since some of the ICs used are quite complex, we've provided additional information on them in Appendix E, "Semiconductor Identification Charts". The following conventions are used: Bus signals are drawn as heavy lines, with the number of signals in the bus indicated by the number next to a diagonal line across the bus line. Signal names are capitalized, with a preceeding slash (/) if the active level of that signal is low. For example, RESET is active when high; while /RESET is active low. Signals with two active states have two names separated by a slash; the second name is active low. For example, 4MHZ/2MHZ means 4 MHz is selected if the signal is high, and 2 MHz if low. The numbers in parentheses after a signal name list the other sheets of the schematic where that name is used.



frequency. The oscillator output is buffered by U501B and fed to divider U502. U502 divides the clock by 3 to get 8.192 MHz for the 8086 clock, and by 12 to get 2.048 MHz for the 2 mSec clock. Flip-flop U571 and the associated gates form a synchronous divider. U571B generates the Z80's clock: 4 MHz if both 4MHz/2MHz and /WAITRQ are high (4 MHz Z80 operation and no wait states are requested), or 2 MHz if either 4MHz/2MHz or /WAITRQ is low (2 MHz Z80 or wait states requested). U571A always outputs a 2 MHz clock to the I/O bus connectors with identical timing to the 2 MHz Z80 clock. Since the H-1000 generates a wait request (/WAITRQ=0) during all I/O instructions, the Z80 will always perform I/O at 2 MHz to aid hardware compatibility with various I/O boards. The remaining sections of high-speed CMOS inverter U501 buffer the 24 MHz, 8 MHz, 4 MHz, and 2 MHz outputs and provide the high-level signals needed to drive the Z80 and 8086 clocks. Finally, U503 divides the 2 MHz clock down to 500 Hz for generating the 2 mSec clock interrupt.

4.02 SYSTEM RESET

When power is first applied, capacitor C506 is discharged and holds both T2 inputs of one-shot U507 low (see fig. 4-2). This causes them to trigger, and set their Q outputs high and /Q outputs low. The /Q output of U507B resets the Z80, the Q output of U507A resets the 8086, and the output of NAND gate U592A generates the /RESET signal to reset the rest of the system. The time constant of capacitor C506 and resistor R510 set the duration of the power-on reset signal to approximately 150 mSec.

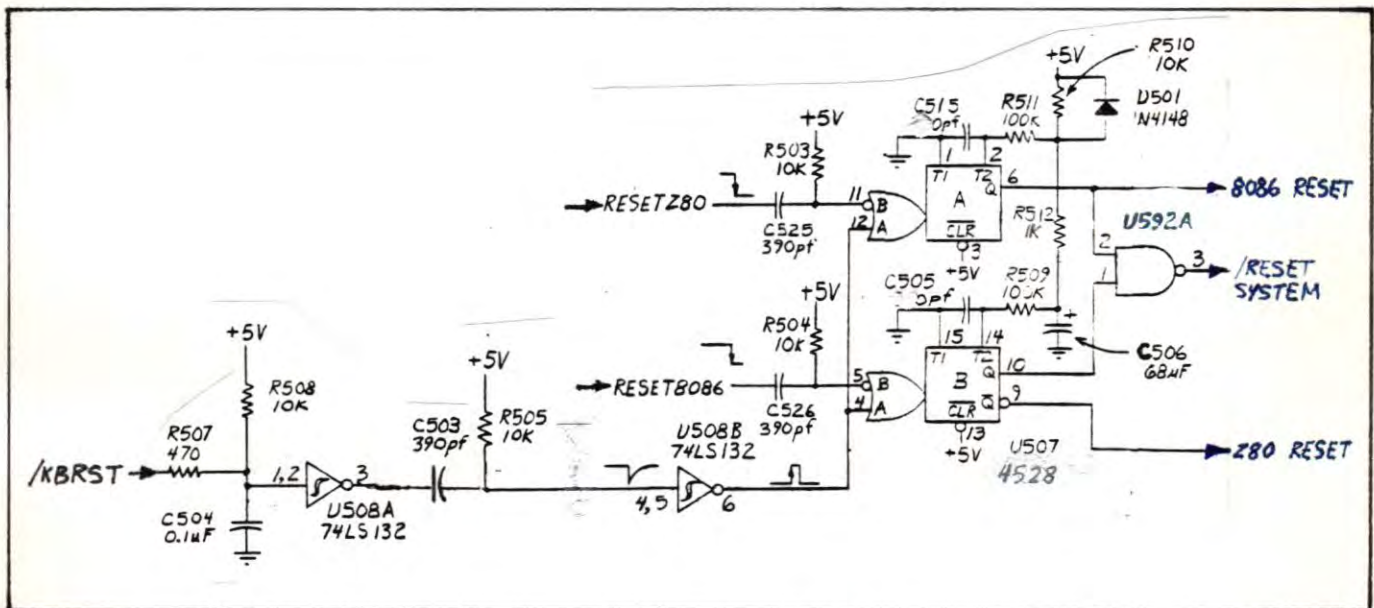


FIG. 4-2 SYSTEM RESET

A manual RESET can be performed from the keyboard by pressing the "reset" and right "shift" keys at the same time. This sets /KBRST low, so the output of Schmitt trigger U508A goes high. When the keys are released, /KBRST returns high, and the output of U508A goes low. This falling edge is inverted by U508B, and triggers both both one-shots, U507A and U507B. Each produces a 50 uSec pulse via its RC timing networks; R511 and C515, and R509 and C505 respectively. These pulses reset the Z80 and 8086 CPUs, and the rest of the system via NAND gate U592A.

Each CPU can also reset itself, each other, or the entire system. If bit 1 of General Purpose Port B (GPB) is reset from 1 to 0, its falling edge will be coupled via C525 and R503 to trigger one-shot U507B. Its /Q output then pulses low for approximately 50 uSec, resetting the Z80. Similarly, if bit 0 of GPB is reset from 1 to 0, its falling edge triggers one-shot U507A. Its Q output then pulses high for approximately 50 uSec, resetting the 8086. Since the 8086 sets its HLDA output active during reset, both CPUs will be held inactive during 8086 reset (see CPU Select Logic, below). If bits 0 and 1 of GPB are simultaneously reset from 1 to 0, both CPUs will be reset; additionally, NAND gate U592A resets the rest of the system (/RESET low) just as if a power-on reset had occurred.

4.03 Z80 CPU

U504 is an 8-bit Z80A, the 4 MHz version of the Z80 used in the H/Z-89 (fig. 4-3). It is fully software compatible with all 8080 code, and all 8085 code not using the RIM and SIM instructions. Following reset, the /WAIT and /BUSRQ lines will be high, so the Z80 will begin executing instructions. It outputs a 16-bit address on A0-A15 and control signals /MREQ, /IORQ, /RD, /WR, /M1, and /RFSH. All data transfers are done via an 8-bit bus (D0-D7). Each instruction fetch (/M1) cycle is automatically followed by a refresh cycle (/RFSH) to maintain data in the dynamic system memory. The Z80 continues to execute its program until one of the following occurs: a) interrupt line /INT or /NMI becomes active, which causes the Z80 to jump to an interrupt handler program; b) slow memory or I/O requests the Z80 to wait momentarily (via /WAIT); or c) the CPU Select Logic tells it to halt (via /BUSRQ) so the 8086 or other device can take over the bus.

4.04 8086 CPU

U570 in fig. 4-3 is an 8086-2 CPU, running at 8 MHz in the minimum mode. It is fully software compatible with the 8088 CPU used in the IBM PC and Zenith Z100, but has a true 16-bit data bus for faster operation. Following RESET, the CPU Select Logic sets the HOLD input high, so the 8086 is idle. When the CPU Select Logic sets HOLD low, the 8086 begins executing instructions. It generates a 20-bit address on A0-A19 and control signals /RD, /WR, M/IO, ALE, DT/R, and /DEN. The 8086 can access 8 bits at an even address (A0 low), an odd address (/BHE low), or both at once for a full 16 bits. Execution continues until either a) the interrupt line INTR goes active, which causes a jump to an interrupt handler program, or b) the CPU Select Logic requests it to wait (via READY) or halt (via HOLD).

4.05 CPU SELECT LOGIC

CPU selection is controlled by the 8086/Z80 signal from General Purpose Port B, bit 3 (see fig. 4-3). When 8086/Z80 is low, the Z80 is selected, and has control of the address, data, and control busses. The 8086 is halted by a high on its HOLD input via gates U577B and U589A, so its address, data, and control lines are all in a high impedance state. To switch to the 8086, the Z80 outputs a "1" to bit 3 of GPB (setting 8086/Z80 high). This causes gate U573B to set the Z80's /BUSRQ input active. The Z80 then halts at

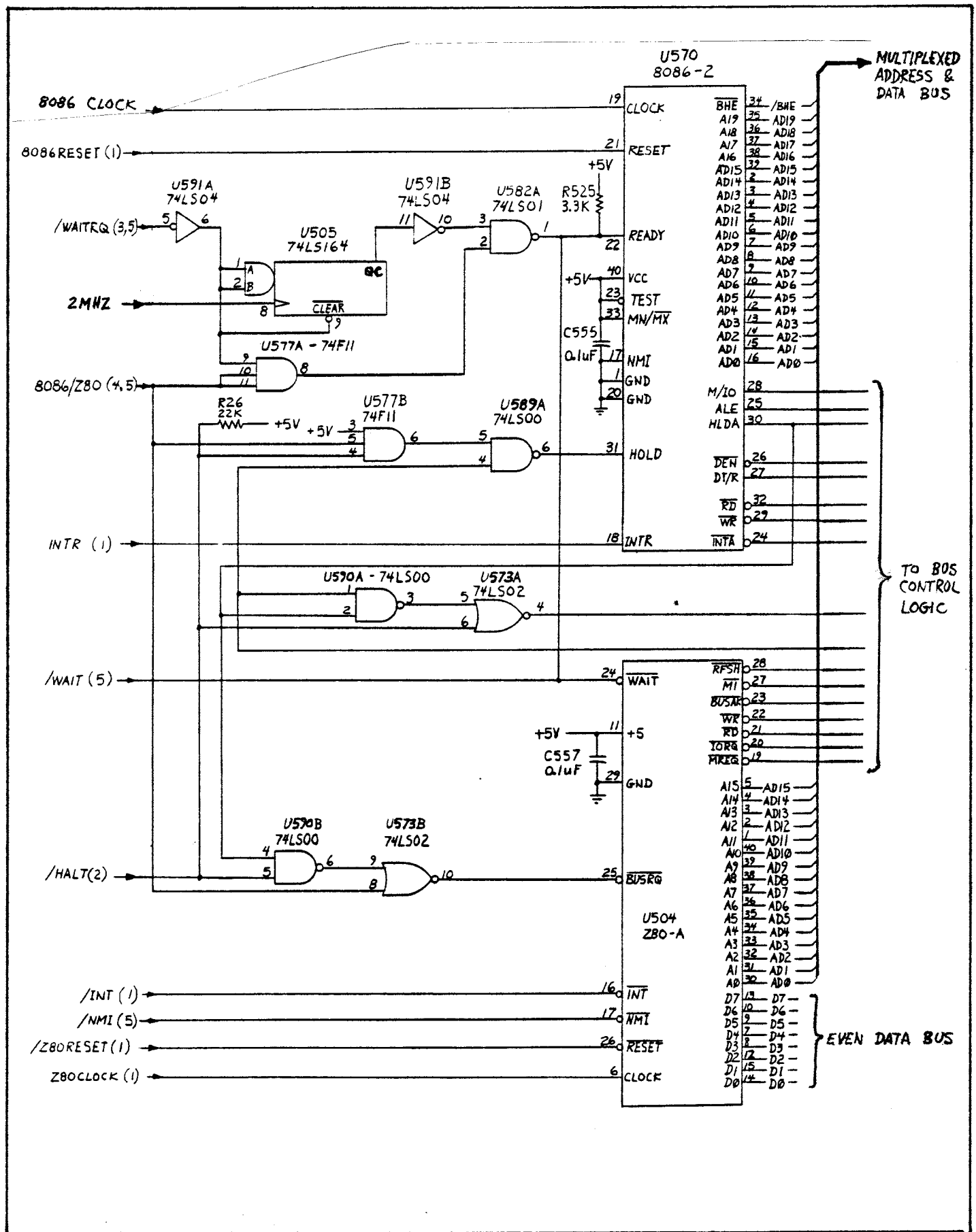


FIG. 4-3 Z80 AND 8086

the end of the current output instruction, disables its address, data, and control outputs, and sets /BUSAK active. /BUSAK is inverted by U589B, and via U589A sets the 8086's HOLD input low. The 8086 responds by setting its HLDA output low, takes control of the address, data, and control busses, and begins execution. To switch back to the Z80, the reverse procedure is followed. The 8086 writes a "0" to bit 3 of GPB (8086/Z80 low), and gates U577B and U589A set the 8086's HOLD input active. The 8086 then halts at the end of the current instruction, tri-states its outputs, and acknowledges the hold with a high on HLDA. Gates U590B and U573B then set the Z80's /BUSERQ high, and the Z80 resumes execution. Each CPU stops smoothly at the end of the output instruction, and resumes its program execution where it left off when re-selected.

The /HALT line on the memory expansion connector allows an accessory board to halt both CPUs at once. When /HALT is pulled low, the currently running CPU halts at the end of the current instruction (leaving both CPUs halted). Gates U590A and U573A acknowledge the halt with a high on HALTA, and the address, data, and control bus drivers are all disabled. The accessory board then has complete access to all memory and I/O for applications requiring DMA controllers, etc. When /HALT is returned high, the bus drivers are reenabled, HALTA returns low, and the previously running CPU resumes execution where it left off. Care must be taken during DMA that the dynamic RAM is adequately refreshed.

4.06 WAIT STATE GENERATOR

The static RAM, ROMs, and many I/O devices are not fast enough to run reliably at 4 MHz and above. Therefore, all I/O cycles and Bank 0 memory accesses are performed at the equivalent of 2 MHz. The wait request line (/WAITRQ) is pulled low during bus I/O instructions by PROM U588, or during Bank 0 memory accesses by PROM U516. During 8086 operation (8086/Z80 high) a low on /WAITRQ is inverted by U591A to enable shift register U505 and to set the output of U577A high (see fig 4-3). Since U505 was previously cleared, its QC output is low, and the output of U591B high. Thus both inputs of NAND gate U582A are high, and /WAIT goes low. This sets the READY input of the 8086 low, so it inserts wait states into the current cycle. Meanwhile U505 is being clocked at 2 MHz, so the high at its input is shifting right 1 position every 500 nSec. After 3 shifts (about 1500 nSec), the QC output goes high, one input of U582A goes low, and /WAIT returns high. The 8086 then completes the current cycle, returning /WAITRQ high. During Z80 operation, the wait state generator is disabled. Instead, /WAITRQ momentarily changes the Z80's clock to 2 MHz as described in section 4.1.

4.07 CONTROL BUS LOGIC

During Z80 operation, the Z80 outputs the read (/RD), write (/WR), memory request (/MREQ), I/O request (/IORQ), refresh request (/RFSH), and instruction fetch (/M1) signals. U509 buffers the first four to produce /BRD, /BWR, /BMREQ, and /BIORQ, and /M1 is buffered by inverter U591C to produce BM1.

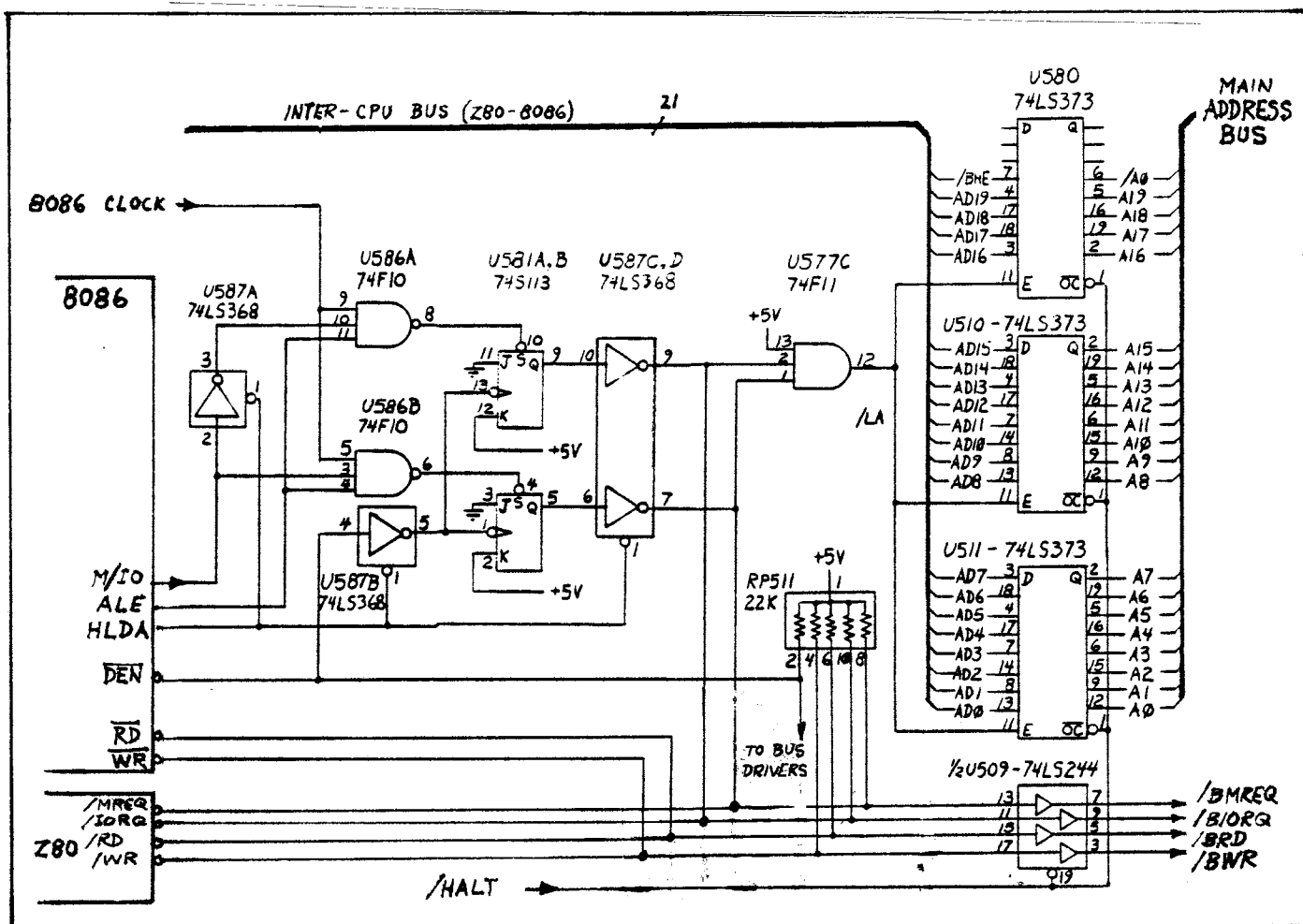


FIG. 4-4 CONTROL BUS LOGIC AND ADDRESS LATCHES

During 8086 operation, /RD and /WR are generated by the 8086 directly. /MREQ and /IORQ are created by U581, U586, and U587. At the beginning of each 8086 cycle, ALE pulses high. If M/IO is high (a memory cycle), the output of U586B goes low at the next 8086 clock cycle and sets U581B. The output of U581B is inverted by U587D to generate /MREQ. Similarly, if M/IO is low (an I/O cycle) it is inverted by U587A, the output of U586A goes low at the next clock cycle, and U581A is set. U587C inverts it to produce /IORQ. The 8086's clock is gated into U586A and -B so /MREQ and /IORQ won't begin until the address from the 8086 is stable. The cycle ends when the 8086's /DEN output goes high. Its rising edge is inverted by U587A, which resets U581A and -B to return /MREQ and /IORQ high. The 8086 does not use the /M1 or /RFSH signals; the Z80 continues to hold them in the inactive state during 8086 operation.

4.08 ADDRESS LATCHES

H-1000 memory is accessed by address lines A0-A19 and /A0 (fig. 4-4). It is divided into two 8-bit groups; even addresses and odd addresses. The 8086 generates these signals directly, and can read a byte at an even address (A0 low, /A0 high); an odd address (A0 high, /A0 low); or both at once (both A0 and /A0 low). The Z80 can read only one byte at a time, so if A0 is low /A0 must be high, and vice versa.

TO ADDRESS LATCHES

8086

AD0-AD15

DEN

DT/R

RD

U574 74LS245

AD15 4

AD14 3

AD13 2

AD12 8

AD11 7

AD10 5

AD9 6

AD8 7

AD7 2

AD6 3

AD5 4

AD4 5

AD3 6

AD2 7

AD1 8

AD0 9

U575 74LS245

AD7 2

AD6 3

AD5 4

AD4 5

AD3 6

AD2 7

AD1 8

AD0 9

U576 74LS245

D7 2

D6 3

D5 4

D4 5

D3 6

D2 7

D1 8

D0 9

U589C 74LS00

RD

BUSAK

Z80

D0-D7

ODD/EVEN (FROM MEMORY AND I/O DECODERS)

ODD DATA

EVEN DATA

During Z80 operation, U576 buffers data to and from odd RAM addresses and from ROM U519. It is enabled by a high on both /BUSAK (i.e., Z80 active) and ODD/EVEN (from address decoder PROMs U516 and U517, and I/O decoder PROM U588). The data direction is controlled by the /RD line; low defines a Z80 memory read, or high if a memory write. All reads and writes to even memory addresses, system ROMs, or to any I/O port are made via the even data bus; like the H89/Z89, this bus is not buffered.

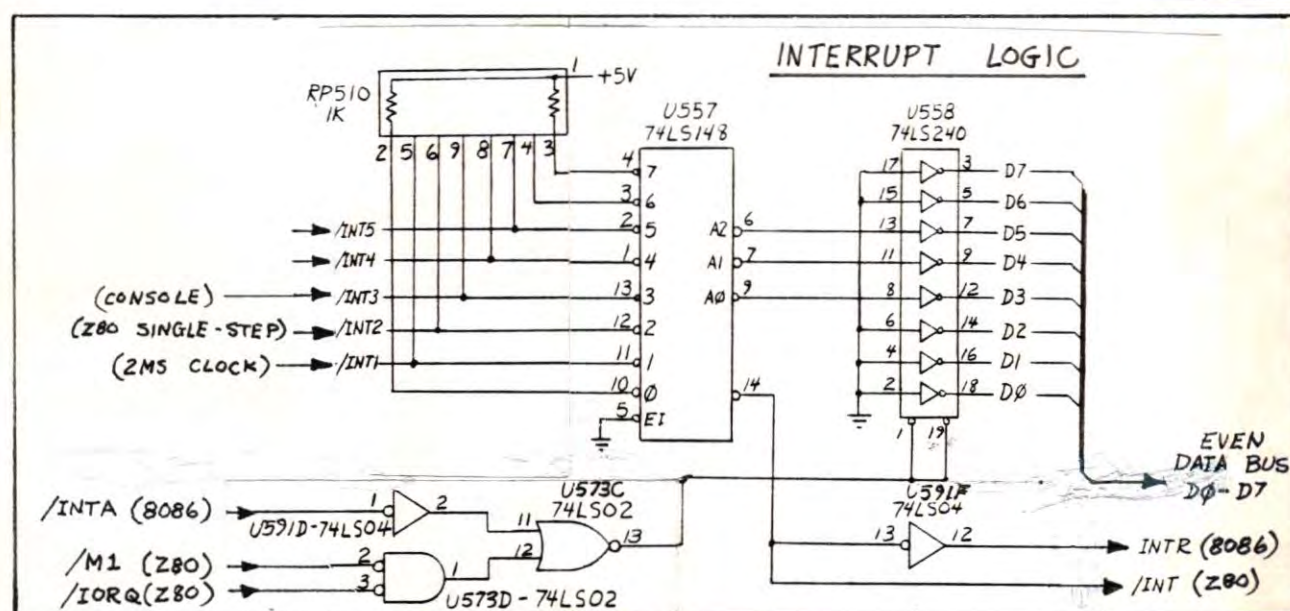


FIG. 4-6 INTERRUPT LOGIC

4.10 INTERRUPT LOGIC

All interrupts except /NMI are routed to priority encoder U557 (fig. 4-6). /INTACK is initially high, so bus driver U558 is disabled. When an interrupt line goes low, it pulls one input of U557 low. This causes U557 to set /INT active to the Z80, and INTR active to the 8086 via inverter U591F. If interrupts are enabled, the currently running CPU will respond with an interrupt acknowledge cycle: /INTA active if the 8086 is running, or a simultaneous /M1 and /IORQ if the Z80. These signals are decoded by U573C, -D, and U591D to produce /INTACK. This signal gates the interrupt number onto the odd data bus through buffer U558. The Z80 interprets this data as a Restart instruction; the 8086 uses it as a vector into a 1K-byte table at the low end of memory.

The Z80 receives a non-maskable interrupt (/NMI low) from I/O decoder U550 whenever there is an access to an I/O port reserved for the Heath H8 computer's front panel. With an appropriate interrupt handler, this allows programs written for the H8 to be run without modification. The 8086's NMI line is not used. If more than one interrupt occurs at once, the one with the highest priority will be recognized first. Once it has been cleared, the next higher one will be processed, etc. The highest priority is /NMI, then /INT5, /INT4, /INT3, Single-step (Z80 only), and the lowest is the 2 mSec Clock.

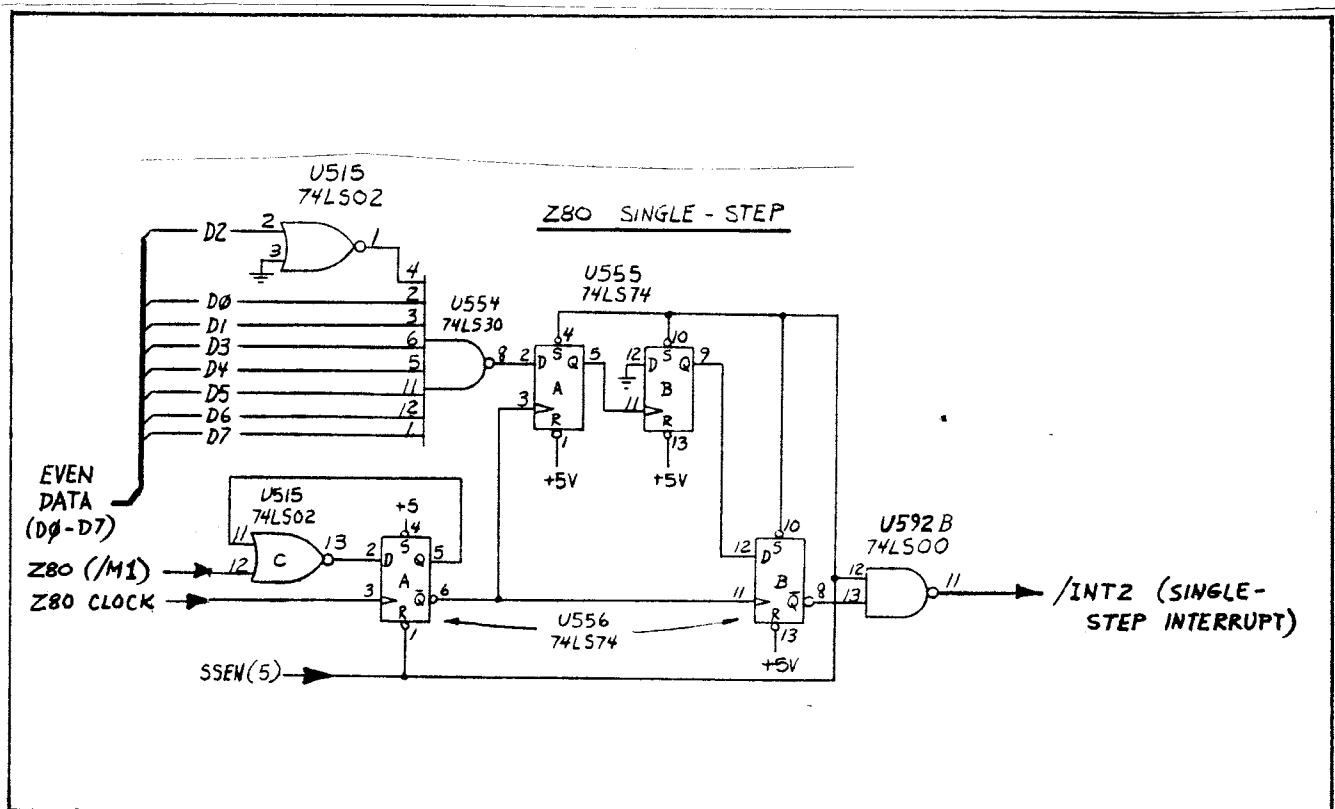


FIG. 4-7 Z80 SINGLE-STEP

4.11 Z80 SINGLE-STEP

The Z80 single-step circuit is identical to that used in the H89/Z89 (see fig. 4-7). When SSEN is low (bit 0 of General Purpose Port A), U555 and U556 are held reset and the output of gate U592B is disabled. When SSEN is set high, Z80 single-step is enabled. U556A synchronizes the /M1 signal to the Z80's clock. U515B and U554 decode the "EI" instruction. Thus execution of an EI instruction is detected and starts a counter consisting of U555A, -B, and U556B. The counter is incremented by each /M1 (instruction fetch) cycle. During the third instruction following "EI", the counter enables gate U592B to generate a level 2 interrupt.

The Single-step circuit is used with a monitor program such as Heath's DEBUG. To execute one instruction of a user's program, the monitor performs the following steps:

1. enable single-step [counter at 0...]
2. execute Enable Interrupt (EI) [...1...]
3. execute Return From Interrupt (RTI) [...2...]
4. (execute user's instruction) [...3!]
- *** INTERRUPT 2 ***
6. disable single-step (clears interrupt)
7. repeat as desired

The single-step circuit is not used by the 8086; it includes single-step as a built-in feature.

4.12 2 mSEC CLOCK

The 2 mSec clock is enabled by setting bit 1 of General Purpose Port A high (2MSCLKEN high). This makes the D input of U506 high, so the next rising edge of the 500 Hz signal from U503 will set U506A. This then generates a level 1 interrupt. When the currently running CPU responds to this interrupt, it is cleared by any write to port A. This causes the /PORTALATCH signal to pulse low, which resets U506. If 2MSCLKEN is again set high by a write to port A, the cycle will repeat in exactly 2 mSec.

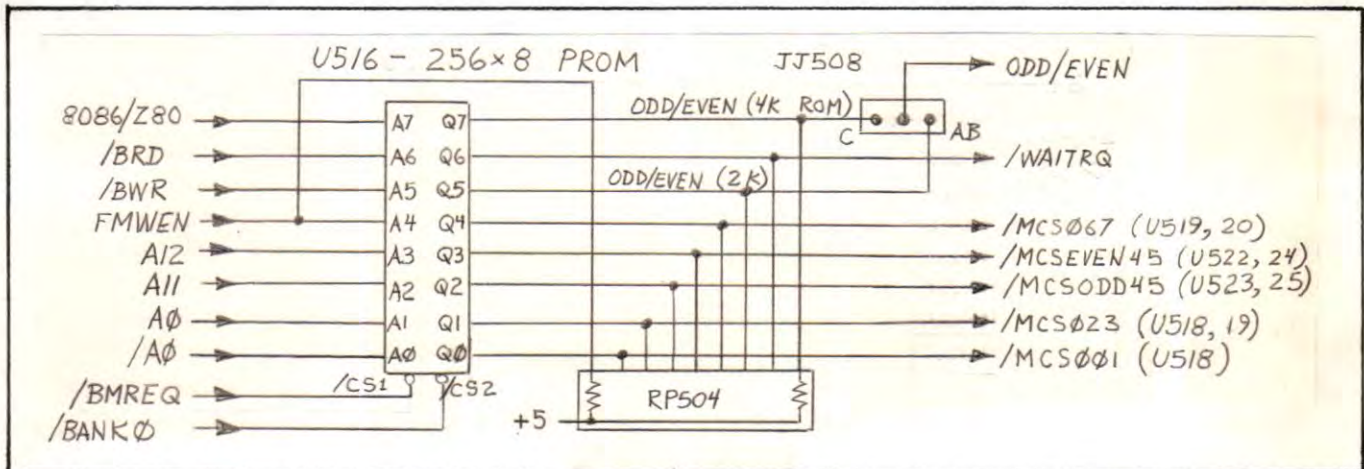


FIG. 4-8

4.13 MEMORY MAP DECODER

U516 and U517 are 256x8 PROMs which decode the latched address lines and determine which memory ICs are to be selected. U516 generates the chip selects and write enables for memories in Bank 0: U518-520 and U522-525. It also outputs /WAITRQ when any Bank 0 memory is selected, to enable wait states as needed and to deselect system RAM. Comparator U579 selects /Bank0 when it is enabled by /ENABLE0 (from General Purpose Port B, bit 5) and when the address is in the right range. When the Z80 is active (8086/Z80 is low), Bank 0 memory is accessed in the lowest 8K of the 1 megabyte memory map (00000-01FFF hex). When /BANK0 is low and 8086/Z80 is high (8086 active), Bank 0 memory is accessed at the very top of memory (from FE000 to FFFFF hex). The 2K of RAM in Bank 0 is also re-mapped to the top 2K to provide memory for an 8086 restart vector following reset. When /BANK0 is high, Bank 0 memory is disabled.

4.14 SYSTEM AND DISK ROMs

U518, U519, and U520 are the system ROMs, which reside at the bottom of Bank 0. Jumpers are provided to select 1K, 2K, or 4K devices, and either triple supply EPROMs (which require +5, +12, and -5 volts) or single supply (+5 volt) parts. Jumper JJ504 is in position "1" for 1K ROMs at U518 and U519; or position "0" for all other parts. JJ505 is in position "0" for triple-supply 2K EPROMs at U518 and U519, or position "1" for 2K single supply parts, or position "2" for 4K parts. JJ506 is in position "0" for triple-supply 2K EPROMs, or position "1" for all others. JJ507 is in position "A" when 1 or 2 2K parts are used in U518 and U519, or position "C" when a single 4K part is used at U518. Position "B" of JJ507 is not used, but is available for compatibility with the Heath H89 board. Jumper JJ508 is in position "AB" for 2K ROMs, or position "C" for 4K parts at U518.

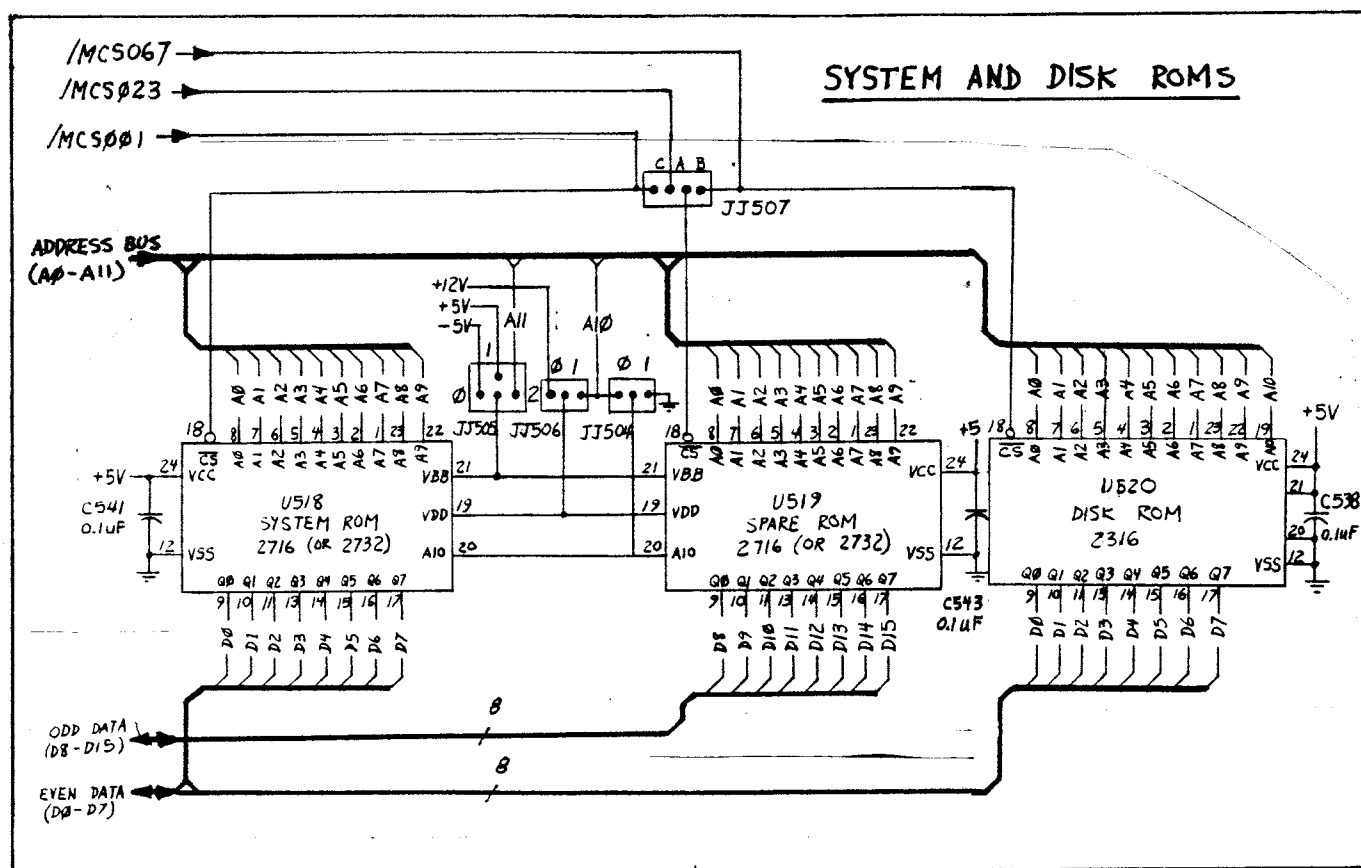


FIG. 4-9

4.15 FLOPPY DISK AND BOOT RAM

U522-525 are 1Kx4 static RAMs, organized to form 2K bytes of RAM. The lower 1K can be write protected via the FMWEN line by logic on the disk controller I/O board (socket P506 and P512). The RAM is connected to both the odd and even data busses, and can be used normally by both the Z80 and 8086 for either programs or data. During Z80 operation, this RAM is used by HDOS. During 8086 operation, it is used to store the restart vector, and is mapped at address FE000-FFFFF.

4.16 SYSTEM DYNAMIC RAM

The H-1000 uses two or four groups of dynamic RAMs, with 8 ICs per group. Either 64Kx1 or 256Kx1 parts may be used, although the following discussion assumes the 64K parts. A different PROM is used for U517 depending on whether 64K or 256K RAMs are used. For the 280, memory is divided into sixteen banks of 64K each, numbered 1 through 16. The 8086 can address the entire memory space directly.

PROM U517 controls the addressing of the dynamic system RAM, plus any additional memory in the memory expansion slot. A low on /BMREQ starts the cycle by enabling U517 and removing the clear from shift register U578 via inverter U591E. If either A0 or /A0 is low, U517 selects either the even (/RAS0 or /RAS2) or odd (/RAS1 or /RAS3) half of memory respectively. If both are low, both halves are enabled simultaneously. The shift register is clocked at 24 MHz, and so if /RFSH is high (not a refresh cycle), a "high" will propagate through the shift register one step every 40 nSec.

Multiplexers U513, U514, and U583 provide the multiplexed addresses needed by the RAMs and buffer the /RFSH, /RD, and /CAS signals. Initially, their Select inputs are low, and address bits A1-A8 are routed to the multiplexed address lines MA0-MA7 (and A17 to MA8 for 256K RAMs). The RAMs U526-541 latch this address on the falling edge of /RAS. About 80 nSec into the cycle, the QB output of U578 goes high, and the multiplexers route address bits A9-A16 to MA0-MA7 (and A18 to MA8 for 256K RAMs). 40 nSec later the QC output of U578 goes high, which is inverted by U583C to produce /CAS. The falling edge of /CAS latches the rest of the address and the RAMs can complete their cycle. The QG output of U578 is routed to U517, and when it goes high it causes the selected RAS outputs (/RAS0, /RAS1, /RAS2, and /RAS3) to return high. This insures an adequate RAM precharge time and lowers power consumption.

During a refresh cycle, /RFSH is low when /BMREQ goes low. U517 then selects all four banks of RAM at once (/RAS0-/RAS3 low), while /RFSH=low disables the shift register so /CAS will not go active. This performs a RAS-only refresh cycle. /RFSH is also inverted by U583D; this output disables the lower 8 address bits from U513 and U514, and replaces them with the current output from refresh counter U512 via buffer U521. At the end of the refresh cycle, the falling edge of RFSH increments the refresh counter. The 280 has an internal refresh counter, but it only provides 7 bits; the 256K dynamic RAMs need an 8-bit refresh, so an external counter is used.

During 8086 operation, memory refresh must be performed by a software program that reads 256 consecutive bytes every 2 mSec., using the 2 mSec clock interrupt. When all 32 RAMs are used, this must be performed in both banks. The 256K RAMs require 256 rows to refresh, so the 8086 software refresh program must read 512 consecutive locations instead of 256, and refresh overhead is approximately 3.5%.

4.17 I/O MAP DECODER

U550 and U588 are 256x8 PROMs that decode the I/O port addresses. U550 is the standard PROM supplied by Heath or other vendors. It is enabled by when /BM1 and /BIORQ are both low (an I/O cycle). This circuit is identical to the Heath H89A to insure hardware and software compatibility with other products. U588 is a new I/O decoder PROM, which decodes the I/O port assignments for General Purpose Port B, /WAITRQ, and the select lines for the two new I/O slots on the H-1000.

4.18 CONSOLE SERIAL PORT

The console serial I/O port is used to communicate with the internal H19 terminal logic board in the H89/Z89. U561 is the 8250 Asynchronous Communications Element (ACE) that converts 8-bit parallel data from the bus into serial data, and vice versa. U559 and U560 convert the TTL levels from the ACE into standard RS-232C signal levels. Capacitors C509, C510, C518-21, C527 and chokes L501-504 provide additional noise immunity and reduce radiated interference. The clock frequency for the ACE is set by crystal X502, capacitors C522 and C523, and resistors R515 and R516. Inverter U564 buffers the clock for the I/O bus, and provides the RESET, /BRD, and /BWR signals. Flip-flop U563 controls the I/O read and write timing for the ACE.

4.19 GENERAL PURPOSE PORTS

General Purpose Input Port A consists of buffer U551 and DIP switch SW501. When the I/O decoder selects port A (/IO362=low) and /BRD is low, gate U553A enables U551 to place the status of the DIP switches on the odd data bus. An open switch represents a "1", and a closed switch a "0".

General Purpose Output Port A consists of latch U552. It is reset to all 0's at power-on and each time /RESET goes low. When the I/O map decoder sets /IO362 low and /BWR is low, gate U553B latches the odd data bus status into U551.

General Purpose Output Port B consists of latch U584 and gate U553C. It is reset to all 0's during power-on and each time /RESET goes low. When I/O map decoder U588 selects /IO363 and /BWR goes low, the reset is removed from U563B by inverter U564D. The next rising edge of the 2 MHz clock will then set U563B, and the subsequent edge will again reset it. The latter produces a rising edge on U563B's /Q output shortly before the end of the output instruction. This edge latches the even data byte into U584 early enough so that if a CPU swap is requested, there is still time for the CPU Select Logic to stop the current CPU at the end of the output instruction.

General Purpose Input Port B consists of buffer U585 and gate U553D. It is selected when the I/O map decoder U588 enables /IO363 and /BRD is low. The inputs of U585 are connected to the outputs of U584, so reading Port B returns the current status of Output Port B.

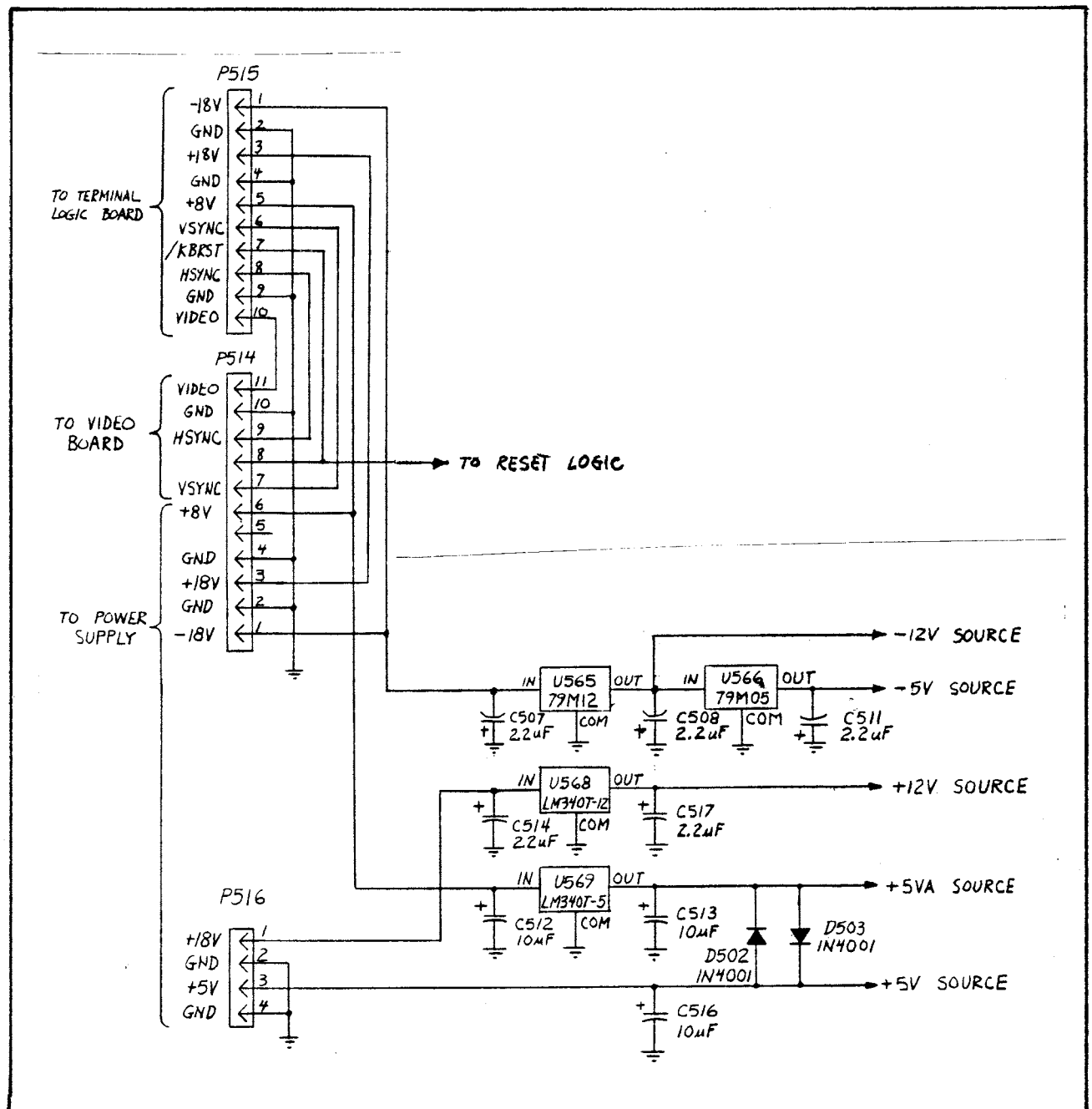


FIG. 4-10

4.20 POWER DISTRIBUTION

The H-1000 board requires +5vdc (regulated), and +8, +16, and -16vdc (unregulated). To reduce the load on the H89/Z89's +5vdc supply the RAMs have their own +5vdc regulator (U569), which uses the +8vdc input. Diodes D502 and D503 insure that the two supplies remain within 0.6vdc of each other. U565 is the -12vdc regulator for the RS-232C interface. U566 supplies -5vdc for 3-supply EPROMs. U568 is a +12vdc regulator for 3-supply EPROMs, the RS-232C, and the accessory board slots. Capacitors C507, C508, C511-14, C516, and C517 keep the regulators stable.



(8086 CLOCK; 8 MHZ)

8086CLOCK(2)

(I/O BUS CLOCK; 2MHZ)

2MHZ (5)

(WAIT STATE GENERATOR; 2MHZ)

WAITCLOCK(2)

(MEMORY EXP; 8MHZ)

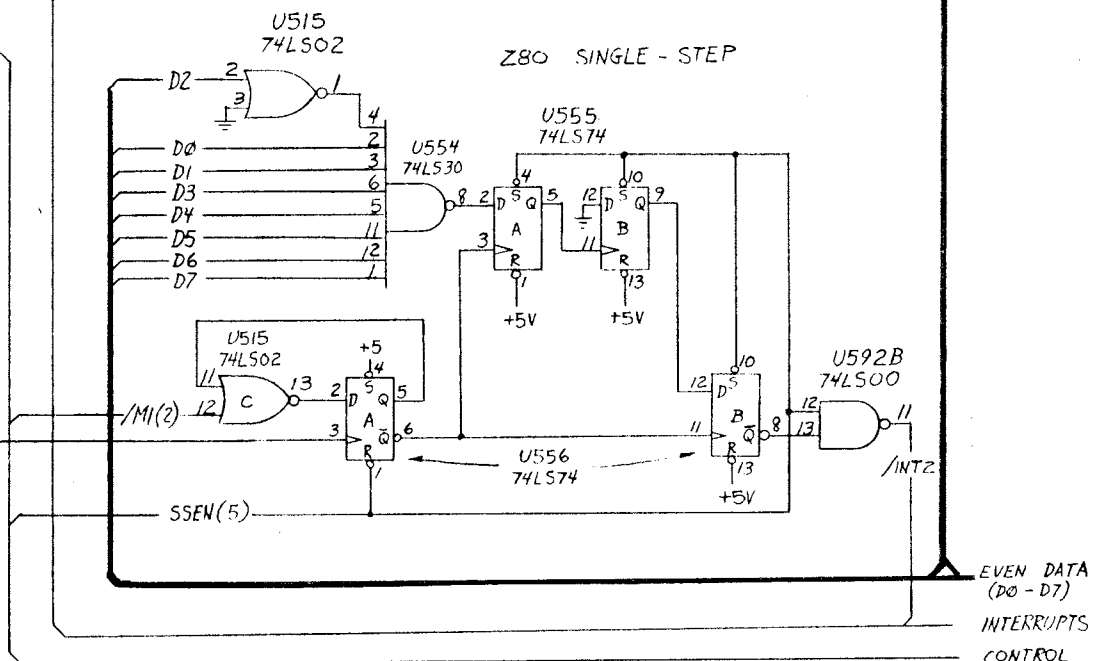
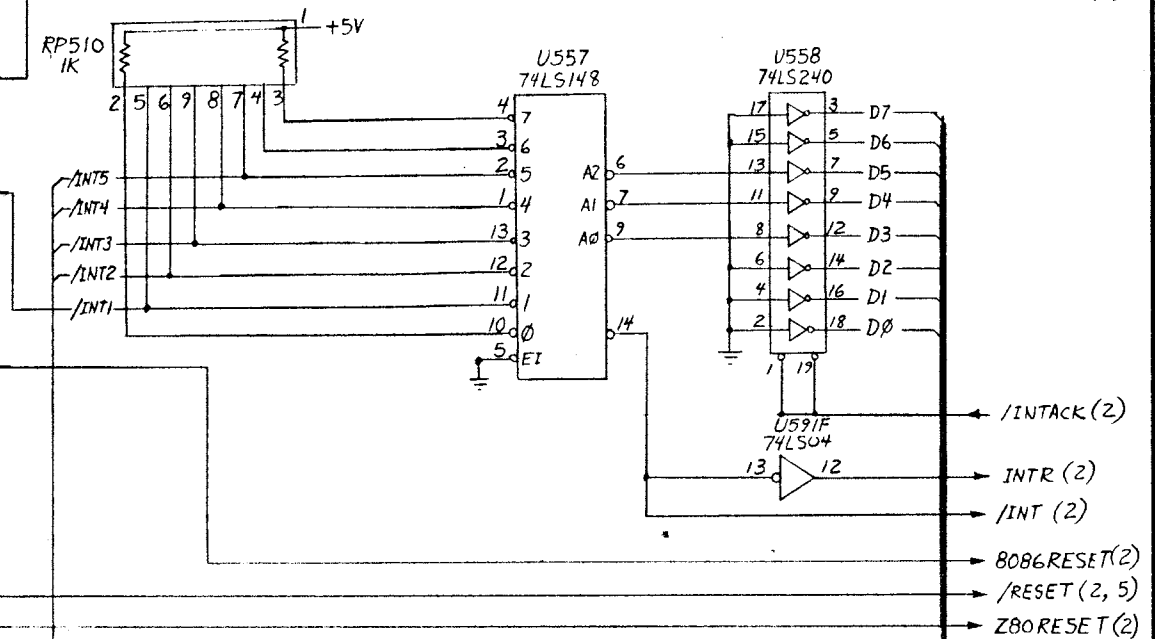
8MHZ (2)

(Z80 CLOCK; 2MHZ OR 4MHZ)

Z80 CLOCK(2)

(DRAM SHIFT REGISTER; 24MHZ)

24MHZ (4)

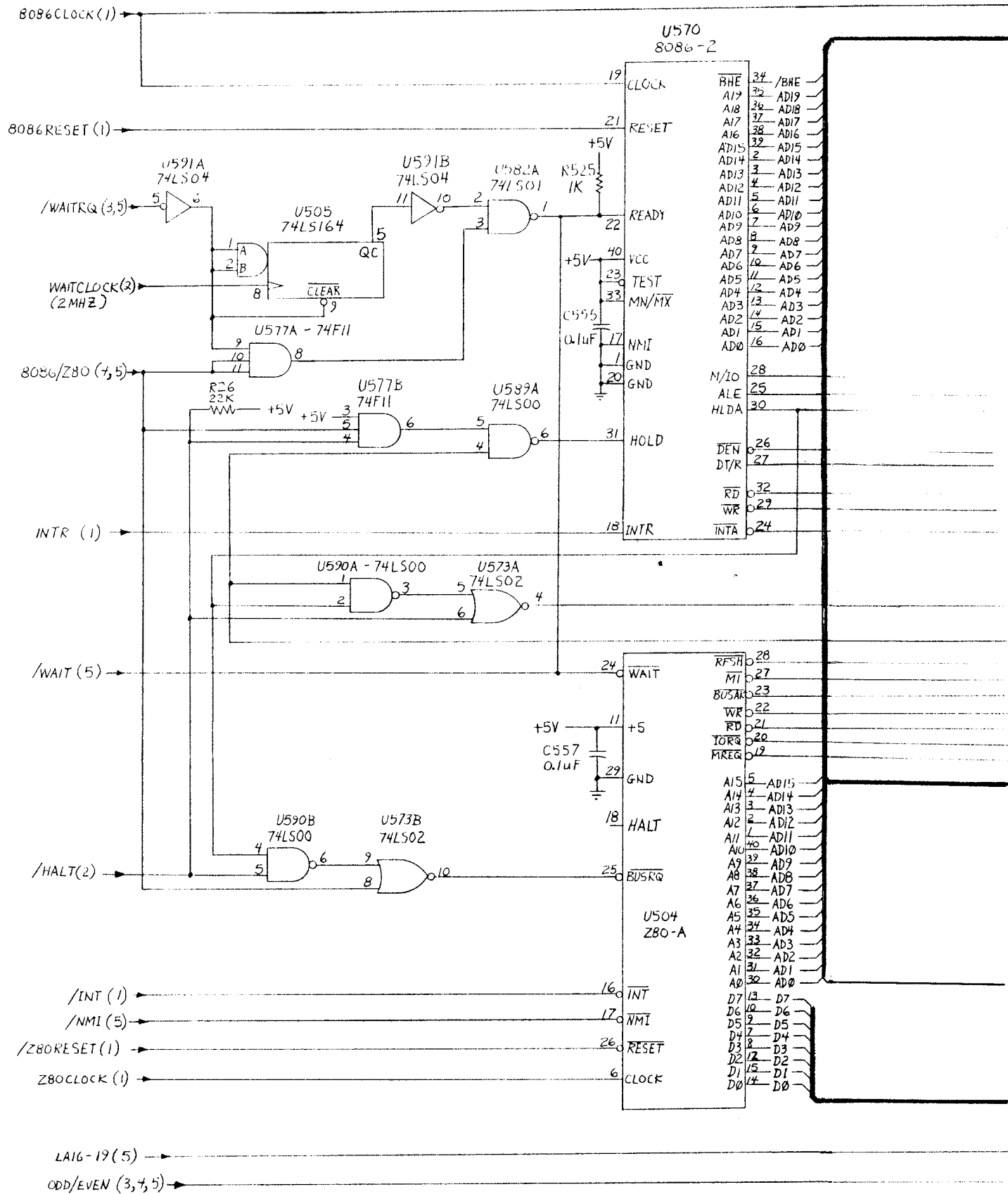


REVISIONS:

- 3/11/83 - U507, WAS 4528. ADDED R512
- 4/20/83 - ADDED PIN# TO U571.
- 6/16/83 - U572 REMOVED (LATCHED INT. REQUESTS).
- 9/1/84 - C505 WAS 390pf. C515 WAS 390pf.
- 10/4/85 - C506 WAS 68 uF.

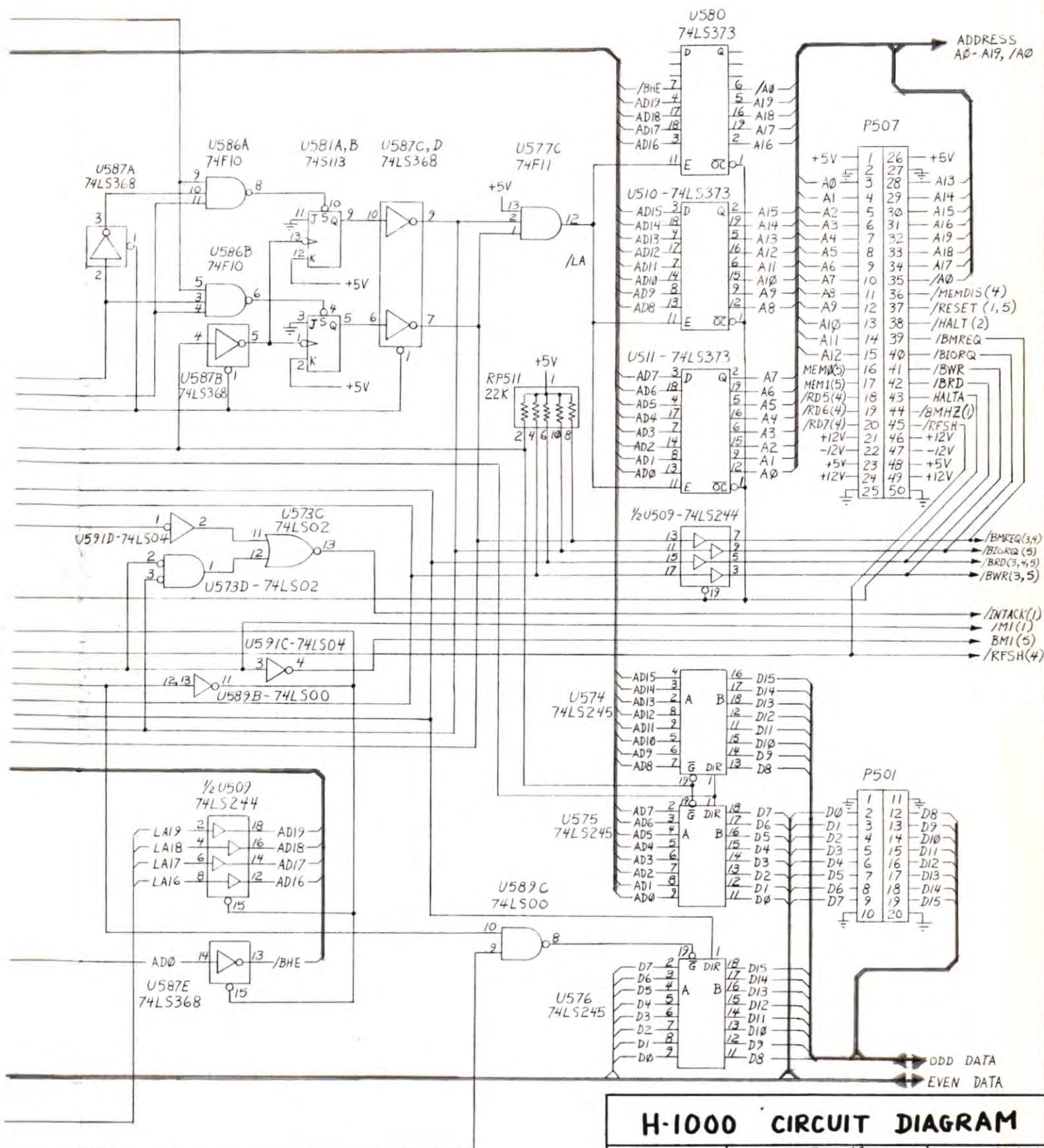
H-1000 CIRCUIT DIAGRAM

SCALE:	APPROVED BY	DRAWN BY
DATE: 11/22/82	John G. Hest...	10/4/85
H-1000 CLOCK AND SINGLE-STEP		DRAWING NUMBER
©1982 BY TECHNICAL MICRO SYSTEMS, INC.		35
366 CLOVERDALE ANN ARBOR MI 48106		SHEET 1 OF 5



REVISIONS

- 4/20/83 - R525, WAS 3.3K
- 10/2/84 - U505 PIN 8 WAS 8086 CLOCK (8MHZ).
- U591 PIN 11 WAS TO U505 PIN 13 (QH).



H-1000 CIRCUIT DIAGRAM

SCALE:

APPROVED BY *Tom Kotler*

DRAWN BY *L. Hart*

DATE: 2/21/83

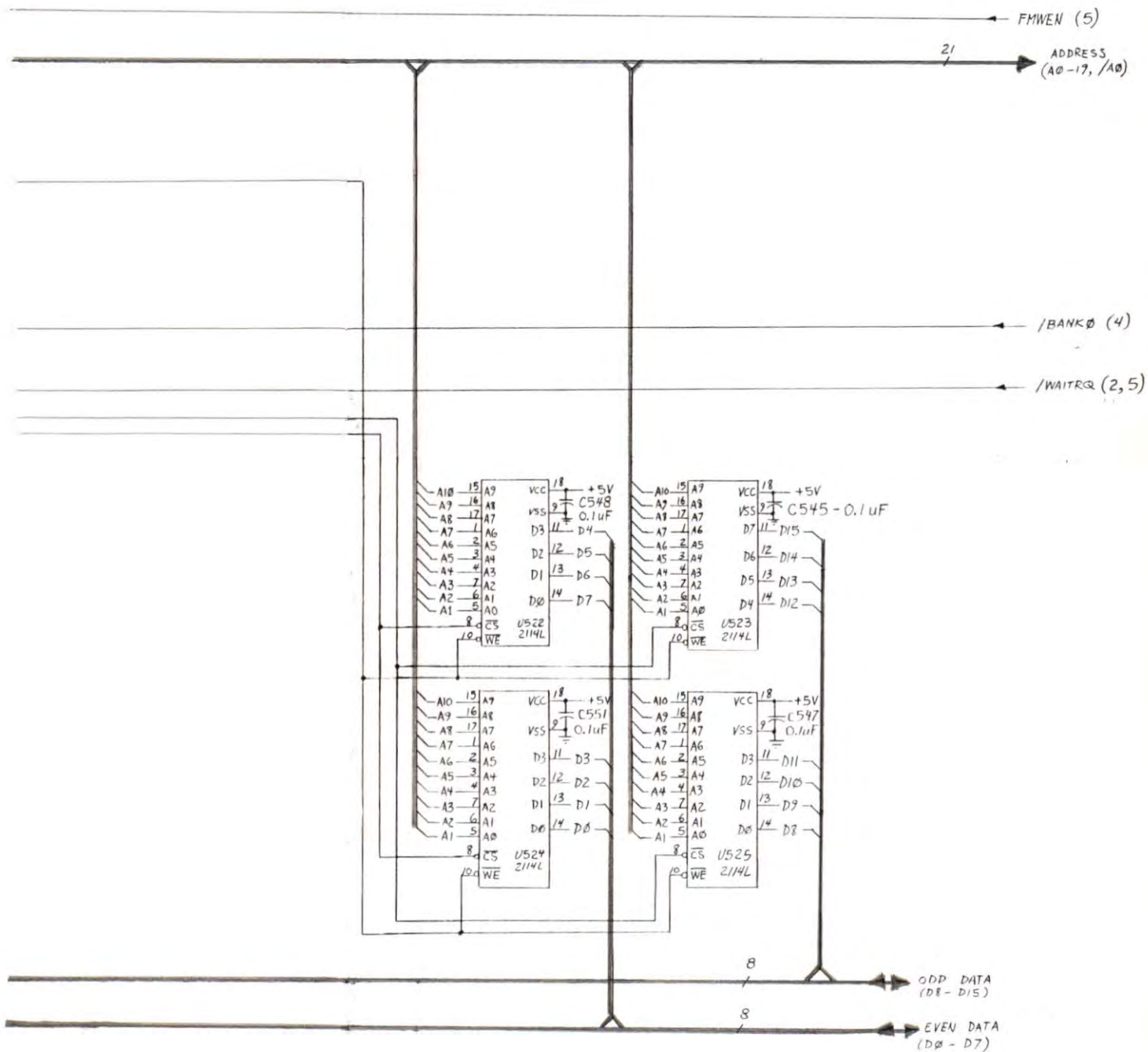
LAST RE: 4/20/83

H-1000 CPU AND BUS DRIVERS

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DRAWING NUMBER 35
SHEET 2 OF 5





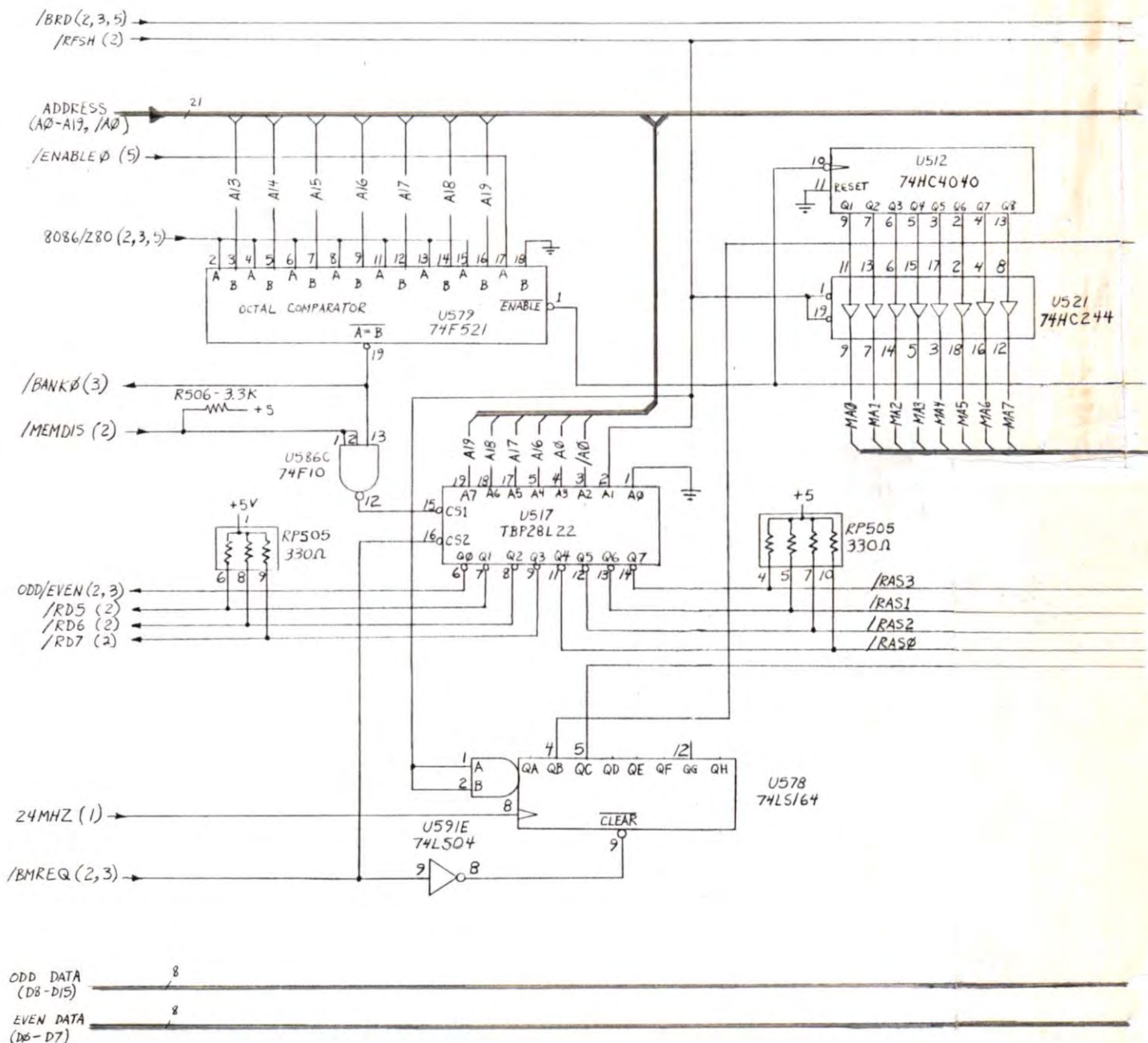
H-1000 CIRCUIT DIAGRAM

SCALE: DATE: 11/6/82 APPROVED BY: J. L. G. H. 12/4/82 DRAWN BY: R. Hart LAST REV. 3/4/83

H-1000 BANK 0 MEMORY

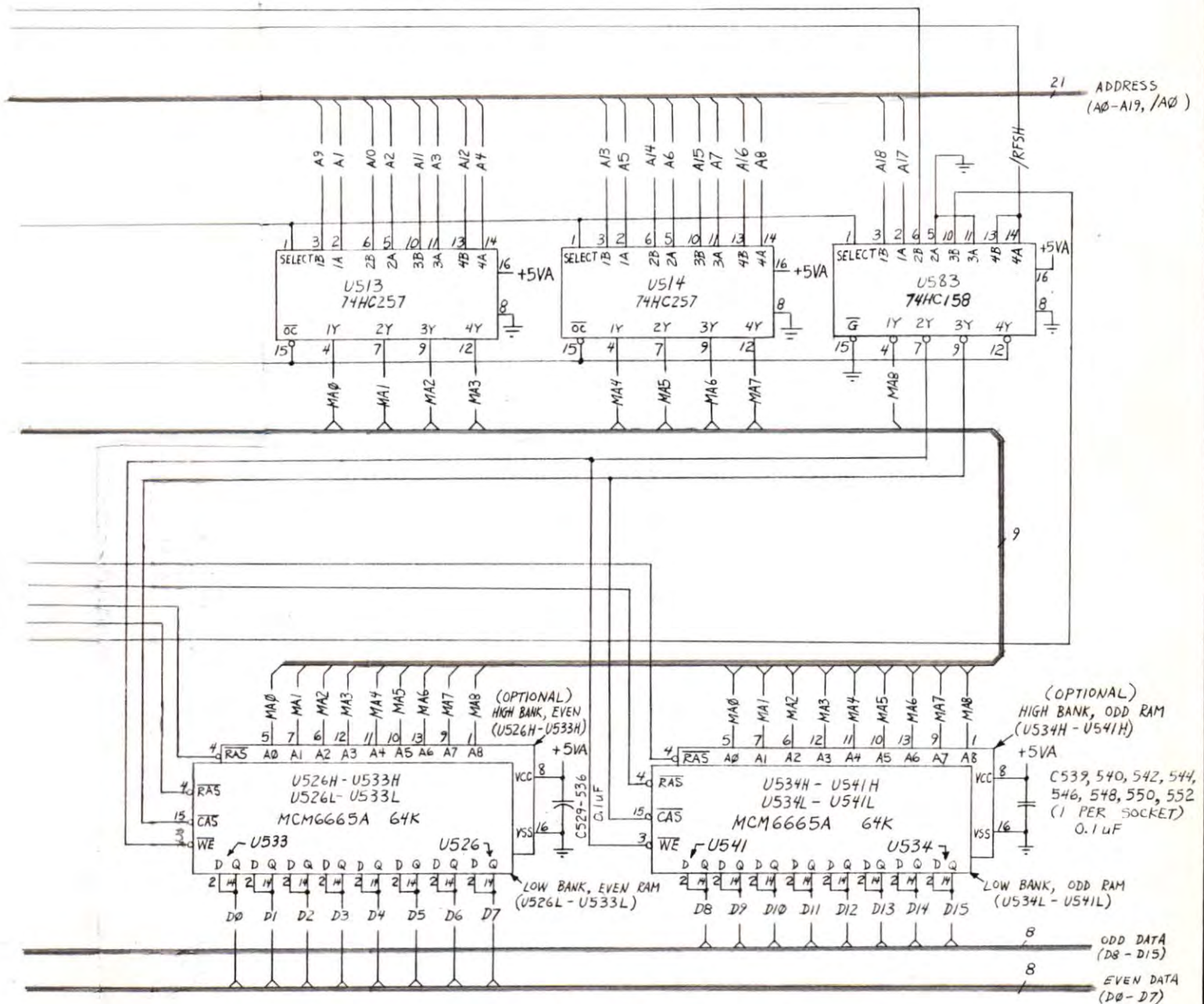
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366 CLOVERDALE ANN ARBOR MI 48105

DRAWING NUMBER 35
SHEET 3 OF 5



REVISIONS

- 4/15/83 - RP505, WAS 1K OHMS, WAS MISLABELED RP515.
- 9/19/83 - U512, WAS 4040. U521, WAS 74LS244.
- 7/9/84 - U578, "MUX" WAS ON PIN 4, NOW 3; "CAS" WAS PIN 5, NOW 4.
- 2/4/85 - U513, U514, U521, U583 CHANGED FROM 74LS- TO 74HC-.
- 8/1/86 - U517, PIN 1 WENT TO U578 PIN 12.



H-1000 CIRCUIT DIAGRAM

SCALE:

APPROVED BY *For [Signature]*

DRAWN BY *L. Hart*

DATE: 11/18/82

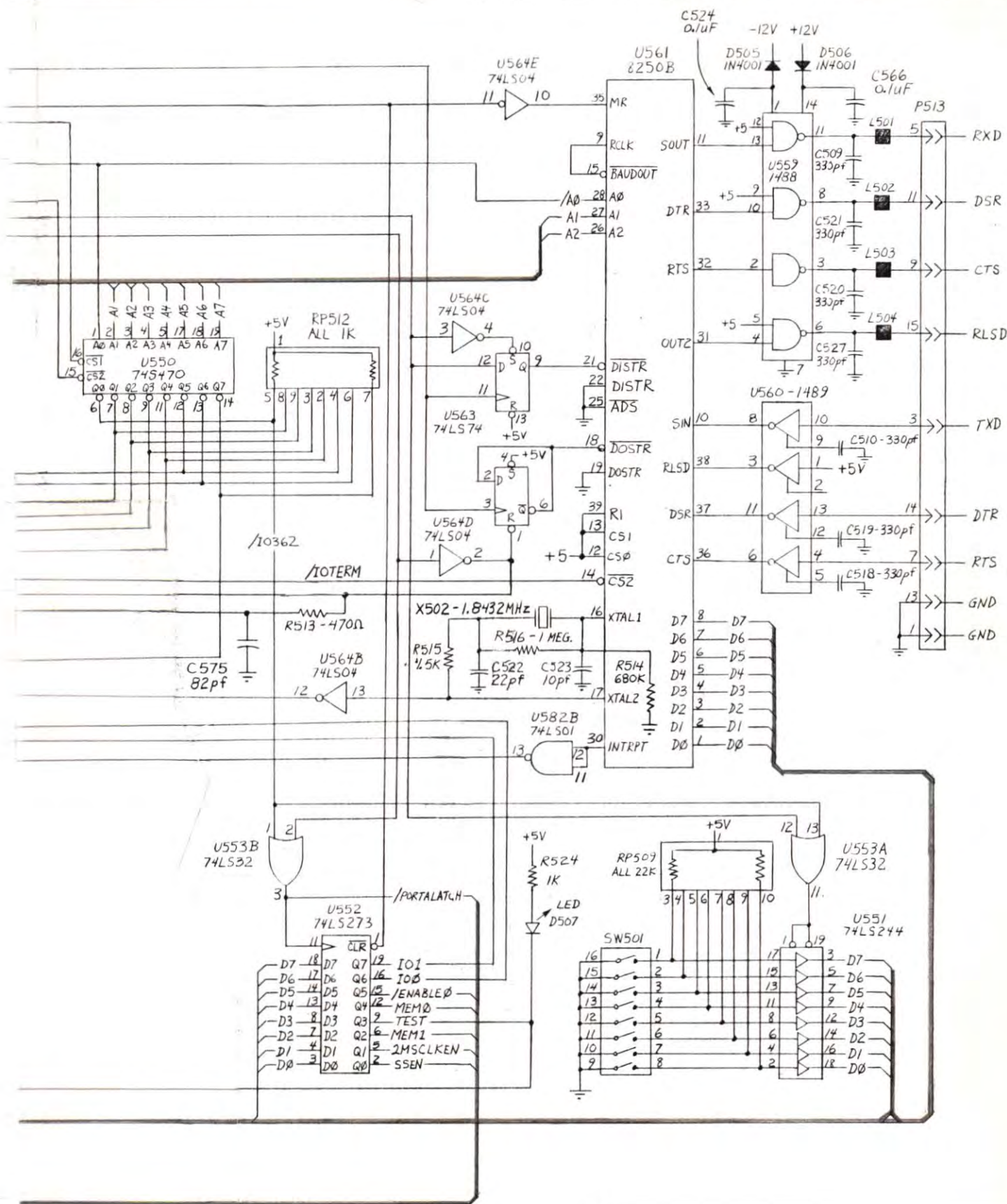
3

LAST REV. 8/1/86

H-1000 SYSTEM RAM

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DRAWING NUMBER
35
SHEET 4 OF 5



SCALE:	APPROVED BY <i>T. Andrew</i>	DRAWN BY <i>L. Hart</i>
DATE: 12/8/82		LAST REV. 5/19/86

H-1000 INPUT/OUTPUT

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CHAPTER 6

CONFIGURING THE H-1000

6.00 INTRODUCTION

The H-1000 board has a number of hardware configuration options to adapt it to your environment. In general, they control memory size (128K to 1 megabyte), memory addressing, and the type of memory ICs used. This chapter will describe your options, and how to make the most of them.

6.01 H-1000 JUMPER OPTIONS

The H-1000 has two types of jumpers. The first type configures the H-1000 for different types of EPROMs at U518-U520. These EPROMs normally come from your old CPU board, so the H-1000 can be set to use any EPROM that works in an H/Z89. Jumpers JJ504-508 are used for this purpose, and are equivalent to those on the H/Z89. Some of these jumpers select power supply voltages, so be careful: A mistake can damage or destroy an EPROM!

JUMPER_JJ504: Configures pin 20 of U518 and U519 (spare ROM and System ROM). JJ504 has two position:

Position 0 connects pin 20 to address line A10.
Position 1 connects pin 20 to ground.

JUMPER_JJ505: Configures pin 21 of U518 and U519 (spare ROM and System ROM). JJ505 has three positions:

Position 0 connects pin 21 to -5 volts.
Position 1 connects pin 21 to +5 volts.
Position 2 connects pin 21 to address line A11.

JUMPER_JJ506: Configures pin 19 of U518 and U519 (spare ROM and System ROM). JJ506 has two positions:

Position 0 connects pin 19 to +12 volts.
Position 1 connects pin 19 to address line A10.

JUMPER_JJ507: Configures the chip select pin (pin 18) of U518 and U519. JJ507 has 3 positions:

Position A selects U519 as a 2nd 2K ROM above U518.
Position B selects U519 as a 2nd 1K ROM below U520.
Position C deselects U519, and selects a 4K ROM at U518.

JUMPER_JJ508: Configures U518 for a 4K or 2K ROM or EPROM:

Position AB is for 2K ROMs.
Position C is for 4K ROMs.

EPROM Jumper Table					
EPROM TYPE	JJ504	JJ505	JJ506	JJ507	JJ508
-----	-----	-----	-----	-----	-----
TMS2716					
Triple-Voltage	0	0	0	A	AB
2716 or 2316					
Single-Voltage	1	1	1	A	AB
2732					
Single-Voltage	1	2	1	C	C

NOTE: Single- and triple-voltage parts may not be mixed. Heath/Zenith part# 444-40 and 444-62 are a 2716 triple-voltage part. Part# 444-142 is a 2732 single-voltage part.

The second type of jumper (JJ509) controls a feature not found on H/289s. It controls the write protect line of the static RAM. Position "1" is the normal position, which gives control of the write-protect line (FMWEN) to the H17 hard-sector disk controller board. Position "0" gives control of the write-protect line to General Purpose Port A, bit 3. In either position, the static RAM memory will be write-protected when the unit is reset (see Chapter 3 for more details).

JUMPER_JJ509: Configures source of FMWEN (Floppy RAM Write Enable):

Position 1 selects control via H17 controller board.
Position 0 selects control by bit 3 of GPA.

6.02 MEMORY UPGRADE

One of the significant advantages of the H-1000 is that it accommodates up to a full megabyte of RAM without additional boards. IC sockets U526-U541 can be populated with either 16 or 32 RAMs, and with either 64K or 256K parts. This gives 4 possible memory sizes: 128K, 256K, 512K, and 1024K. We strongly recommend that memory upgrades be done only by your TMSI dealer or other qualified personnel. However, if you insist on doing it yourself, this section will tell you how.

On a high-performance product like the H-1000, the choice of RAMs is critical. Dynamic RAMs are very complex, and exceedingly difficult to test fully. Use only first-quality parts, purchased from reputable dealers. Demand for these parts is at an all-time high, so it is easy for the unscrupulous to sell substandard "reject" parts at tempting prices. Also, most "hobby" dealers sell their parts untested, so you may need more than you think to get a working set.

RAMs used in the H-1000 must have a worst-case access time from Column Address Strobe $t(CAC)$ = 100 nSec or less. With most brands, this means an "advertised" access time of 150 nSec. Refresh requirements for 64K parts should be 128 rows/2 mSec, or 256 rows/4

mSec. for 256K parts. Based on our testing of RAMs at TMSI, we recommend the following parts (in order of preference). With any others, you're on you own!

64K RAMs (U517 = 101.517.0)	256K RAMs (U517 = 101.517.1)
-----	-----
1. Motorola MCM6665AP15	1. Hitachi HM50256-15Z
2. Motorola MCM6665AP20	2. Motorola MCM6256-15
3. OKI M3764-15RS	3. Toshiba TMM41256-15
4. Intel D2164A-15	
5. Mostek MK4564N-15	
6. Hitachi HM4864-2	

Motorola MCM6664AP RAMs are equivalent to the -6665- parts, but have a special self-refreshing mode that is enabled when pin 1 goes low. The H-1000 has a separate on-board power supply for the RAM and controls pin 1 properly, so this part offers some interesting possibilities for building non-volatile memories.

The address decoder PROM at U517 must be selected to match the kind of RAM used. 64K RAMs require TMSI part #101.517.0 at U517; 256K RAMs require part #101.517.1 at U517. No other changes are necessary.

6.03 MEMORY IC REMOVAL

CAUTION: THE MEMORY IC SOCKETS USED ON THE H-1000 ARE EASILY DAMAGED WHEN REMOVING OR INSERTING ICs. IF YOU BREAK OFF A LOCKING COMB IN THE SOCKET, THE SOCKET WILL HAVE TO BE REPLACED. READ THE FOLLOWING INSTRUCTIONS COMPLETELY BEFORE STARTING. TMSI RECOMMENDS THAT THIS PROCEDURE BE DONE ONLY BY AN AUTHORIZED DEALER OR FACTORY SERVICE PERSONNEL.

1. Remove the locking combs on each side of the socket (see fig. 6-1). This may be done with the IC extraction tool by gripping each end of the locking combs and pulling straight up. Be careful to pull both ends up evenly and not to twist or bend the locking combs.
2. Remove the upper IC (if present). Use the IC extraction tool, and pull the IC straight up.
3. Use a small screwdriver to push the gold contacts of the upper IC into the socket wall and out of the way. Then carefully remove the lower IC with the extraction tool.

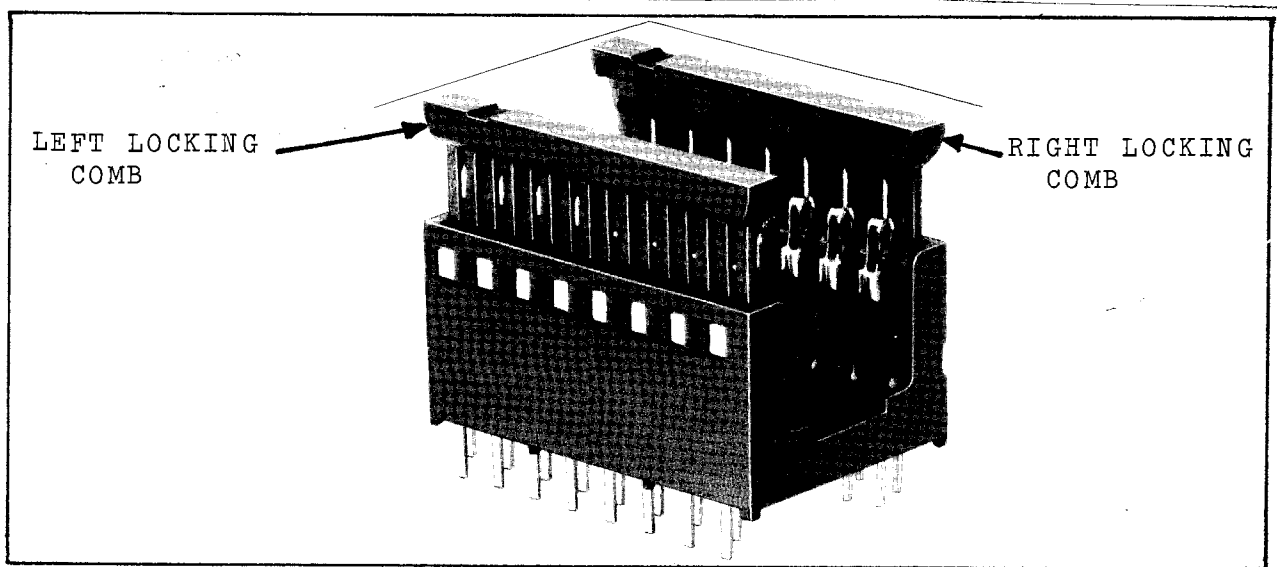


Fig. 6-1 - Memory IC Stacking Socket

6.04 MEMORY IC INSERTION

1. Memory ICs installed on the H-1000 board must have their leads trimmed to a maximum length of 0.125" from the bottom of the package. Failure to do this will cause a short circuit between the top and bottom ICs.
2. Remove the two locking combs from the socket (see fig 6-1). This may be done with the IC extraction tool by gripping each end of the locking combs and pulling straight up. Be careful to pull both ends up evenly and not to twist or bend the locking combs.
3. Bottom IC: Use a small screwdriver and push the gold contacts for the top IC back into the socket wall. Insert the bottom IC with the notch (or pin 1 end) toward the top of the board. Be sure the pins enter the socket and do not bend underneath.
4. Top IC (if used): Look at fig. 6-1, and insert the locking combs just far enough so they push the upper contacts inward. Be sure the "bumpy" side of the locking combs faces inward, and that the polarizing notches are toward the top of the board. Now insert the IC into the upper position with the notch (or pin 1 end) toward the top of the board. Be sure the pins enter the contact boxes.
5. Carefully push the locking combs straight down into the sockets. Be careful not to bend or force them or they may break.

TECHNICAL SPECIFICATIONS

CENTRAL PROCESSING UNIT

```

CPU #1  Type . . . . . Z80-A, 8-bit, 4 MHz
        Clock . . . . . 2.048 or 4.096 MHz, software selectable
        Reset . . . . . Reset upon power-on, keyboard command,
                           or optionally upon CPU swap to Z80.
        Single-step . . . . Optional interrupt after each instruc-
                           tion (H89/Z89 compatible).

```

```

CPU #2  Type . . . . . 8086-2, 16-bit, 8 MHz
        Clock . . . . . 8.192 MHz
        Reset . . . . . Reset upon power-on, keyboard command,
                           or optionally upon CPU swap to 8086.
        Single-step . . . Optional interrupt after each instruc-
                           tion (8086 built-in feature).

```

CPU Select Software selectable. One CPU runs at a time; the other is halted via its BUSRQ/HOLD input.

```
Interrupts . . . . . 8-level priority interrupt controller
                (8080-mode; H89/Z89 compatible).
```

Z80	8086	Source of Interrupt
----	-----	-----
---	vector 0	8086 divide error (highest priority)
---	vector 1	8086 single-step
---	vector 2	8086 NMI (not used)
---	vector 3	8086 breakpoint
---	vector 4	8086 overflow
---	vector 5-31	8086 reserved vectors
NMI	-----	Z80 access to H8 front panel; port F0 or FA (hex), 360 or 372 (octal)
RST 7	vector 255	HDOS and CP/M System Calls
RST 6	vector 247	unused
RST 5	vector 239	I/O boards
RST 4	vector 231	I/O boards
RST 3	vector 223	I/O boards and console
RST 2	vector 215	Z80 single-step
RST 1	vector 207	2 mSec. clock
RST 0	vector 199	Master Reset/Clear (lowest priority)

MEMORY

Organization: Two independent banks of on-board memory (bank 0 and bank 1), plus one memory expansion slot (bank 2). All memory mapped into a 1-megabyte memory space by fusible-link PROMs.

Addressing (Z80 active) . . . Lower 16 bits (A0-A15) supplied by Z80; upper 4 bits (A16-A19) selected via I/O port B. Reads 1 byte at a time.
(8086 active) . . . Supplies A0-A19 directly. Can read either 1 or 2 bytes at a time.

BANK 0: System initialization and boot memory. An 8K block of RAM and ROM/EPROM that can be enabled at address 00000-01FFF (hex) for the Z80, FE000-FFFFFF (hex) for the 8086, or disabled completely. When enabled, Bank 0 has precedence over Banks 1 and 2. Bank 0 is enabled following Reset.

ROM/EPROM three 24-pin sockets (empty), for ROMs from original CPU board.
Type standard 2K or 4K ROMs and EPROMs (2716, 2732, or equivalent). Jumpers for +5vdc or +5/-5/+12vdc parts.
Size 6K bytes maximum
Speed 450 nSec minimum. CPU speed is reduced during access by adding wait states (8086) or reducing clock to 2 MHz (Z80).
Selection via General Purpose Port A, fusible-link PROM U516, and jumpers JJ504-8.

(Z80 active) U518: 00000-007FF (hex) with 2K ROM
 00000-00FFF (hex) with 4K ROM
 U519: 00800-00FFF (hex) 2K or 4K ROM
 U520: 01800-01FFF (hex) 2K only

(8086 active) U518: FE800-FEFFF (hex, even bytes), 2K
 FE800-FF7FF (hex, even bytes), 4K
 U519: FE800-FEFFF (hex, odd bytes), 2K
 FE800-FEFFF (hex, odd bytes), 4K
 U520: FE000-FE7FF (hex, even bytes), 2K

Static RAM 2K bytes static RAM
Type CMOS, uPD444 or equivalent
Speed 450 nSec minimum. CPU speed is reduced during access by adding wait states (8086) or reducing clock to 2 MHz (Z80).
Write Protect software write-protect via General Purpose Port A or H17 disk controller.
Selection via General Purpose Port A and fusible-link PROM U516.

(Z80 active) 01000-017FF (hex)
(8086 active) FF800-FFFFFF (hex)

BANK 1: Main memory, 128K (minimum) to 1 megabyte (maximum) of on-board dynamic RAM.

Type . (standard) . 64K-bit, Motorola MCM6665A or equivalent
 (optional) . 256K-bit, Motorola MCM6256 or equivalent
Speed 150 nSec minimum. No wait states.
Selection Contiguous RAM from 00000 up to:
 1FFFF with 16 64K RAMs (128K)
 3FFFF with 32 64K RAMs (256K)
 7FFFF with 16 256K RAMs (512K)
 FFFFFF with 32 256K RAMs (1024K)
Refresh (Z80) . . . Automatic refresh cycle after each
 instruction fetch. External counter for
 compatibility with 256K RAMs.
 (8086) . . Software refresh via 2 mSec. clock
 interrupt. This interrupt must not be
 disabled for more than 2 mSec unless
 special provisions are made for RAM
 refresh.

BANK 2: Memory expansion connector, located at the leftmost accessory board position. Not compatible with Heath 16K memory expansion board, but accepts memory-mapped I/O boards. This connector provides access to the entire address, data, and control busses for advanced applications.

INPUT/OUTPUT

Organization 1 on-board serial port, 2 parallel ports, and 5 expansion slots. I/O ports set by PROMs U550 and U588.
Selection . . (Z80 active) operation identical to H/Z89
 (8086 active) Even ports accessed with 8-bit I/O instructions. Odd ports accessed with a 16-bit I/O instruction to the next lower (even) port address (example: read port F3 with a 16-bit INPUT instruction from port F2). The desired data will always be in the low byte of the AX register.
Console Serial Port National 8250 (ACE) for communicating with Terminal Logic Board (H19).
Selection port E8-EF (hex), 350-357 (octal)
Compatibility RS-232C compatible. Supports primary handshake lines CTS, RTS, DTR, DSR.
Baud Rates Software programmable; includes all standard rates to 38400 baud.
Character Length . . 5, 6, 7, or 8 bits
Parity Even, Odd, Mark, or none
Stop Bits 1, 1-1/2, or 2

APPENDIX B

RS-232 SERIAL INTERFACE

The RS-232C is perhaps the most commonly-used standard for serial communications. It is used to connect printers, modems, terminals, and other devices to the computer. It is a "loose" standard, which means that different manufacturers choose to implement it in slightly different ways. It is common for two RS-232 devices to "almost" work together. Sometimes they just plug together; other times a considerable amount of experimentation is needed to get them to talk to each other properly. The information in this section will be helpful in sorting out such problems.

The Heath/Zenith H/Z89 series of computers use an H/Z19 Terminal Logic Board to handle the keyboard and display functions. This board communicates with the main computer board via an RS-232 serial link. Handling the computer and keyboard/display functions separately speeds up the system's response time (the computer is free to compute while the terminal handles all keyboard and display functions).

Since it is designed as a drop-in replacement for the H/Z89 CPU board, the H-1000 has retained the same on-board serial port for communicating with the console. Though normally used with a Heath/Zenith H/Z19 terminal, this port will actually work with any standard RS-232 terminal or device. The on-board port is also identical to each of the RS-232 ports on the Heath H-88-3 3-port serial I/O board, commonly used with H/Z89s.

The complete standard is defined as "EIA Standard RS-232C; Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange (1969)" and is available from the Electronic Industries Association, Engineering Department, 2001 Eye St. NW, Washington DC 20006.

RS-232 PINOUTS AND SIGNAL DESCRIPTION

RS232 H/Z89					
PIN	PIN	NAME	DESCRIPTION	SOURCE	TYPE
1	1	GND	protective ground (chassis)	-	ground
2	3	TXD	transmit data from terminal	DTE	data
3	5	RXD	receive data to terminal	DCE	data
4	7	RTS	request to send (terminal on-line)	DTE	control
5	9	CTS	clear to send (response to RTS)	DCE	control
6	11	DSR	data set ready (phone functions)	DCE	control
7	13	GND	signal ground	-	ground
8	15	RLSD	carrier detect (received line signal detector)	DCE	control
20	14	DTR	data terminal ready (terminal on-line)	DTE	control

GENERAL -- RS-232 handles serial binary signals, 0-20,000 baud, synchronous or asynchronous formats, with any character length or code. Heath/Zenith equipment is normally asynchronous format, ASCII code, with 10 bits per character.

DTE vs. DCE -- H/Z19 terminals and printers are defined as DTE (Data Terminal Equipment), and transmit data on pin 2. The H-1000 and Modems are defined as DCE (Data Communication Equipment) and transmit data on pin 3. The Heath 3-port board has one DTE and two DCE ports. To connect like devices (both DTE or DCE), swap 2 and 3, 4 and 5, 6 and 20.

HANDSHAKING -- Signals RTS, CTS, DSR, and DTR are usually required for transmission on TXD; RLSD usually required for reception on RXD. Handshaking requirements vary widely between devices.

ELECTRICAL -- Logic levels defined as positive and negative voltages; positive = +5 to +15 vdc, negative = -5 to -15 vdc. All signals have a common ground, and are protected against short circuits and voltages up to ± 25 vdc.

CONNECTORS -- Miniature "D" connector: male, Cinch DB-25P; female, Cinch DB-25S.

DATA SIGNALS -- Active low.
 negative = 1 = Mark = Idle
 positive = 0 = Space = Break

CONTROL SIGNALS -- Active high.
 positive = 1 = On = True
 negative = 0 = Off = False

APPENDIX C

HEATH/ZENITH MANUALS OF INTEREST

Heath/Zenith computers are "open" systems, and come with perhaps the finest manuals and documentation in the microcomputer field. They are available at negligible cost from Heath, and are required reading if you plan to do any extensive programming with the H-1000. If there is a fault, it is that the sheer magnitude of information makes it difficult to find the manual that can tell you what you need to know. The following list should help you find what you're looking for.

SUBJECT	HEATH #	DESCRIPTION
CP/M-80	595-2775	CP/M-80 rev. 2.203 BIOS source listing
H14		low-cost dot matrix printer manual
H-17-1	595-2716	H17 5-1/4" hard-sector drive controller manual
H-17-1	595-2326	Siemens 5-1/4" disk drive service manual
H-19	595-2284	H19 terminal operation manual
H-19	595-2191	H19 terminal assembly manual
H-19	597-2215	H19 conversion to H88 manual
H-19A	595-2595	H19A terminal operation manual
H-19A	595-2594	H19A terminal assembly manual
H-25	595-2555	H25 high-speed printer operation manual
H-25	595-2454	H25 high-speed printer assembly manual
H-29	595-2992	H29 terminal operation manual
H-29	595-2965	H29 terminal assembly manual
H-47	595-2467	H47 dual 8" disk drive manual
H-77	595-2356	H77 dual 5-1/4" disk drive cabinet manual
H-77A	595-2687	H77A dual 5-1/4" disk drive cabinet manual
H-88	597-2571	H88/H89/Z89/Z90 configuration guide
H-88	595-2268	H88 computer (w/o disk drive) operation manual
H-88	595-2267	H88 computer (w/o disk drive) assembly manual
H-88-1	597-2377	5-1/4" H17 disk controller accessory manual
H-88-3	597-2375	Serial Interface (3-port) accessory manual
H-88-9	595-2722	5-1/4" drive mounting accessory manual
H-89A	595-2766	H89A computer w. H17 disk drive operation manual
H-89A	595-2596	H89A computer w. H17 disk drive assembly manual
MTR-88		MTR-88 monitor ROM manual and source listing
MTR-89	595-2508	MTR-89 monitor ROM manual and source listing
MTR-90	595-2696	MTR-90 monitor ROM manual and source listing
WH-88-16	595-2489	assembled H88 computer manual

SUBJECT	HEATH #	DESCRIPTION
Z-19HW		Zenith Z19 (=H19) terminal manual
Z-19CN		Zenith Z19 low-cost terminal manual
Z-25AA	595-2729	Zenith Z25 (=H25) high-speed printer manual
Z-37	595-2678	Zenith Z37 dual 5-1/4" disk drive cabinet manual
Z-67	595-2675	Zenith Z67 8" Winchester disk drive manual
Z-87	595-2394	Zenith (=H17) 5-1/4" disk drive cabinet manual
Z-89FA	595-2412	Zenith Z89 (=H89) manual
Z-89-37	595-2674	5-1/4" soft-sector controller operation manual
Z-89-37	595-2707	5-1/4" soft-sector controller installation manual
Z-89-67	595-2697	8" Winchester controller installation manual

APPENDIX D

H-1000 PARTS LIST

The following parts list is for an H-1000 with 256K bytes of RAM. Where possible, H-1000 parts use the same key number as their equivalent on the original Heath board, and equivalent Heath part numbers are given. When ordering replacement parts, please identify them as described below.

INTEGRATED CIRCUITS

Key #	TMSI #	Heath #	Qty	Description
U501	74HCU04		1	hex inverter (fast CMOS)
U502	74F161		1	4-bit divider (fast TTL)
U503	4040B	443-760	1	14-stage counter (CMOS)
U504	Z80A		1	4MHz 8-bit CPU
U505,78	74LS164		2	8-bit shift register
U506,55,56,63	74LS74	443-730	4	dual D flip-flop
U507	4528B		1	dual one-shot (CMOS)
U508	74LS132	443-792	1	quad NAND Schmitt trigger
U509,51,85	74LS244	443-791	3	octal Tri-state buffer
U510,11,72,80	74LS373	443-837	4	octal tri-state latch
U512	74HC4040		1	14-stage counter (fast CMOS)
U513,14	74LS257		2	quad data selector
U515,73	74LS02	443-779	2	quad 2-input NOR
U516	101.516		1	TBP28LA22 Bank 0 PROM
U517	101.517		1	TBP28L22 memory PROM
U518		444-142		Heath system ROM
U519				Heath reserved ROM
U520		444-19		Heath disk ROM
U521,58	74LS240	443-754	2	octal tri-state inverter
U522,23,24,25	5114	443-765	4	uPD444C 1Kx4 CMOS static RAM
U526-41(H,L)	4164		32	64K DRAM, Motorola MCM6665A
U542-49,62,67				(unused)
U550		444-61		Heath I/O decoder PROM
U552,84	74LS273	443-805	2	octal latch with reset
U553	74LS32	443-875	1	quad 2-in OR
U554	74LS30	443-732	1	8-in NAND
U557	74LS148	443-912	1	8-bit priority encoder
U559	1488	443-794	1	quad RS-232 driver
U560	1489	443-795	1	quad RS-232 receiver
U561	8250	443-952	1	ACE (Async.Com.Element)
U564,91	74LS04	443-755	2	hex inverter
U565	79M12	442-664	1	-12v regulator
U566	79M05	442-683	1	-5v regulator
U568	LM340T12	442-663	1	+12v regulator
U569	LM340T5	442-54	1	+5v regulator
U570	8086-2		1	8MHz 16-bit CPU
U571,81	74S113		2	dual J-K flip-flop, Schottky
U574,75,76	74LS245	443-885	3	octal bus transceiver
U577	74F11		1	triple AND (fast TTL)
U579	74F521		1	8-bit comparator (fast TTL)
U582	74LS01		1	quad 2-in NAND, OC
U583	74LS158		1	quad data selector
U586	74F10		1	triple NAND (fast TTL)
U587	74LS368		1	hex tri-state inverter
U588	101.588		1	TPB28L22 I/O decoder PROM
U589,90,92	74LS00	443-728	3	quad 2-in NAND

RESISTORS

Key #	TMSI #	Heath #	Qty	Description
-----	-----	-----	---	-----
R501,16	106R5.25	6-105-12	2	1 megohm, 5% 1/4W carbon film
R502,7	471R5.25	6-471-12	2	470 ohm " " " "
R503,4,5,8,10	103R5.25	6-103-12	5	10K ohms " " " "
R506	332R5.25	6-332-12	1	3.3K ohms " " " "
R509,11	105R5.25	6-104-12	2	100K ohms " " " "
R512,13,21-25	102R5.25	6-102-12	7	1K ohms " " " "
R514,17-20				(unused)
R515	152R5.25	6-152-12	1	1.5K ohms " " " "
R526	223R5.25	6-223-12	1	22K ohms " " " "

RESISTOR NETWORKS

Key #	TMSI #	Heath #	Qty	Description
-----	-----	-----	---	-----
RP501-3,6-8				(unused)
RP504	9-R332		1	3.3Kx9 SIP network
RP505	9-R331		1	330x9 SIP network
RP510,12,13	9-R102		3	1Kx9 SIP network
RP509,11	9-R223		2	22Kx9 SIP network

CAPACITORS

Key #	TMSI #	Heath #	Qty	Description
-----	-----	-----	---	-----
C501,22,75	312C220	20-77	3	22 pF, NPO ceramic
C502	312C820		1	82 pF, NPO ceramic
C503,5,9,10, 18-21,25-27	320C391	20-106	12	390 pF, ceramic
C504,24,28-74	322C104		49	0.1 uF, ceramic
C506	362C686	25-282	1	68 uF, 15 VDC tantalum
C507,8,11,14,17	361C225	25-221	5	2.2 uF, 25 VDC tantalum
C512,13,16	361C106		3	10 uF, 25 VDC tantalum
C515	320C221		1	220 pF, ceramic
C523	312C100	21-3	1	10 pF, NPO ceramic

DIODES

Key #	TMSI #	Heath #	Qty	Description
-----	-----	-----	---	-----
D501	1N4148	56-56	1	signal diode, 100mA, 50 PIV
D502,3,5,6	1N4001	57-65	4	diode, 1 amp, 50 PIV
D504				(unused)
D507	MV5753		1	LED, red, T1-3/4

SOCKETS AND CONNECTORS

Key #	TMSI #	Heath #	Qty	Description
H526-41	609-16-1		16	stacking IC socket, T.B. Ansley
H557	IC16.3		1	16-pin IC socket
H522, 23, 24, 25	IC18.3		4	18-pin IC socket
H516, 17, 50, 58, 88	IC20.3		5	20-pin IC socket
H518, 19, 20	IC24.6		3	24-pin IC socket
H504, 61, 70	IC40.6		3	40-pin IC socket
P501	P2X10.1		1	2x10 header, .025" x .1 x .1"
P502-506	P10.1		5	10-pin header, .025" x .1"
P507	P2X25.1		1	2x25 header, .025" x .1 x .1"
P508-512	P25.1		5	25-pin header, .025" x .1"
P513	P15.1		1	15-pin header, .025" x .1"
P514	P10.156		1	10-pin header, .045" x .156"
P515	P11.156		1	11-pin header, .045" x .156"
P516	P4.156		1	4-pin header, .045" x .156"
JJ504, 6, 8, 9	P3.1		4	3-pin header, .025" x .1"
JJ505	P3X1.1		1	4-pin header, .025" x .1"
JJ507	P4.1		1	4-pin header, .025" x .1"

MISCELLANEOUS

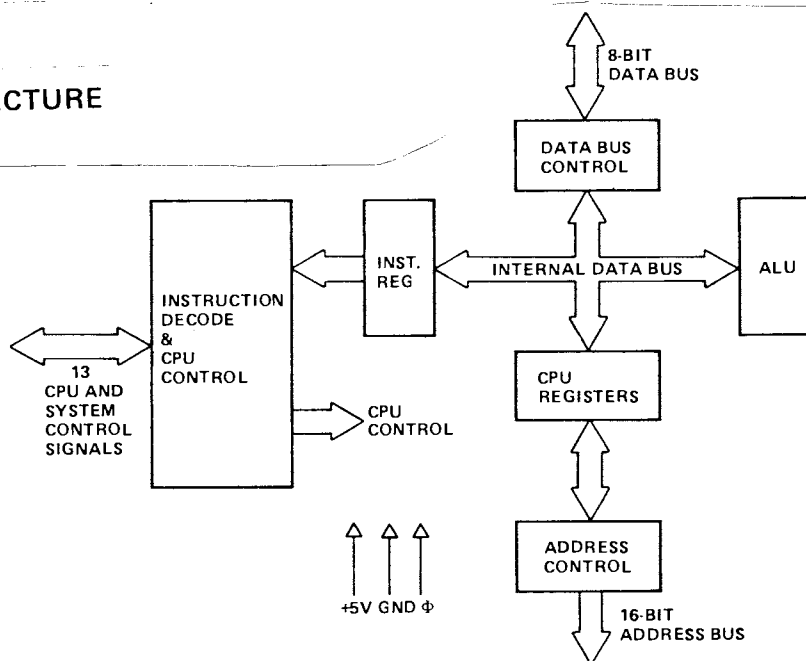
Key #	TMSI #	Heath #	Qty	Description
L501-4	57-3425		4	ferrite bead
SW501	206.8	60-621	1	8-section DIP switch
X501	104.005		1	24.576 MHz crystal
X502	104.003	404-608	1	1.8432 MHz crystal
-	200.103		1	printed circuit board
-	204.001		1	heatsink
-	F1-10-106		2	threaded inserts, Southco Inc
-	210.600	250-89	3	#6-32 x 3/8 RH screw
-	212.600	254-1	3	#6 lockwasher
-	211.600	252-3	3	#6-32 hex nut
-	219.001		7	1/8" "pop" rivet
-	4880		1	T0-220 transistor mtg. kit
-			6"	#24 uninsulated wire
-		352-31	1	thermal grease (U568, U569)
-	209.100		6	programming jumper
-	208.002		1	I/O mounting bracket assy

APPENDIX E

DATA SHEETS

Z80 Data Sheet	E-2
8086 Data Sheet	E-10
8250 ACE Data Sheet	E-34
64K RAM Data Sheet (Motorola MCM6665)	E-50
256K RAM Data Sheet (Motorola MCM6256)	E-66
TTL Logic Data Sheets	E-78
16-Pin Stacking Socket Data Sheet	E-82

2.0 Z-80 CPU ARCHITECTURE



Z-80 CPU BLOCK DIAGRAM
FIGURE 2.0-1

2.1 CPU REGISTERS

The Z-80 CPU contains 208 bits of R/W memory that are accessible to the programmer. Figure 2.0-2 illustrates how this memory is configured into eighteen 8-bit registers and four 16-bit registers. All Z-80 registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulator and flag registers.

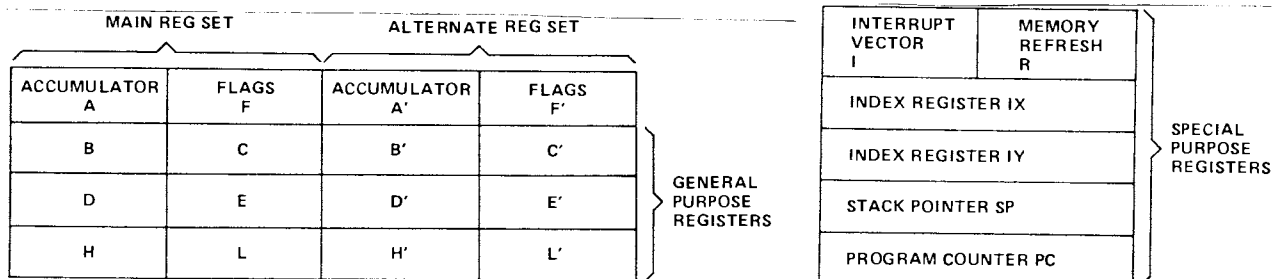
Special Purpose Registers

1. **Program Counter (PC).** The program counter holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transferred to the address lines. When a program jump occurs the new value is automatically placed in the PC, overriding the incrementer.
2. **Stack Pointer (SP).** The stack pointer holds the 16-bit address of the current top of a stack located anywhere in external system RAM memory. The external stack memory is organized as a last-in first-out (LIFO) file. Data can be pushed onto the stack from specific CPU registers or popped off of the stack into specific CPU registers through the execution of **PUSH** and **POP** instructions. The data popped from the stack is always the last data pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data manipulation.
3. **Two Index Registers (IX & IY).** The two independent index registers hold a 16-bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer. This mode of addressing greatly simplifies many types of programs, especially where tables of data are used.
4. **Interrupt Page Address Register (I).** The Z-80 CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I Register is used for this purpose to store the high order 8-bits of the indirect address while the interrupting device provides the lower 8-bits of the address. This feature allows interrupt routines to be dynamically located anywhere in memory with absolute minimal access time to the routine.

5. **Memory Refresh Register (R).** The Z-80 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. Seven bits of this 8 bit register are automatically incremented after each instruction fetch. The eighth bit will remain as programmed as the result of an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the I register are placed on the upper 8 bits of the address bus.

Accumulator and Flag Registers

The CPU includes two independent 8-bit accumulators and associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16-bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair that he wishes to work with with a single exchange instruction so that he may easily work with either pair.



General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange commands need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

2.2 ARITHMETIC & LOGIC UNIT (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

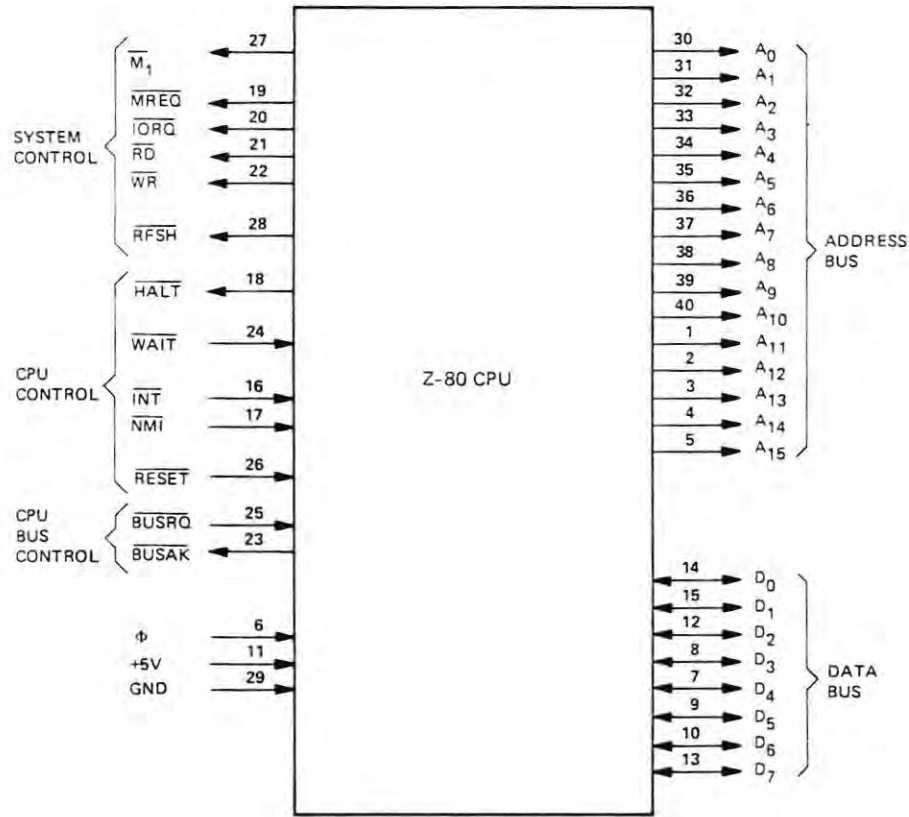
Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset bit
Compare	Test bit

2.3 INSTRUCTION REGISTER AND CPU CONTROL

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

3.0 Z-80 CPU PIN DESCRIPTION

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in figure 3.0-1 and the function of each is described below.



Z-80 PIN CONFIGURATION
FIGURE 3.0-1

A₀-A₁₅
(Address Bus)

Tri-state output, active high. A₀-A₁₅ constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A₀ is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D₀-D₇
(Data Bus)

Tri-state input/output, active high. D₀-D₇ constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

\overline{M}_1
(Machine Cycle one)

Output, active low. \overline{M}_1 indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, \overline{M}_1 is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. \overline{M}_1 also occurs with \overline{IORQ} to indicate an interrupt acknowledge cycle.

\overline{MREQ}
(Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{\text{IORQ}}$
(Input/Output Request)

Tri-state output, active low. The $\overline{\text{IORQ}}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{\text{IORQ}}$ signal is also generated with an $\overline{\text{M1}}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.

$\overline{\text{RD}}$
(Memory Read)

Tri-state output, active low. $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{\text{WR}}$
(Memory Write)

Tri-state output, active low. $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{\text{RFSH}}$
(Refresh)

Output, active low. $\overline{\text{RFSH}}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{\text{MREQ}}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{\text{HALT}}$
(Halt state)

Output, active low. $\overline{\text{HALT}}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{\text{WAIT}}$
(Wait)

Input, active low. $\overline{\text{WAIT}}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{\text{INT}}$
(Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{\text{BUSRQ}}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{\text{IORQ}}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

$\overline{\text{NMI}}$
(Non Maskable Interrupt)

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{\text{NMI}}$ automatically forces the Z-80 CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous $\overline{\text{WAIT}}$ cycles can prevent the current instruction from ending, and that a $\overline{\text{BUSRQ}}$ will override a $\overline{\text{NMI}}$.

RESET

Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

- 1) Disable the interrupt enable flip-flop
- 2) Set Register I = 00_H
- 3) Set Register R = 00_H
- 4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.

BUSRQ

(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK

(Bus Acknowledge)

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Φ

Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

Absolute Maximum Ratings

Temperature Under Bias
Storage Temperature
Voltage On Any Pin
with Respect to Ground
Power Dissipation

Specified operating range,
-65°C to +150°C
-0.3V to +7V
1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{CC} .

$$I_{CC} = 200 \text{ mA}$$

Z80-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - 0.6$		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.8 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0 \text{ to } V_{CC}$
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	$V_{OUT} = 2.4 \text{ to } V_{CC}$
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	$V_{OUT} = 0.4 \text{ V}$
I_{LD}	Data Bus Leakage Current in Input Mode			± 10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C - Ceramic
P - Plastic
S - Standard $5V \pm 5\%$ 0° to 70°C
E - Extended $5V \pm 5\%$ -40° to 85°C
M - Military $5V \pm 10\%$ -55° to 125°C

Z80A-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - 0.6$		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.8 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0 \text{ to } V_{CC}$
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	$V_{OUT} = 2.4 \text{ to } V_{CC}$
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	$V_{OUT} = 0.4 \text{ V}$
I_{LD}	Data Bus Leakage Current in Input Mode			± 10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C - Ceramic
P - Plastic
S - Standard $5V \pm 5\%$ 0° to 70°C

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5V \pm 5\%$, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	110	[1]	nsec	
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	110	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_D(AD)$	Address Output Delay		110	nsec	$C_L = 50\text{pF}$
	$t_F(AD)$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to \overline{MREQ} (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to \overline{IORQ} , \overline{RD} or \overline{WR} (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable From \overline{RD} , \overline{WR} , \overline{IORQ} or \overline{MREQ}	[3]		nsec	
	t_{caf}	Address Stable From \overline{RD} or \overline{WR} During Float	[4]		nsec	
D_{0-7}	$t_D(D)$	Data Output Delay		150	nsec	$C_L = 50\text{pF}$
	$t_F(D)$	Delay to Float During Write Cycle		90	nsec	
	$t_{SD}(D)$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{SD}(D)$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to \overline{WR} (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to \overline{WR} (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From \overline{WR}	[7]		nsec	
	t_H	Any Hold Time for Setup Time		0	nsec	
\overline{MREQ}	$t_{DL\Phi}(\overline{MR})$	\overline{MREQ} Delay From Falling Edge of Clock, \overline{MREQ} Low		85	nsec	$C_L = 50\text{pF}$
	$t_{DH\Phi}(\overline{MR})$	\overline{MREQ} Delay From Rising Edge of Clock, \overline{MREQ} High		85	nsec	
	$t_{w}(\overline{MRL})$	\overline{MREQ} Delay From Falling Edge of Clock, \overline{MREQ} High	[8]		nsec	
	$t_{w}(\overline{MRH})$	Pulse Width, \overline{MREQ} Low	[9]		nsec	
	$t_{w}(\overline{MRH})$	Pulse Width, \overline{MREQ} High			nsec	
\overline{IORQ}	$t_{DL\Phi}(\overline{IR})$	\overline{IORQ} Delay From Rising Edge of Clock, \overline{IORQ} Low		75	nsec	$C_L = 50\text{pF}$
	$t_{DL\Phi}(\overline{IR})$	\overline{IORQ} Delay From Falling Edge of Clock, \overline{IORQ} Low		85	nsec	
	$t_{DH\Phi}(\overline{IR})$	\overline{IORQ} Delay From Rising Edge of Clock, \overline{IORQ} High		85	nsec	
	$t_{DH\Phi}(\overline{IR})$	\overline{IORQ} Delay From Falling Edge of Clock, \overline{IORQ} High		85	nsec	
	$t_{w}(\overline{IRL})$	Pulse Width, \overline{IORQ} Low			nsec	
\overline{RD}	$t_{DL\Phi}(\overline{RD})$	\overline{RD} Delay From Rising Edge of Clock, \overline{RD} Low		85	nsec	$C_L = 50\text{pF}$
	$t_{DL\Phi}(\overline{RD})$	\overline{RD} Delay From Falling Edge of Clock, \overline{RD} Low		95	nsec	
	$t_{DH\Phi}(\overline{RD})$	\overline{RD} Delay From Rising Edge of Clock, \overline{RD} High		85	nsec	
	$t_{DH\Phi}(\overline{RD})$	\overline{RD} Delay From Falling Edge of Clock, \overline{RD} High		85	nsec	
	$t_{w}(\overline{RDL})$	Pulse Width, \overline{RD} Low			nsec	
\overline{WR}	$t_{DL\Phi}(\overline{WR})$	\overline{WR} Delay From Rising Edge of Clock, \overline{WR} Low		65	nsec	$C_L = 50\text{pF}$
	$t_{DL\Phi}(\overline{WR})$	\overline{WR} Delay From Falling Edge of Clock, \overline{WR} Low		80	nsec	
	$t_{DH\Phi}(\overline{WR})$	\overline{WR} Delay From Rising Edge of Clock, \overline{WR} High		80	nsec	
	$t_{w}(\overline{WRL})$	Pulse Width, \overline{WR} Low	[10]		nsec	
	$t_{w}(\overline{WRH})$	Pulse Width, \overline{WR} High			nsec	
$\overline{M1}$	$t_{DL}(\overline{M1})$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	$C_L = 50\text{pF}$
	$t_{DH}(\overline{M1})$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
\overline{RFSH}	$t_{DL}(\overline{RF})$	\overline{RFSH} Delay From Rising Edge of Clock, \overline{RFSH} Low		130	nsec	$C_L = 50\text{pF}$
	$t_{DH}(\overline{RF})$	\overline{RFSH} Delay From Rising Edge of Clock, \overline{RFSH} High		120	nsec	
\overline{WAIT}	$t_s(WT)$	\overline{WAIT} Setup Time to Falling Edge of Clock	70		nsec	
\overline{HALT}	$t_D(HT)$	\overline{HALT} Delay Time From Falling Edge of Clock		300	nsec	$C_L = 50\text{pF}$
\overline{INT}	$t_s(IT)$	\overline{INT} Setup Time to Rising Edge of Clock	80		nsec	
\overline{NMI}	$t_w(NML)$	Pulse Width, \overline{NMI} Low	80		nsec	
\overline{BUSRQ}	$t_s(BQ)$	\overline{BUSRQ} Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSA\overline{K}}$	$t_{DL}(\overline{BA})$	$\overline{BUSA\overline{K}}$ Delay From Rising Edge of Clock, $\overline{BUSA\overline{K}}$ Low		100	nsec	$C_L = 50\text{pF}$
	$t_{DH}(\overline{BA})$	$\overline{BUSA\overline{K}}$ Delay From Falling Edge of Clock, $\overline{BUSA\overline{K}}$ High		100	nsec	
\overline{RESET}	$t_s(RS)$	\overline{RESET} Setup Time to Rising Edge of Clock	60		nsec	
	$t_F(C)$	Delay to Float (\overline{MREQ} , \overline{IORQ} , \overline{RD} and \overline{WR})		80	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to \overline{IORQ} (Interrupt Ack.)	[11]		nsec	

$$[12] \quad t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$$

$$[1] \quad t_{acm} = t_w(\Phi H) + t_f - 65$$

$$[2] \quad t_{aci} = t_c - 70$$

$$[3] \quad t_{ca} = t_w(\Phi L) + t_f - 50$$

$$[4] \quad t_{caf} = t_w(\Phi L) + t_f - 45$$

$$[5] \quad t_{dcm} = t_c - 170$$

$$[6] \quad t_{dci} = t_w(\Phi L) + t_f - 170$$

$$[7] \quad t_{cdf} = t_w(\Phi L) + t_f - 70$$

$$[8] \quad t_w(\overline{MRL}) = t_c - 30$$

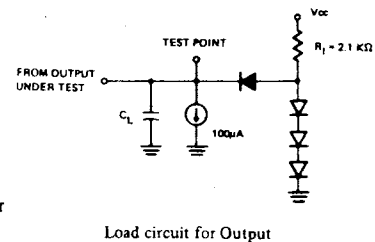
$$[9] \quad t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 20$$

$$[10] \quad t_w(\overline{WRL}) = t_c - 30$$

$$[11] \quad t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$$

NOTES:

- Data should be enabled onto the CPU data bus when \overline{RD} is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and \overline{IORQ} are both active.
- All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- The \overline{RESET} signal must be active for a minimum of 3 clock cycles.
- Output Delay vs. Loaded Capacitance
 $T_A = 70^\circ\text{C}$ $V_{CC} = +5V \pm 5\%$
 Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.
- Although static by design, testing guarantees $t_w(\Phi H)$ of 200 μsec maximum





iAPX 86/10 16-BIT HMOS MICROPROCESSOR

8086/8086-2/8086-1

- Direct Addressing Capability to 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages.
- 14 Word, by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide
- Range of Clock Rates:
5 MHz for 8086,
8 MHz for 8086-2,
10 MHz for 8086-1
- MULTIBUS™ System Compatible Interface

The Intel iAPX 86/10 high performance 16-bit CPU is available in three clock rates: 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The iAPX 86/10 operates in both single processor and multiple processor configurations to achieve high performance levels.

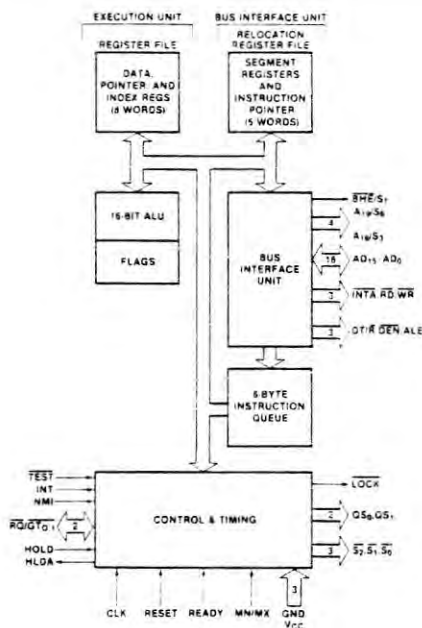


Figure 1. iAPX 86/10 CPU Block Diagram

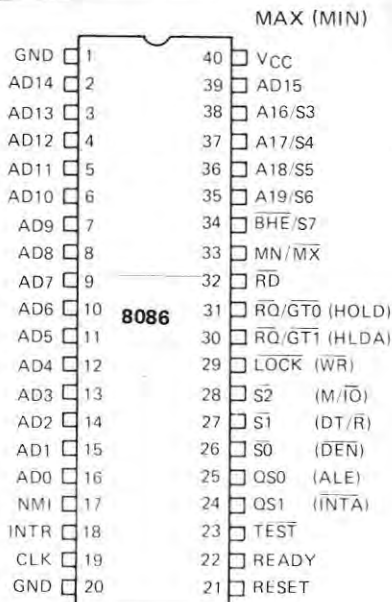


Figure 2. iAPX 86/10 Pin Configuration

(8086 data supplied courtesy of Intel Corporation)

Table 1. Pin Description

The following pin function descriptions are for IAPX 86 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function																		
AD ₁₅ -AD ₀	2-16, 39	I/O	Address Data Bus: These lines constitute the time multiplexed memory/I/O address (T ₁) and data (T ₂ , T ₃ , T _W , T ₄) bus. A ₀ is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins D ₇ -D ₀ . It is LOW during T ₁ when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A ₀ to condition chip select functions. (See $\overline{\text{BHE}}$.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge."																		
A ₁₉ /S ₆ , A ₁₈ /S ₅ , A ₁₇ /S ₄ , A ₁₆ /S ₃	35-38	O	Address/Status: During T ₁ these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T ₂ , T ₃ , T _W , and T ₄ . The status of the interrupt enable FLAG bit (S ₆) is updated at the beginning of each CLK cycle. A ₁₇ /S ₄ and A ₁₆ /S ₃ are encoded as shown. This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge."																		
			<table><tr><th>A₁₇/S₄</th><th>A₁₆/S₃</th><th>Characteristics</th></tr><tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr><tr><td>0</td><td>1</td><td>Stack</td></tr><tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr><tr><td>1</td><td>1</td><td>Data</td></tr><tr><td colspan="2">S₆ is 0 (LOW)</td><td></td></tr></table>	A ₁₇ /S ₄	A ₁₆ /S ₃	Characteristics	0 (LOW)	0	Alternate Data	0	1	Stack	1 (HIGH)	0	Code or None	1	1	Data	S ₆ is 0 (LOW)		
A ₁₇ /S ₄	A ₁₆ /S ₃	Characteristics																			
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1 (HIGH)	0	Code or None																			
1	1	Data																			
S ₆ is 0 (LOW)																					
$\overline{\text{BHE}}$ /S ₇	34	O	Bus High Enable/Status: During T ₁ the bus high enable signal ($\overline{\text{BHE}}$) should be used to enable data onto the most significant half of the data bus, pins D ₁₅ -D ₈ . Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{\text{BHE}}$ to condition chip select functions. $\overline{\text{BHE}}$ is LOW during T ₁ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S ₇ status information is available during T ₂ , T ₃ , and T ₄ . The signal is active LOW, and floats to 3-state OFF in "hold." It is LOW during T ₁ for the first interrupt acknowledge cycle.																		
			<table><tr><th>$\overline{\text{BHE}}$</th><th>A₀</th><th>Characteristics</th></tr><tr><td>0</td><td>0</td><td>Whole word</td></tr><tr><td>0</td><td>1</td><td>Upper byte from/to odd address</td></tr><tr><td>1</td><td>0</td><td>Lower byte from/to even address</td></tr><tr><td>1</td><td>1</td><td>None</td></tr></table>	$\overline{\text{BHE}}$	A ₀	Characteristics	0	0	Whole word	0	1	Upper byte from/to odd address	1	0	Lower byte from/to even address	1	1	None			
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1	0	Lower byte from/to even address																			
1	1	None																			
$\overline{\text{RD}}$	32	O	Read: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S ₂ pin. This signal is used to read devices which reside on the 8086 local bus. $\overline{\text{RD}}$ is active LOW during T ₂ , T ₃ and T _W of any read cycle, and is guaranteed to remain HIGH in T ₂ until the 8086 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge."																		
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/I/O is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.																		
INTR	18	I	Interrupt Request: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.																		
TEST	23	I	TEST: input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.																		

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
			If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
LOCK	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge."
QS ₁ , QS ₀	24, 25	O	Queue Status: The queue status is valid during the CLK cycle after which the queue operation is performed. QS ₁ and QS ₀ provide status to allow external tracking of the internal 8086 instruction queue.

The following pin function descriptions are for the 8086 in minimum mode (i.e., $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

M/\overline{IO}	28	O	Status line: logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/\overline{IO} becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle ($M = \text{HIGH}$, $IO = \text{LOW}$). M/\overline{IO} floats to 3-state OFF in local bus "hold acknowledge."
\overline{WR}	29	O	Write: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/\overline{IO} signal. \overline{WR} is active for T_2 , T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge."
\overline{INTA}	24	O	\overline{INTA} is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2 , T_3 and T_W of each interrupt acknowledge cycle.
ALE	25	O	Address Latch Enable: provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
DT/\overline{R}	27	O	Data Transmit/Receive: needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/\overline{R} is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/\overline{IO} . ($T = \text{HIGH}$, $R = \text{LOW}$.) This signal floats to 3-state OFF in local bus "hold acknowledge."
\overline{DEN}	26	O	Data Enable: provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. \overline{DEN} is active LOW during each memory and I/O access and for \overline{INTA} cycles. For a read or \overline{INTA} cycle it is active from the middle of T_2 until the middle of T_4 , while for a write cycle it is active from the beginning of T_2 until the middle of T_4 . \overline{DEN} floats to 3-state OFF in local bus "hold acknowledge."
HOLD, HLDA	31, 30	I/O	HOLD: indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWER HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{RQ}/\overline{IGT}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
NMI	17	I	Non-maskable interrupt: an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	Reset: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	Clock: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V _{CC}	40		V _{CC} : +5V power supply pin.
GND	1, 20		Ground
MN/ \overline{MX}	33	I	Minimum/Maximum: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., $MN/\overline{MX} = V_{SS}$). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

$\overline{S_2}, \overline{S_1}, \overline{S_0}$	26-28	O	<p>Status: active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.</p> <p>These signals float to 3-state OFF in "hold acknowledge." These status lines are encoded as shown.</p> <table border="1"> <thead> <tr> <th>$\overline{S_2}$</th><th>$\overline{S_1}$</th><th>$\overline{S_0}$</th><th>Characteristics</th></tr> </thead> <tbody> <tr> <td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>Acknowledge</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>Read I/O Port</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>Write I/O Port</td></tr> <tr> <td>1 (HIGH)</td><td>0</td><td>0</td><td>Half</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Code Access</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Read Memory</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Write Memory</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Passive</td></tr> </tbody> </table>	$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics	0 (LOW)	0	0	Interrupt	0	0	1	Acknowledge	0	1	0	Read I/O Port	0	1	1	Write I/O Port	1 (HIGH)	0	0	Half	1	0	1	Code Access	1	1	0	Read Memory	1	1	1	Write Memory	1	1	1	Passive
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$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$	30, 31	I/O	<p>Request/Grant: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 9):</p> <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 8086 (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the "hold" request is about to end and that the 8086 can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. 																																								

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal functions of the iAPX 86/10 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank (D₁₅-D₈) and a low bank (D₇-D₀) of 512K 8-bit bytes addressed in parallel by the processor's address lines

A₁₉ - A₁. Byte data with even addresses is transferred on the D₇-D₀ bus lines while odd addressed byte data (A₀ HIGH) is transferred on the D₁₅-D₈ bus lines. The processor provides two enable signals, BHE and A₀, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

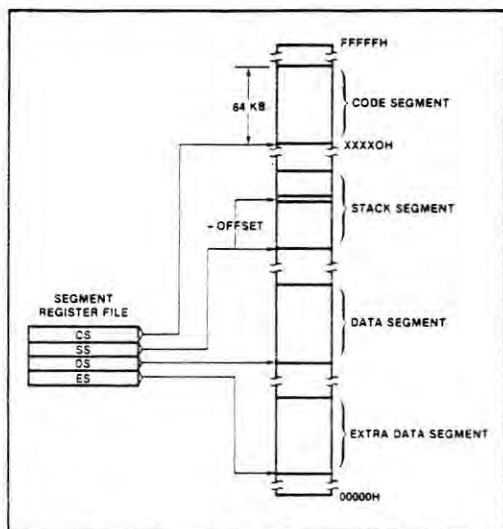


Figure 3a. Memory Organization

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 3b.) Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element

consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

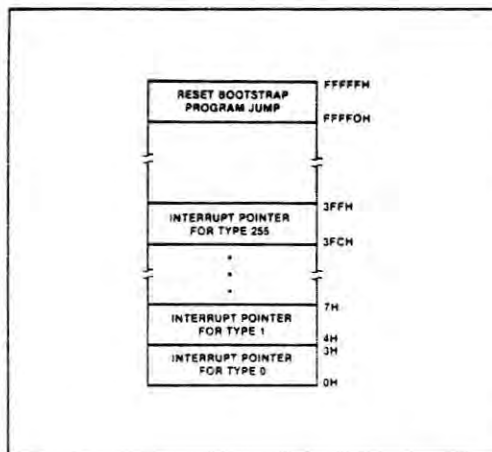


Figure 3b. Reserved Memory Locations

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum IAPX 86/10 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/MX pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into $\overline{S_0}, \overline{S_1}, \overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS™ architecture. When the MN/MX pin is strapped to V_{CC}, the 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

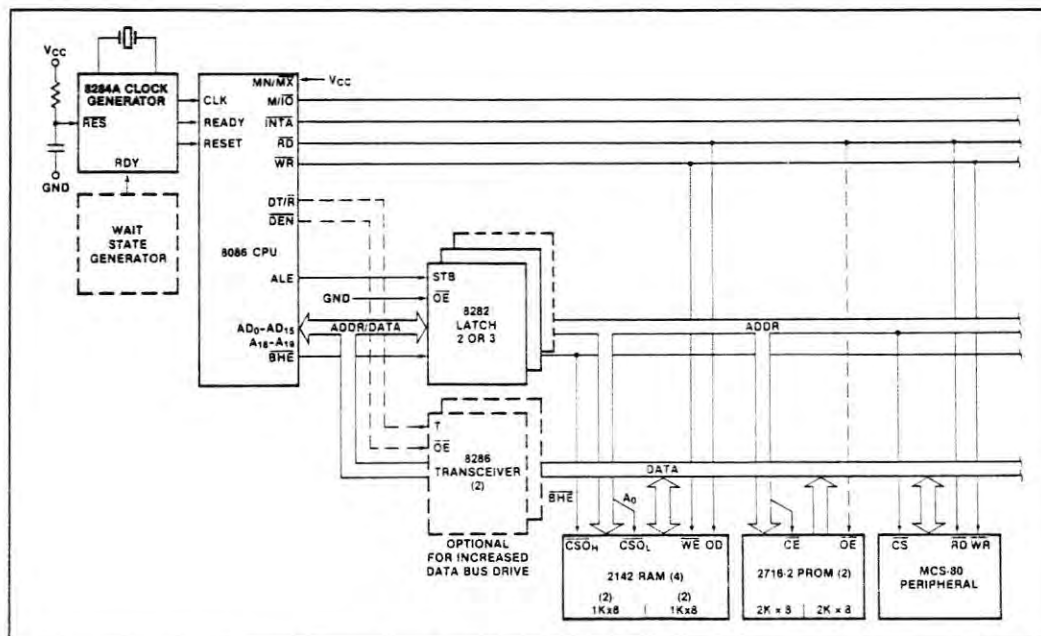


Figure 4a. Minimum Mode iAPX 86/10 Typical Configuration

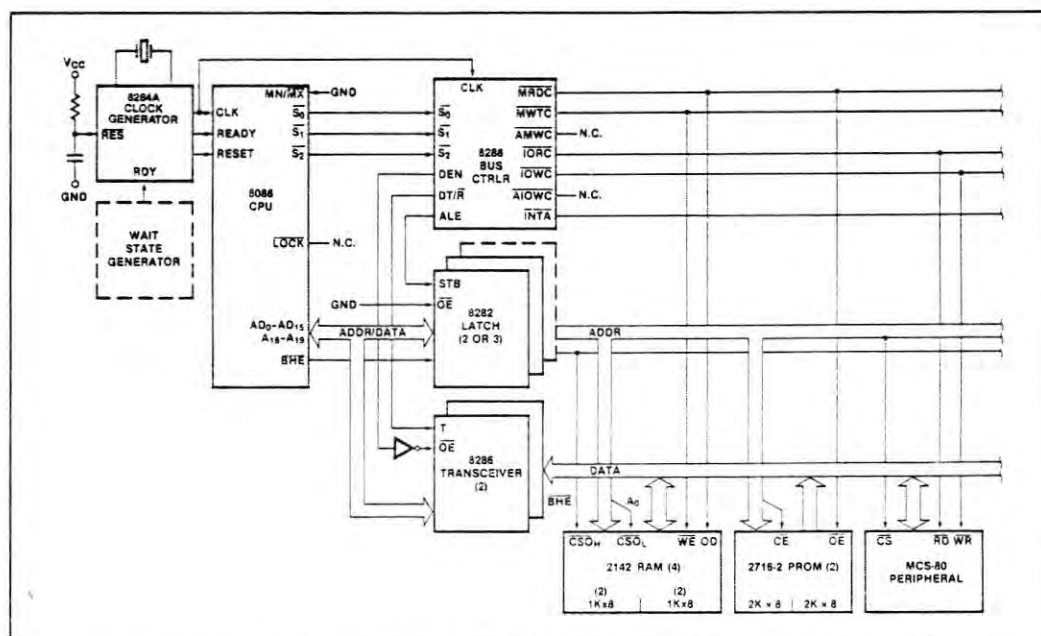


Figure 4b. Maximum Mode iAPX 86/10 Typical Configuration

BUS OPERATION

The 86/10 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1 , T_2 , T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4 . T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T_3 and T_4 . Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between 8086 bus cycles. These are referred to as "Idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/\overline{MX} strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_7 are multiplexed with high-order address bits and the \overline{BHE} signal, and are therefore valid during T_2 through T_4 . S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. $S_6=0$ and S_7 is a spare status bit.

I/O ADDRESSING

In the 86/10, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines $A_{15}-A_0$. The address lines $A_{19}-A_{16}$ are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on $D_{15}-D_8$. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The 8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3B). The details of this operation are specified in the Instruction Set description of the MCS-86 Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μ s after power-up, to allow complete initialization of the 8086.

NMI may not be asserted prior to the 2nd CLK cycle following the end of RESET.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge

sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 86/10 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the

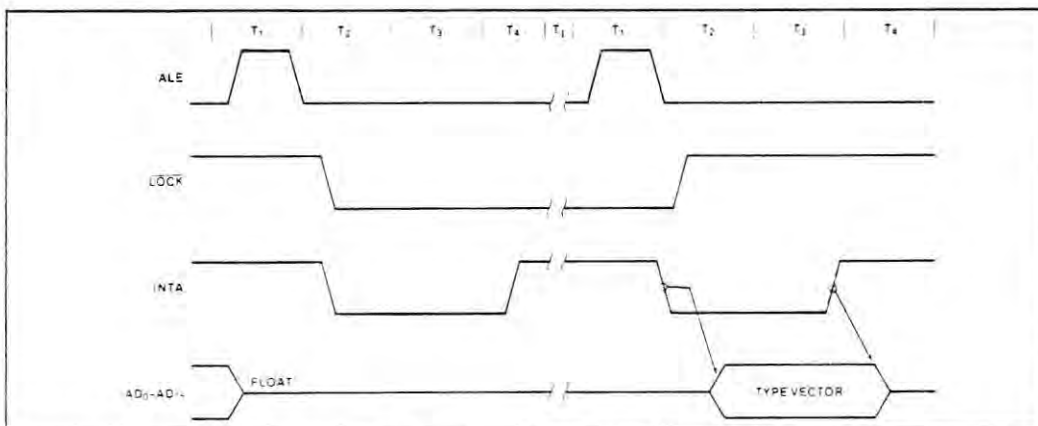


Figure 6. Interrupt Acknowledge Sequence

FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (figure 6) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 8086 emits the LOCK signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In Maximum Mode, the processor issues appropriate HALT status on $\overline{S_2}, \overline{S_1}, \overline{S_0}$ and the 8288 bus controller issues one ALE. The 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 8086 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The LOCK status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multi-processor system configurations to accomplish "test and set lock" operations. The LOCK signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While LOCK is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 8086 provides a single software-testable input known as the TEST signal. At any time the program may execute a WAIT instruction. If at that time the TEST signal is inactive (HIGH), program execution becomes suspended while the processor waits for TEST

to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 8086 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

BASIC SYSTEM TIMING

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/MX pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/MX pin is strapped to V_{SS} and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 5 illustrates the signal timing relationships.

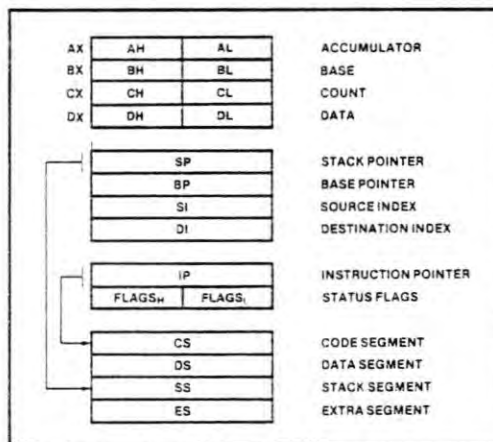


Figure 7. iAPX 86/10 Register Model

SYSTEM TIMING — MINIMUM SYSTEM

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the 8282/8283 latch. The \overline{BHE} and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/\overline{IO} signal indicates a memory or I/O operation. At T_2 the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2 . The read (\overline{RD}) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal

to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (8286/8287) is required to buffer the 8086 local bus, signals $\overline{DT/\overline{R}}$ and \overline{DEN} are provided by the 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The $\overline{M/\overline{IO}}$ signal is again asserted to indicate a memory or I/O write operation. In the T_2 immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4 . During T_2 , T_3 , and T_4 the processor asserts the write control signal. The write (\overline{WR}) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

The \overline{BHE} and A_0 signals are used to select the proper byte(s) of the memory/I/O word to be read or written according to the following table:

\overline{BHE}	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on $D_{15}-D_8$.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal (\overline{INTA}) is asserted in place of the

read (\overline{RD}) signal and the address bus is floated. (See Figure 6.) In the second of two successive \overline{INTA} cycles, a byte of information is read from bus lines D_7-D_0 as supplied by the interrupt system logic (i.e., 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

BUS TIMING—MEDIUM SIZE SYSTEMS

For medium size systems the $\overline{MN/\overline{MX}}$ pin is connected to V_{SS} and the 8288 Bus Controller is added to the system as well as an 8282/8283 latch for latching the system address, and a 8286/8287 transceiver to allow for bus loading greater than the 8086 is capable of handling. Signals ALE, \overline{DEN} , and $\overline{DT/\overline{R}}$ are generated by the 8288 instead of the processor in this configuration although their timing remains relatively the same. The 8086 status outputs ($\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$) provide type-of-cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The 8286/8287 transceiver receives the usual \overline{T} and \overline{OE} inputs from the 8288's $\overline{DT/\overline{R}}$ and \overline{DEN} .

The pointer into the interrupt vector table, which is passed during the second \overline{INTA} cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the 8286/8287 transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

**ABSOLUTE MAXIMUM RATINGS***

Ambient Temperature Under Bias 0°C to 70°C
Storage Temperature - 65°C to + 150°C
Voltage on Any Pin with
Respect to Ground - 1.0 to + 7V
Power Dissipation 2.5 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (8086: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)
(8086-1: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)
(8086-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	- 0.5	+ 0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.5\text{ mA}$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = - 400\text{ }\mu\text{A}$
I_{CC}	Power Supply Current: 8086 8086-1 8086-2		340 360 350	mA	$T_A = 25^\circ\text{C}$
I_{LI}	Input Leakage Current		± 10	μA	$0\text{V} \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		± 10	μA	$0.45\text{V} \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	- 0.5	+ 0.6	V	
V_{CH}	Clock Input High Voltage	3.9	$V_{CC} + 1.0$	V	
C_{IN}	Capacitance of Input Buffer (All input except $AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	$f_c = 1\text{ MHz}$
C_{IO}	Capacitance of I/O Buffer ($AD_0 - AD_{15}$, $\overline{RQ}/\overline{GT}$)		15	pF	$f_c = 1\text{ MHz}$



A.C. CHARACTERISTICS (8086: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)
(8086-1: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)
(8086-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

**MINIMUM COMPLEXITY SYSTEM
TIMING REQUIREMENTS**

Symbol	Parameter	8086		8086-1 (Preliminary)		8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	100	500	125	500	ns	
TCLCH	CLK Low Time	$(\frac{3}{4} \text{ TCLCL}) - 15$		$(\frac{3}{4} \text{ TCLCL}) - 14$		$(\frac{3}{4} \text{ TCLCL}) - 15$		ns	
TCHCL	CLK High Time	$(\frac{1}{4} \text{ TCLCL}) + 2$		$(\frac{1}{4} \text{ TCLCL}) + 6$		$(\frac{1}{4} \text{ TCLCL}) + 2$		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		5		20		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into 8086	$(\frac{3}{4} \text{ TCLCL}) - 15$		53		$(\frac{3}{4} \text{ TCLCL}) - 15$		ns	
TCHRYX	READY Hold Time into 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		-10		-8		ns	
THVCH	HOLD Setup Time	35		20		20		ns	
TINVCH	INTR, NMI, TEST Setup Time (See Note 2)	30		15		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIMIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

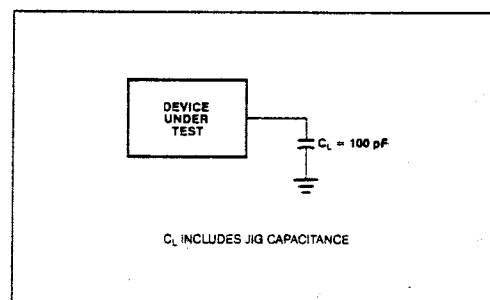
**A.C. CHARACTERISTICS (Continued)****TIMING RESPONSES**

Symbol	Parameter	8086		8086-1 (Preliminary)		8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	50	10	60	ns	*C _L = 20-100 pF for all 8086 Out- puts (In addi- tion to 8086 self- load)
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	10	40	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH-20		TCLCH-10		TCLCH-10		ns	
TCLLH	ALE Active Delay		80		40		50	ns	
TCHLL	ALE Inactive Delay		85		45		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	10	50	10	60	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		TCLCH-25		TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	10	50	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	45	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	50	10	70	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLRL	\overline{RD} Active Delay	10	165	10	70	10	100	ns	
TCLRH	\overline{RD} Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	\overline{RD} Inactive to Next Address Active	TCLCL-45		TCLCL-35		TCLCL-40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	60	10	100	ns	
TRLRH	\overline{RD} Width	2TCLCL-75		2TCLCL-40		2TCLCL-50		ns	
TWLWH	\overline{WR} Width	2TCLCL-60		2TCLCL-35		2TCLCL-40		ns	
TAVAl	Address Valid to ALE Low	TCLCH-80		TCLCH-35		TCLCH-40		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

NOTES:

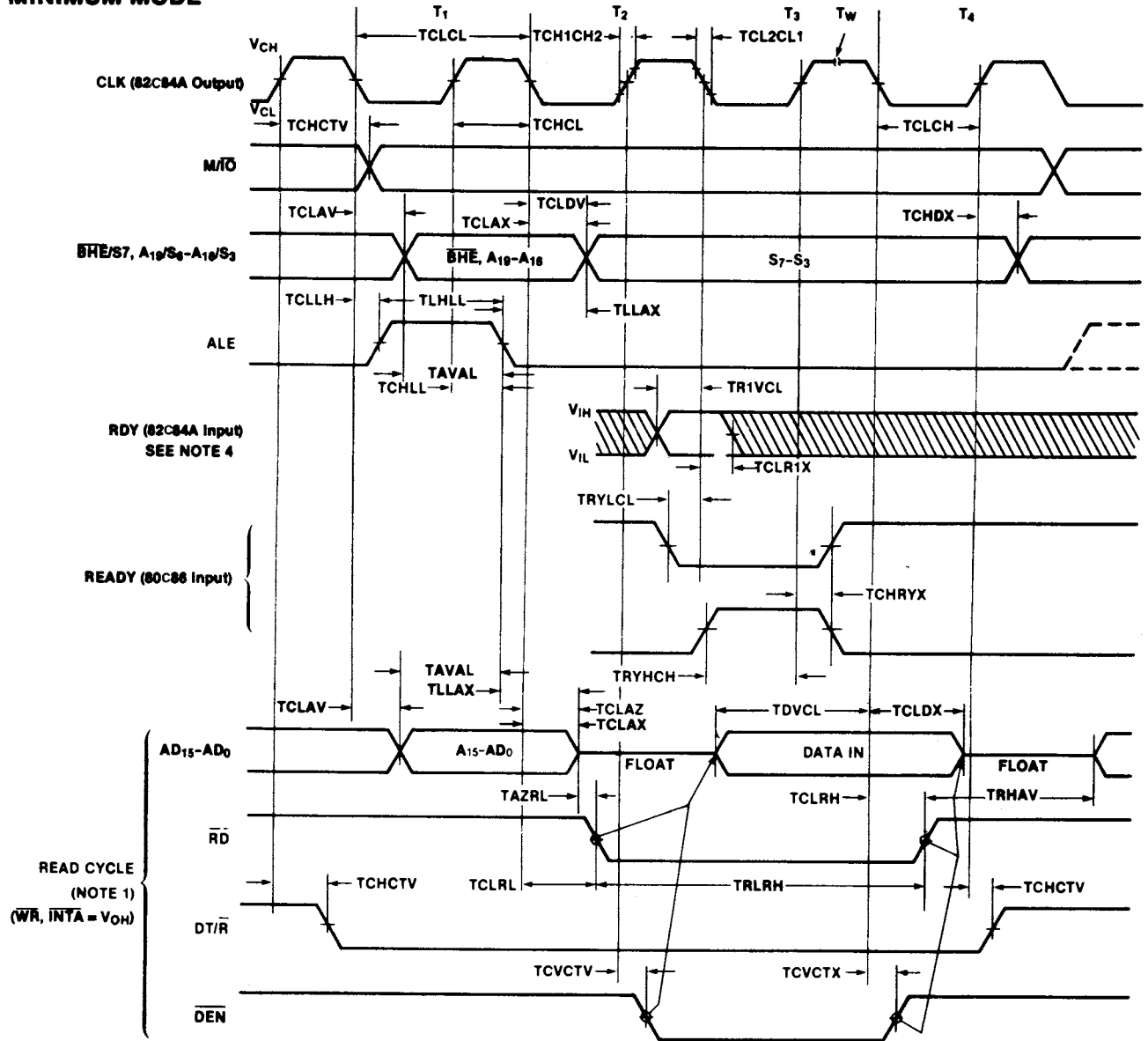
1. Signal at 8284A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3).

A.C. TESTING LOAD CIRCUIT

[illegible]

Waveforms

MINIMUM MODE





A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER)
TIMING REQUIREMENTS

Symbol	Parameter	8086		8086-1 (Preliminary)		8086-2 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	100	500	125	500	ns	
TCLCH	CLK Low Time	$(\frac{1}{2} \text{ TCLCL}) - 15$		$(\frac{1}{2} \text{ TCLCL}) - 14$		$(\frac{1}{2} \text{ TCLCL}) - 15$		ns	
TCHCL	CLK High Time	$(\frac{1}{2} \text{ TCLCL}) + 2$		$(\frac{1}{2} \text{ TCLCL}) + 8$		$(\frac{1}{2} \text{ TCLCL}) + 2$		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		5		20		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into 8086	$(\frac{1}{2} \text{ TCLCL}) - 15$		53		$(\frac{1}{2} \text{ TCLCL}) - 15$		ns	
TCHRYX	READY Hold Time into 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	-8		-10		-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		15		15		ns	
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ Setup Time	30		12		15		ns	
TCHGX	$\overline{\text{RQ}}$ Hold Time into 8086	40		20		30		ns	
TIHIL	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

NOTES:

- Signal at 8284A or 8288 shown for reference only.
- Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- Applies only to T3 and wait states.
- Applies only to T2 state (8 ns into T3).



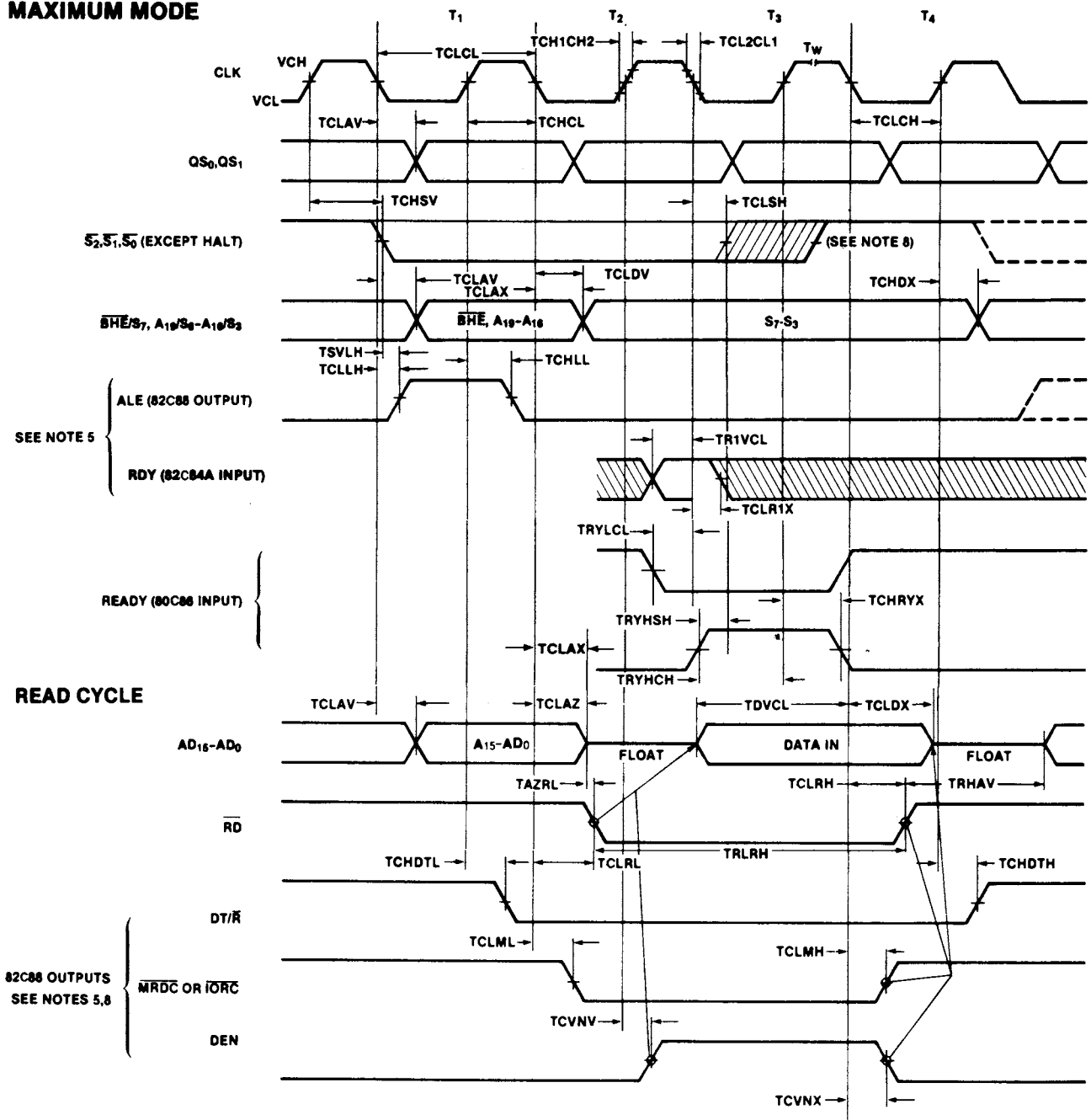
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8086		8086-1 (Preliminary)		8086-2 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	10	35	ns	C _L = 20-100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		45		65	ns	
TCHSV	Status Active Delay	10	110	10	45	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	55	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	50	10	60	ns	
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	10	40	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	50	10	60	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		0		ns	
TCLRL	RD Active Delay	10	165	10	70	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL - 45		TCLCL - 35		TCLCL - 40		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30		30	ns	
TCLGL	GT Active Delay	0	85	0	45	0	50	ns	
TCLGH	GT Inactive Delay	0	85	0	45	0	50	ns	
TRLRH	RD Width	2TCLCL - 75		2TCLCL - 40		2TCLCL - 50		ns	
TOLOH	Output Rise Time		20		20		20	ns	
TOHOL	Output Fall Time		12		12		12	ns	

Waveforms

MAXIMUM MODE



MAXIMUM MODE (Continued)

WRITE CYCLE

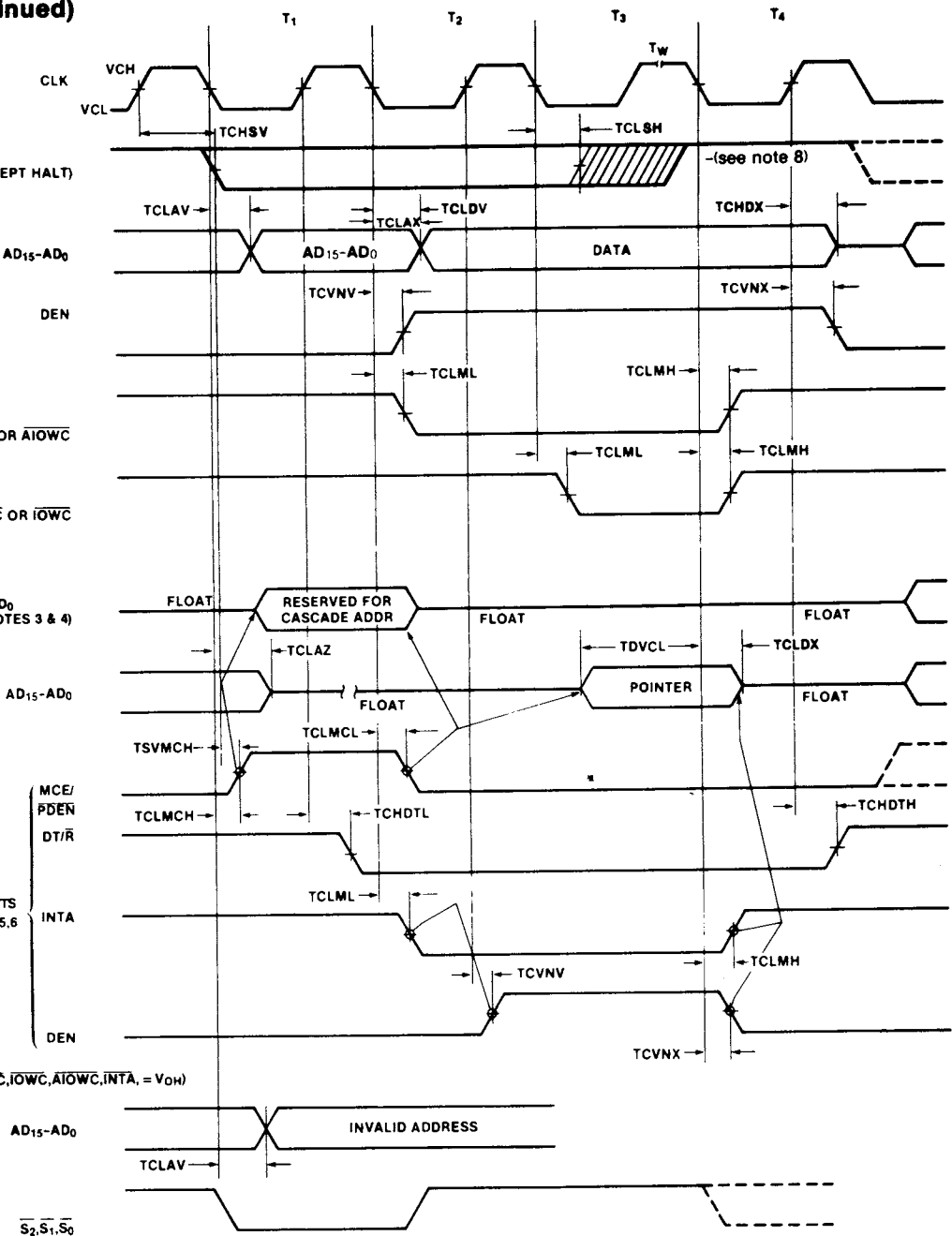
82C88 OUTPUTS
SEE NOTES 5, 6

INTA CYCLE

AD₁₅-AD₀
(SEE NOTES 3 & 4)

82C88 OUTPUTS
SEE NOTES 5, 6

SOFTWARE HALT —
(DEN = V_{OL}; RD, MRDC, IORC, MWTC, AMWC, IOWC, AIOWC, INTA = V_{OH})

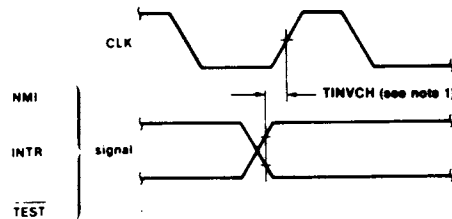


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T₂, T₃, T₄ to determine if T_{WS} machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T₄.

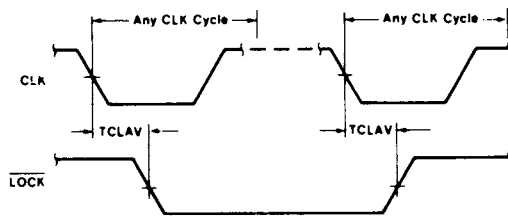
Waveforms (continued)

ASYNCHRONOUS SIGNAL RECOGNITION

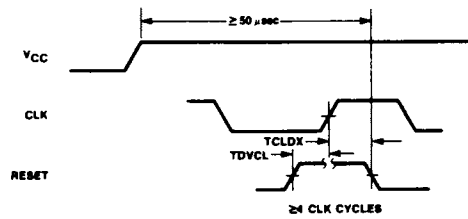


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

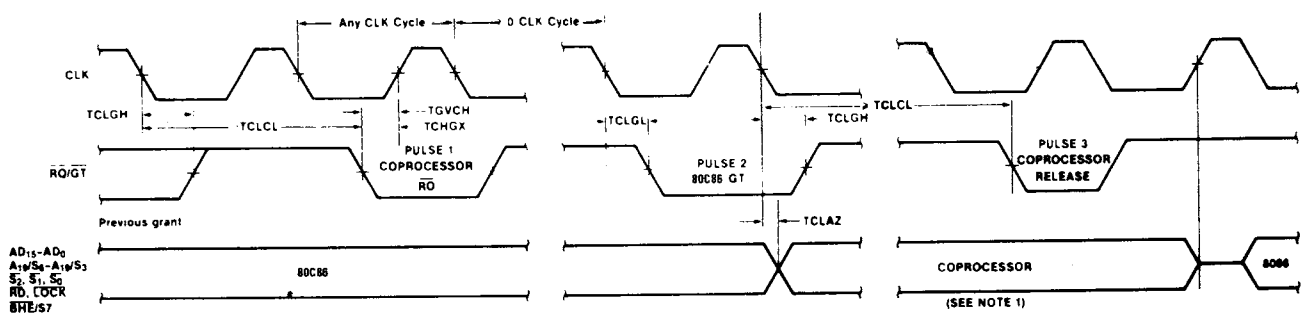
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING

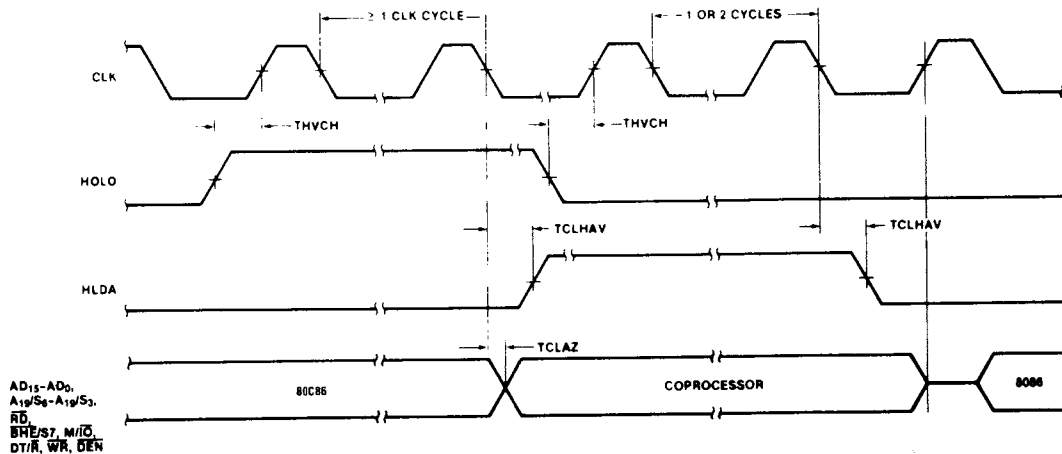


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTES: 1. THE COPROCESSOR MAY NOT DRIVE THE BUSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



Instruction Set Summary

DATA TRANSFER

MOV - Move:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to register	1 0 1 1 w reg	data	data if w 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr low	addr high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr low	addr high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		

PUSH - Push:

Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m
Register	0 1 0 1 0 reg	
Segment register	0 0 0 reg 1 1 0	

POP - Pop:

Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m
Register	0 1 0 1 1	reg
Segment register	0 0 0	reg 1 1 1

XCHG - Exchange:

Register/memory with register	1 0 0 0 0 1 1 w	mod	reg	r/m
Register with accumulator	1 0 0 1 0 reg			

IN - Input from:

Fixed port	1 1 1 0 0 1 0 w	port
Variable port	1 1 1 0 1 1 0 w	

OUT - Output to:

Fixed port	1 1 1 0 0 1 1 w	port
Variable port	1 1 1 0 1 1 1 w	

XLAT - Translate byte to AL

LEA - Load EA to register	1 1 0 1 0 1 1 1
---------------------------	-----------------

LDS - Load pointer to DS	1 0 0 0 1 1 0 1	mod reg r/m
--------------------------	-----------------	-------------

LES - Load pointer to ES	1 1 0 0 0 1 0 1	mod reg r/m
--------------------------	-----------------	-------------

LAHF - Load AH with flags	1 0 0 1 1 1 1 1
---------------------------	-----------------

SAHF - Store AH into flags	1 0 0 1 1 1 1 0
----------------------------	-----------------

PUSHF - Push flags	1 0 0 1 1 1 0 0
--------------------	-----------------

POPF - Pop flags	1 0 0 1 1 1 0 1
------------------	-----------------

ARITHMETIC

ADD - Add:

Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w 1	

ADC - Add with carry:

Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	

INC - Increment:

Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m
Register	0 1 0 0 0 reg	

AAA - ASCII adjust for add	0 0 1 1 0 1 1 1
DAA - Decimal adjust for add	0 0 1 0 0 1 1 1

SUB - Subtract:

Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	

SBB - Subtract with borrow

Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	

DEC - Decrement:

Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m
Register	0 1 0 0 1 reg	
NEG Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m

CMP - Compare:

Register/memory and register	0 0 1 1 1 0	d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0	s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0	w		data	data if w 1
AAS ASCII adjust for subtract	0 0 1 1 1 1 1 1				
DAS Decimal adjust for subtract	0 0 1 0 1 1 1 1				
MUL Multiply (unsigned)	1 1 1 1 0 1 1	w	mod 1 0 0 r/m		
IMUL Integer multiply (signed)	1 1 1 1 0 1 1	w	mod 1 0 1 r/m		
AAM ASCII adjust for multiply	1 1 0 1 0 1 0 0		0 0 0 0 1 0 1 0		
DIV Divide (unsigned)	1 1 1 1 0 1 1	w	mod 1 1 0 r/m		
IDIV Integer divide (signed)	1 1 1 1 0 1 1	w	mod 1 1 1 r/m		
AAD ASCII adjust for divide	1 1 0 1 0 1 0 1		0 0 0 0 1 0 1 0		
CBW Convert byte to word	1 0 0 1 1 0 0 0				
CWD Convert word to double word	1 0 0 1 1 0 0 1				

LOGIC

NOT - Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m
SHL/SAL - Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m
SHR - Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m
SAR - Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m
ROL - Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m
ROR - Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m
RCL - Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m
RCR - Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m

AND - And:

Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 1 0 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	

TEST - And function to flags, no result:

Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	

OR - Or:

Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	

XOR - Exclusive or:

Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 1 1 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w 1	

STRING MANIPULATION

REP - Repeat	1 1 1 1 0 0 1 2
MOVS - Move byte/word	1 0 1 0 0 1 0 w
CMPS - Compare byte/word	1 0 1 0 0 1 1 w
SCAS - Scan byte/word	1 0 1 0 1 1 1 w
LODS - Load byte/word to AL/AX	1 0 1 0 1 1 0 w
STOS - Store byte/word from AL/AX	1 0 1 0 1 0 1 w

Instruction Set Summary (continued)

CONTROL TRANSFER

CALL = Call:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0	r/m
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1	r/m

JMP = Unconditional Jump:

Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0	r/m
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1	r/m

RET = Return from CALL:

Within segment	1 1 0 0 0 1 1 1		
Within seg adding immed to SP	1 1 0 0 0 1 0 1	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ-Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE-Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG-Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE-Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA-Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE-Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO-Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS-Jump on sign	0 1 1 1 0 0 0 0	disp	
JNE/JNZ-Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE-Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG-Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

JNB/JAE-Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA-Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO-Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO-Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS-Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP-Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE-Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE-Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ-Jump on CX zero	1 1 1 0 0 0 1 1	disp

INT Interrupt

Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INT0 Interrupt on overflow	1 1 0 0 1 1 1 0	
INRET Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLO Clear direction	1 1 1 1 1 1 0 0	
STO Set direction	1 1 1 1 1 1 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 1 0 1 1	
HLT Halt	1 1 1 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
 AX = 16-bit accumulator
 CX = Count register
 DS = Data segment
 ES = Extra segment
 Above/below refers to unsigned value.
 Greater = more positive;
 Less = less positive (more negative) signed values
 if d = 1 then "to" reg; if d = 0 then "from" reg
 if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
 if mod = 00 then DISP = 0*, disp-low and disp-high are absent
 if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
 if mod = 10 then DISP = disp-high: disp-low
 if r/m = 000 then EA = (BX) + (SI) + DISP
 if r/m = 001 then EA = (BX) + (DI) + DISP
 if r/m = 010 then EA = (BP) + (SI) - DISP
 if r/m = 011 then EA = (BP) + (DI) - DISP
 if r/m = 100 then EA = (SI) + DISP
 if r/m = 101 then EA = (DI) + DISP
 if r/m = 110 then EA = (BP) + DISP*
 if r/m = 111 then EA = (BX) + DISP
 DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
 if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
 if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
 x = don't care
 z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

INS8250A Asynchronous Communications Element

General Description

The INS8250A is the enhanced version of the programmable Asynchronous Communications Element (ACE) chip—the 8250. It provides an on-board programmable baud generator, and is contained in a standard 40-pin dual-in-line package. The new ACE is fabricated using National Semiconductor's advanced, scaled N-channel silicon-gate MOS process, XMOS. It functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250A is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

The INS8250A performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250A at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250A, as well as any error conditions (parity, overrun, framing, or break interrupt).

The INS8250A includes a programmable baud generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a $16 \times$ clock for driving the internal transmitter logic. Provisions are also included to use this $16 \times$ clock to drive the receiver logic. Also included in the INS8250A is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

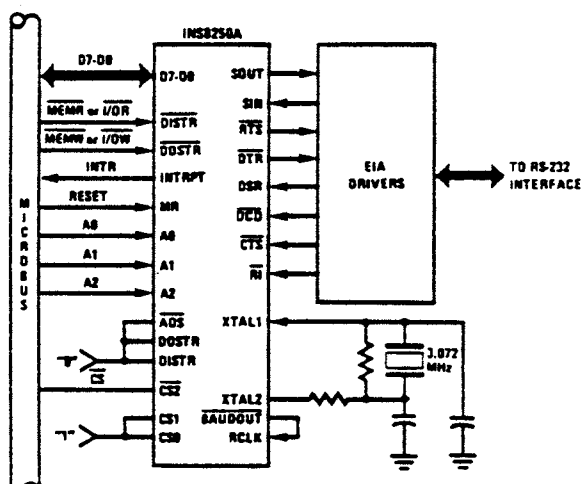
Features

- Easily interfaces to most popular microprocessors.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.

- Full double buffering eliminates need for precise synchronization.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to $(2^{16} - 1)$ and generates the internal $16 \times$ clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
 - 5-, 6-, 7-, or 8-bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1-, 1½-, or 2-stop bit generation
 - Baud generation (DC to 56k baud).
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
- Line break generation and detection.
- Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation
 - Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.
- Microbus™ compatible.

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Microbus™ is a trademark of National Semiconductor Corp.

Microbus Configuration



Courtesy of National
Semiconductor Corporation.

Absolute Maximum Ratings

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	-0.5V to +7.0V
Power Dissipation	400mW

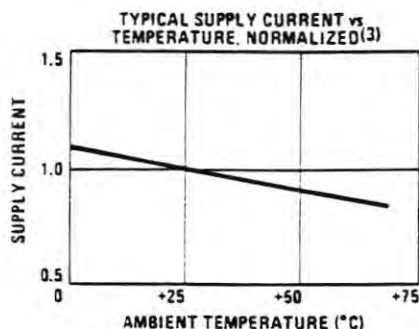
Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

DC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ILX}	Clock Input Low Voltage	$I_{OL} = 1.6\text{mA}$ on all outputs; $I_{OH} = -100\mu\text{A}$	-0.5		0.8	V
V_{IHx}	Clock Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})			65	80	mA
I_{IL}	Input Leakage				± 10	μA
I_{CL}	Clock Leakage				± 10	μA
V_{ILMR}	MR Schmitt V_{IL}				0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0			V
V_{HMR}	MR Schmitt Hysteresis		0.2			V

Capacitance $T_A = 25^\circ\text{C}$, $V_{CC} = V_{SS} = 0\text{V}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{XIN}	Clock Input Capacitance	$f_c = 1\text{MHz}$ Unmeasured pins returned to V_{SS}		15	20	pF
C_{XOUT}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF



AC Electrical Characteristics $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$.

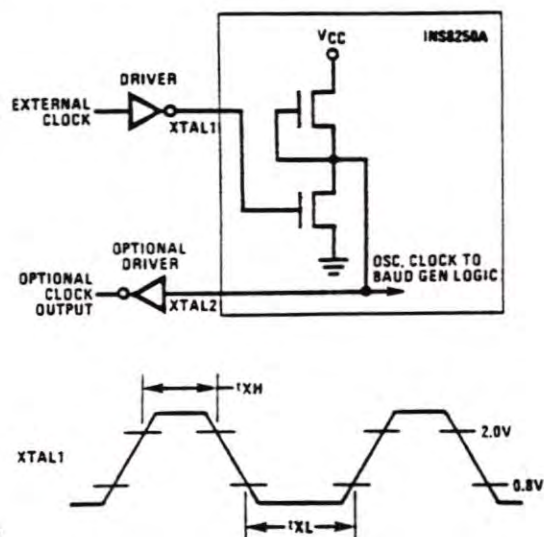
Symbol	Parameter	Conditions	Min.	Max.	Units
t_{AW}	Address Strobe Width		90		ns
t_{AS}	Address Setup Time		110		ns
t_{AH}	Address Hold Time		0		ns
t_{CS}	Chip Select Setup Time		110		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{DID}	$\overline{DISTR}/DISTR$ Strobe Delay		0		ns
t_{DIW}	$\overline{DISTR}/DISTR$ Strobe Width		175		ns
t_{RC}	Read Cycle Delay		1735		ns
RC	Read Cycle = $t_{AW} + t_{DID} + t_{DIW} + t_{RC}$		2000		ns
t_{DD}	$\overline{DISTR}/DISTR$ to Driver Disable Delay	- @100pF loading		150	ns
t_{DDO}	Delay from $\overline{DISTR}/DISTR$ to Data	- @100pF loading		250	ns
t_{HZ}	$\overline{DISTR}/DISTR$ to Floating Data Delay	- @100pF loading	100		ns
t_{DOD}	$\overline{DOSTR}/DOSTR$ Strobe Delay		50		ns
t_{DOW}	$\overline{DOSTR}/DOSTR$ Strobe Width		175		ns
t_{WC}	Write Cycle Delay		1785		ns
WC	Write Cycle = $t_{AW} + t_{DOD} + t_{DOW} + t_{WC}$		2100		ns
t_{DS}	Data Setup Time		175		ns
t_{DH}	Data Hold Time		60		ns
t_{CSC}^*	Chip Select Output Delay from Select	- @100pF loading		200	ns
t_{RA}^*	Address Hold Time from $\overline{DISTR}/DISTR$		50		ns
t_{RCS}^*	Chip Select Hold Time from $\overline{DISTR}/DISTR$		50		ns
t_{AR}^*	$\overline{DISTR}/DISTR$ Delay from Address		110		ns
t_{CSR}^*	$\overline{DISTR}/DISTR$ Delay from Chip Select		110		ns
t_{WA}^*	Address Hold Time from $\overline{DOSTR}/DOSTR$		50		ns
t_{WCS}^*	Chip Select Hold Time from $\overline{DOSTR}/DOSTR$		50		ns
t_{AW}^*	$\overline{DOSTR}/DOSTR$ Delay from Address		160		ns
t_{CSW}^*	$\overline{DOSTR}/DOSTR$ Delay from Select		160		ns
t_{MRW}	Master Reset Pulse Width		25		μs

* Applicable only when \overline{ADS} input is tied permanently low.

AC Electrical Characteristics (Continued)

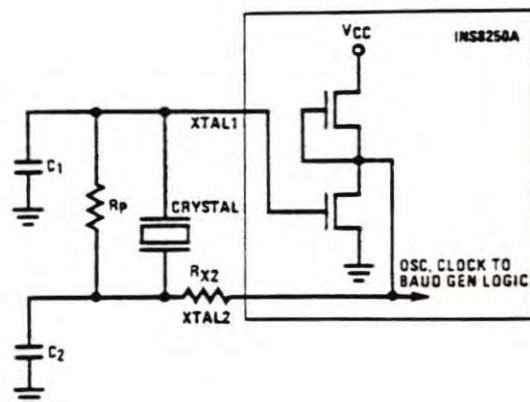
Symbol	Parameter	Conditions	Min.	Max.	Units
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t _{BLD}	Baud Output Negative Edge Delay	100pF Load		250 typ.	ns
t _{BHD}	Baud Output Positive Edge Delay	100pF Load		250 typ.	ns
t _{LW}	Baud Output Down Time	100pF Load	425 typ.		ns
t _{HW}	Baud Output Up Time	100pF Load	330 typ.		ns
Receiver					
t _{SCD}	Delay from RCLK to Sample Time			2 typ.	μs
t _{SINT}	Delay from Stop to Set Interrupt	100pF Load		2 typ.	μs
t _{RINT}	Delay from $\overline{\text{DISTR}}$ /DISTR (RD RBR/RDLSR) to Reset Interrupt	100pF Load		1 typ.	μs
Transmitter					
t _{HR}	Delay from $\overline{\text{DOSTR}}$ /DOSTR (WR THR) to Reset Interrupt	100pF Load		1 typ.	μs
t _{IRS}	Delay from Initial INTR Reset to Transmit Start			16 typ.	BAUDOUT Cycles
t _{SI}	Delay from Initial Write to Interrupt			24 typ.	BAUDOUT Cycles
t _{STI}	Delay from Stop to Interrupt (THRE)			8 typ.	BAUDOUT Cycles
t _{IR}	Delay from $\overline{\text{DISTR}}$ /DISTR (RD IIR) to Reset Interrupt (THRE)	100pF Load		1 typ.	μs
Modem Control					
t _{MOO}	Delay from DOSTR/ $\overline{\text{DOSTR}}$ (WR MCR) to Output	100pF Load		1 typ.	μs
t _{SIM}	Delay to Set Interrupt from MODEM Input	100pF Load		1 typ.	μs
t _{RIM}	Delay to Reset Interrupt from $\overline{\text{DISTR}}$ /DISTR (RD MSR)	100pF Load		1 typ.	μs

Typical Clock Circuits



Timing	Min	Units
t_{XH}	140	ns
t_{XL}	140	ns

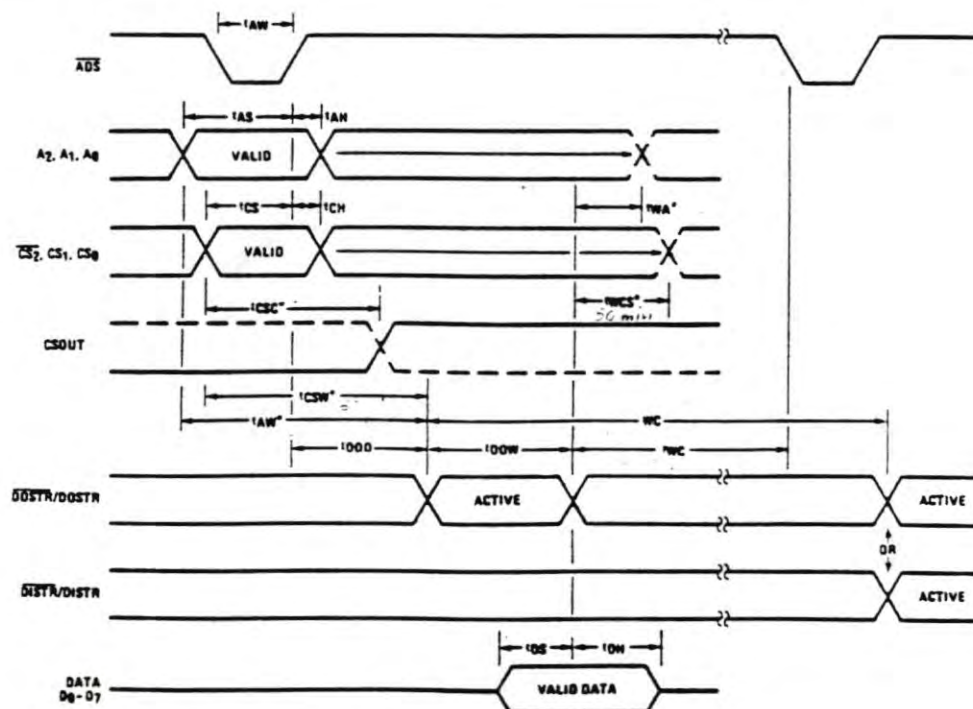
A. External Clock Input (3.1 MHz Max.)



CRYSTAL	Rp	Rx2	C1	C2
3.1 MHz	1 MΩ	1.5K	10 - 30 pF	40 - 60 pF

B. Typical Crystal Oscillator Network

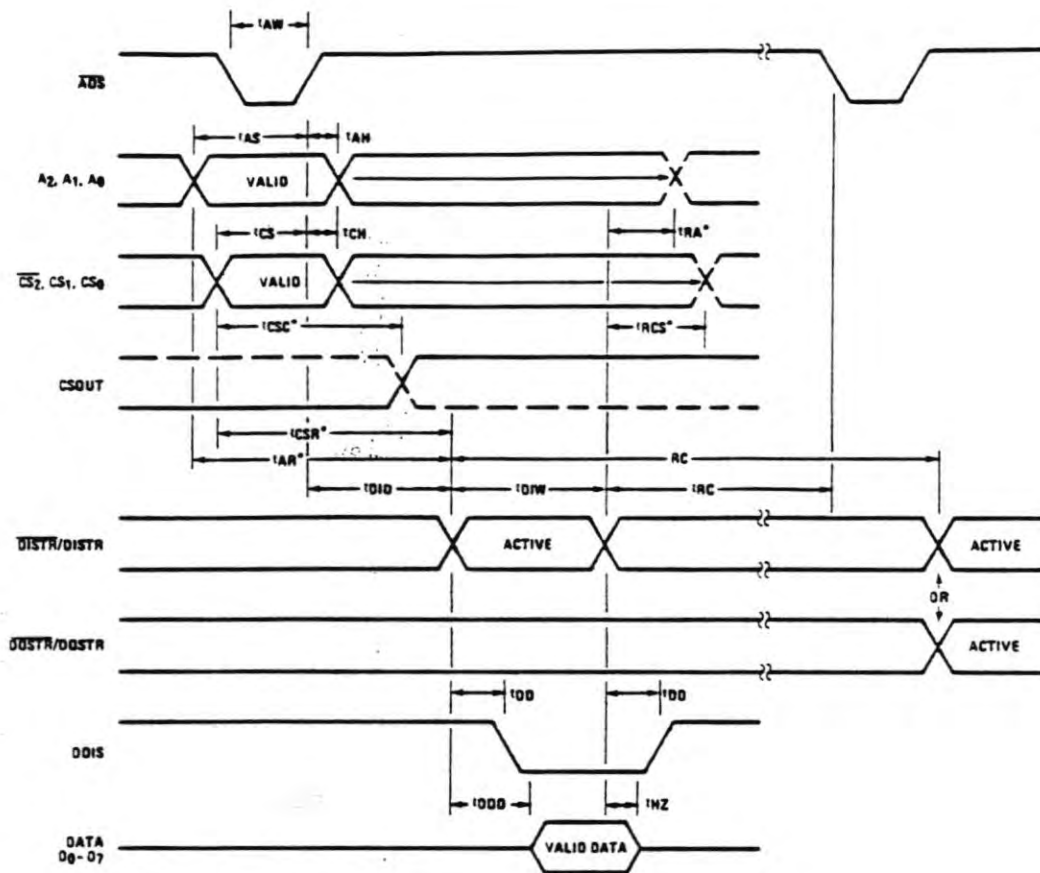
Timing Waveforms



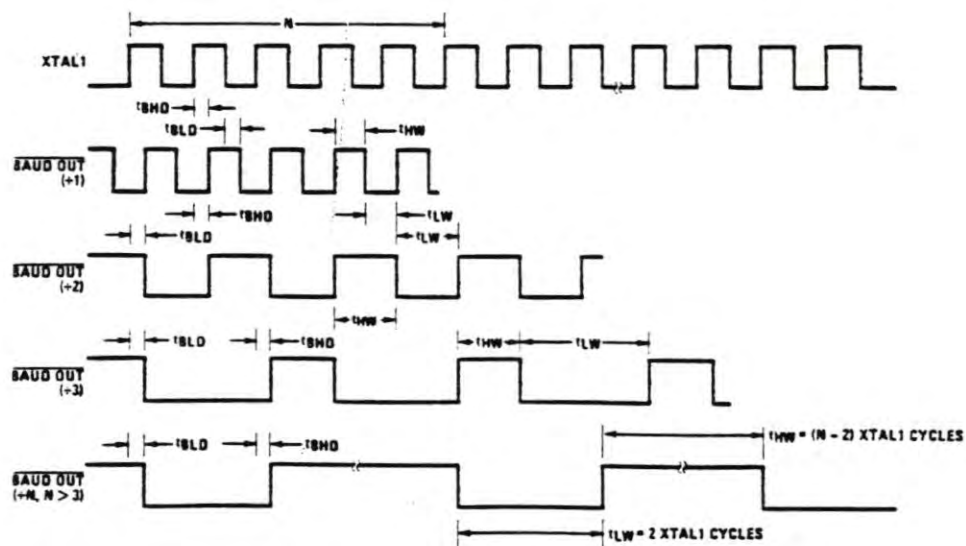
*APPLICABLE ONLY WHEN A0S IS TIED LOW.

Write Cycle

Timing Waveforms (continued)

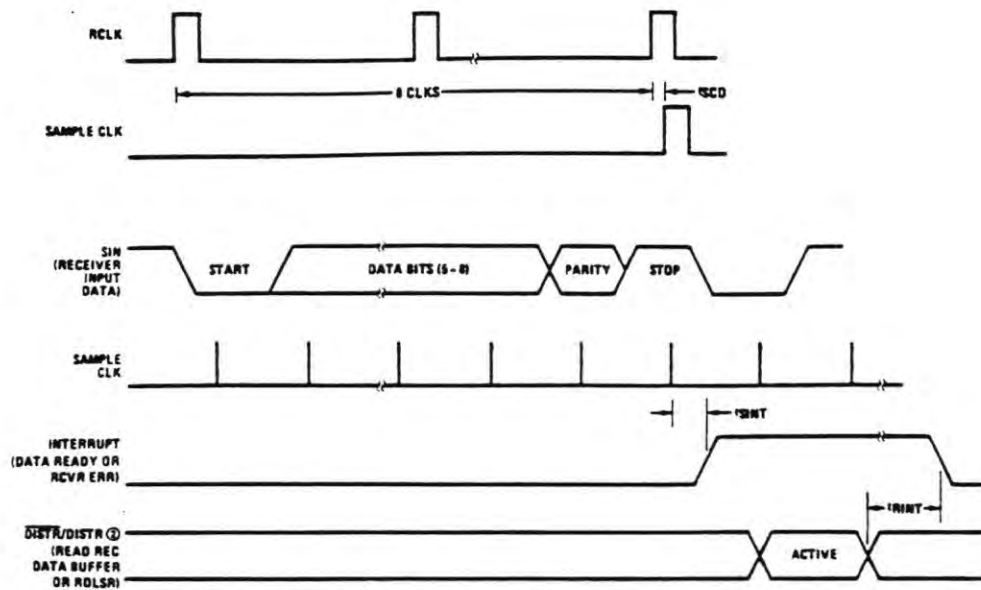


Read Cycle

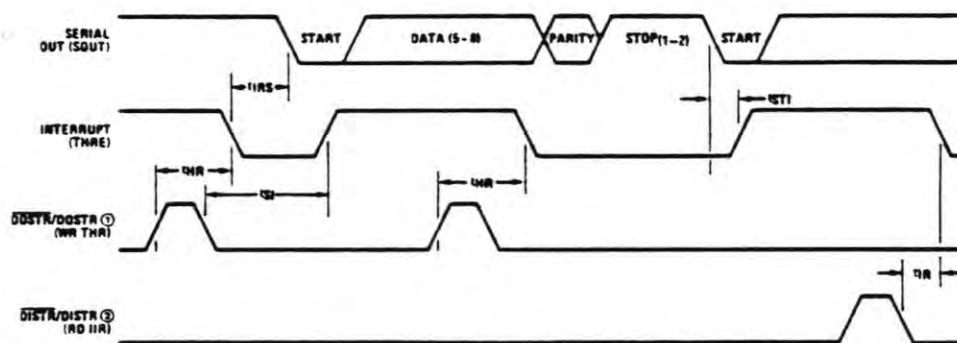


BAUDOUT Timing

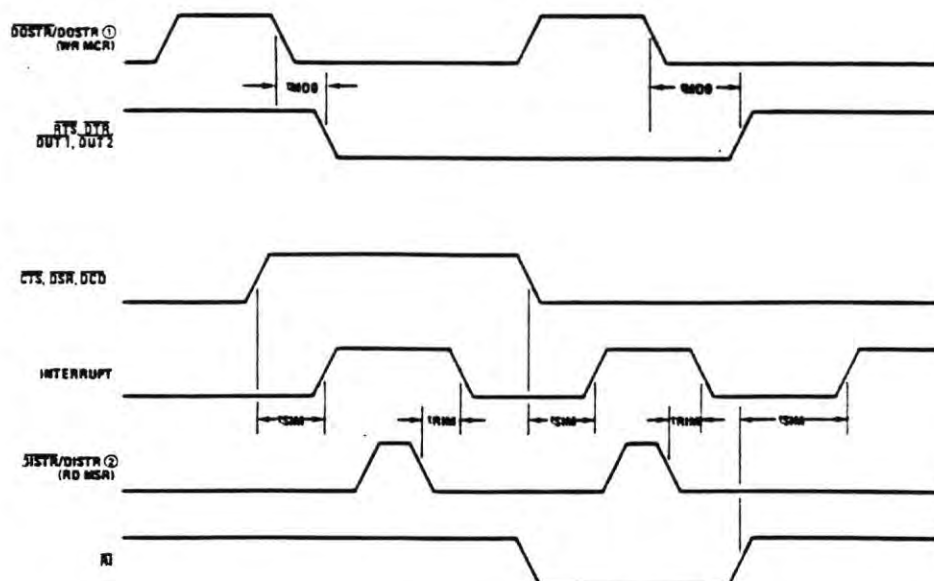
Timing Waveforms (continued)



Receiver Timing



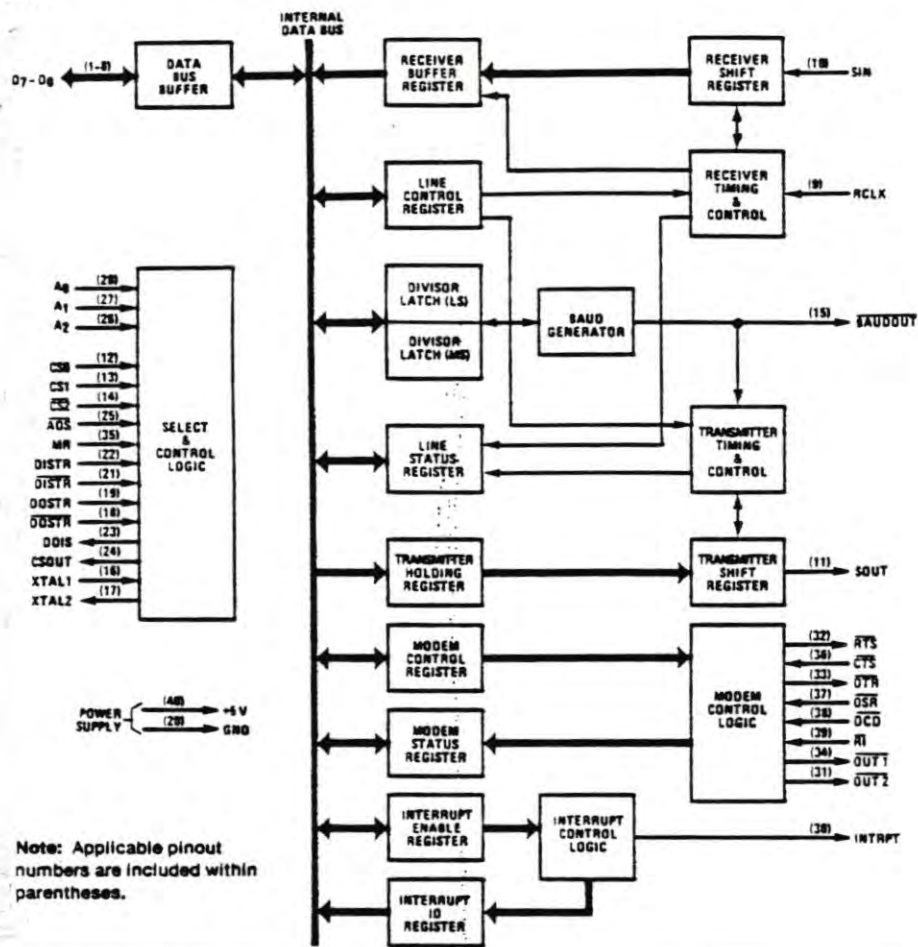
Transmitter Timing



MODEM Controls Timing

Note 1: See Write Cycle Timing

Block Diagram



Note: Applicable pinout numbers are included within parentheses.

Functional Pin Description

The following describes the function of all INS8250A input/output pins. Some of these descriptions reference internal circuits.

Note: In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Input Signals

Chip Select (CS0, CS1, $\overline{\text{CS2}}$), Pins 12-14: When CS0 and CS1 are high and $\overline{\text{CS2}}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{\text{ADS}}$) input. This enables communication between the INS8250A and the CPU.

Data Input Strobe (DISTR, $\overline{\text{DISTR}}$), Pins 22 and 21: When DISTR is high or $\overline{\text{DISTR}}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250A.

Note: Only an active DISTR or $\overline{\text{DISTR}}$ input is required to transfer data from the INS8250A during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{\text{DISTR}}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{\text{DOSTR}}$), Pins 19 and 18: When DOSTR is high or $\overline{\text{DOSTR}}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250A.

Note: Only an active DOSTR or $\overline{\text{DOSTR}}$ input is required to transfer data to the INS8250A during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{\text{DOSTR}}$ input permanently high, if not used.

Address Strobe ($\overline{\text{ADS}}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{\text{CS2}}$) signals.

Note: An active $\overline{\text{ADS}}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{\text{ADS}}$ input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an INS8250A register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250A registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A ₂	A ₁	A ₀	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: This input is buffered with a TTL-compatible Schmitt Trigger. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250A. Also, the state of various output signals (SOUT, INTRPT, OUT 1, OUT 2, RTS, DTR) are affected by an active MR input. (Refer to Table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16 x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send (CTS), Pin 36: The CTS signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register. CTS has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Data Set Ready (DSR), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250A. The DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Data Carrier Detect (DCD), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The DCD signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the DCD input has changed state since the previous reading of the MODEM Status Register. DCD has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Ring Indicator (RI), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The RI signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.

V_{CC}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

Output Signals

Data Terminal Ready (DTR), Pin 33: When low, informs the MODEM or data set that the INS8250A is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation. The DTR signal is forced to its inactive state (high) during loop mode operation.

Request to Send (RTS), Pin 32: When low, informs the MODEM or data set that the INS8250A is ready to transmit data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The RTS signal is set high upon a Master Reset operation. The RTS signal is forced to its inactive state (high) during loop mode operation.

Output 1 (OUT 1), Pin 34: User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. The OUT 1 signal is set high upon a Master Reset Operation. The OUT 1 signal is forced to its inactive state (high) during loop mode operation.

Output 2 (OUT 2), Pin 31: User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. The OUT 2 signal is set high upon a Master Reset Operation. The OUT 2 signal is forced to its inactive state (high) during loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250A. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250A on the D₇-D₀ Data Bus) at all times, except when the CPU is reading data.

Baud Out (BAUDOUT), Pin 15: $16 \times$ clock signal for the transmitter section of the INS8250A. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

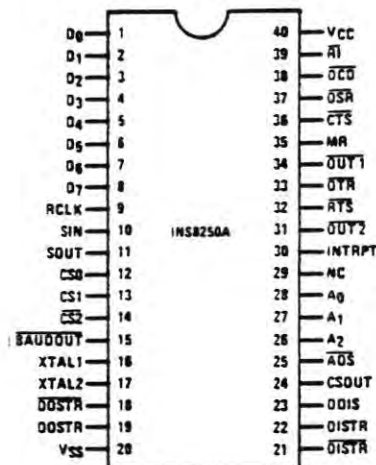
Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D_7 – D_0) Bus, Pins 1–8: This bus comprises eight TRI-STATE[®] input/output lines. The bus provides bidirectional communications between the INS8250A and the CPU. Data, control words, and status information are transferred via the D_7 – D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2) Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250A.



Pin Configuration

Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3–7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0–3 Low Bits 4–7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

Accessible Registers

The system programmer may access or control any of the INS8250A registers summarized in Table 2 via the CPU. These registers are used to control INS8250A operations and to transmit and receive data.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one

Table 2. Summary of INS8250A Accessible Registers

Bit No.	Register Address										
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, TEND = 1, and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The INS8250A contains a programmable Baud Generator that is capable of taking any clock input (DC to 3.1MHz) and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baud Generator is $16 \times$ the Baud [divisor # = (frequency input) \div (baud rate \times 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432MHz and 3.072MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Note: The maximum operating frequency of the Baud Generator is 3.1MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1MHz. In no case should the data rate be greater than 56k Baud.

Table 3. Baud Rates Using 1.8432MHz Crystal

Desired Baud Rate	Divisor Used to Generate $16 \times$ Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Note: 1.8432MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072MHz Crystal

Desired Baud Rate	Divisor Used to Generate $16 \times$ Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250A is ready to accept a new character for transmission. In addition, this bit causes the INS8250A to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: For diagnostic purposes, bits 0 to 5 can be written to, while bit 6 is read only.

Interrupt Identification Register

The INS8250A has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250A prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the INS8250A to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready (\overline{DTR}) output. When bit 0 is set to a logic 1, the \overline{DTR} output is forced to a logic 0. When bit 0 is reset to a logic 0, the \overline{DTR} output is forced to a logic 1.

Note: The \overline{DTR} output of the INS8250A may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (\overline{RTS}) output. Bit 1 affects the \overline{RTS} output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the INS8250A. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (\overline{CTS} , \overline{DSR} , \overline{DCD} , and \overline{RI}) are disconnected; and the four MODEM Control outputs (\overline{DTR} , \overline{RTS} , $\overline{OUT 1}$, and $\overline{OUT 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and receive-data paths of the INS8250A.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250A interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250A operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 or the MODEM Control Register must be reset to logic 0. The Transmitter should be IDLE when this bit changes state.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the \overline{CTS} input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the \overline{DSR} input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the \overline{RI} input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the \overline{DCD} input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Typical Applications

Figures 1 and 2 show how to use the INS8250A chip in an INS8080A system and in a microcomputer system with a high-capacity data bus.

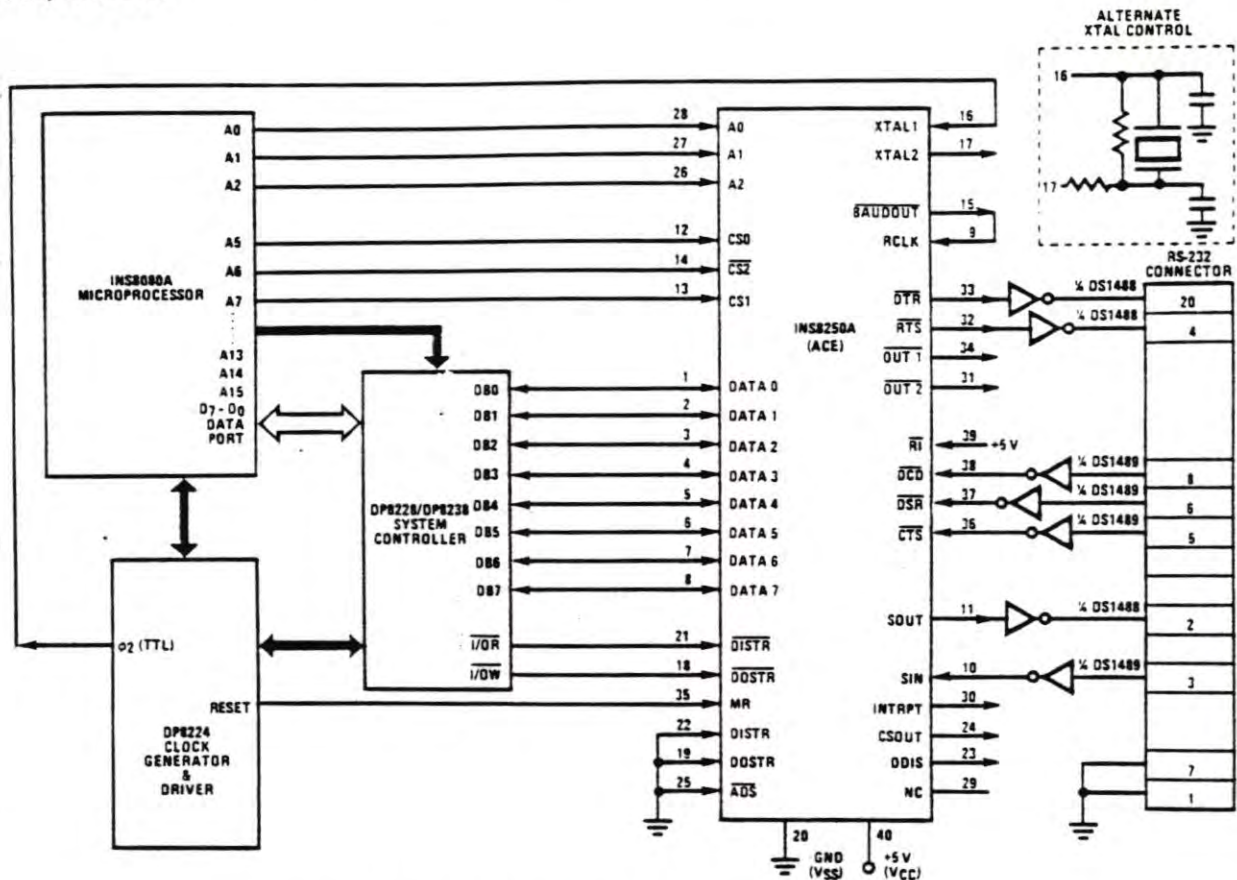


FIGURE 1. Typical INS8080A/INS8250 RS232 Terminal Interface

Bit 4: This bit is the complement of the Clear to Send ($\overline{\text{CTS}}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{\text{DSR}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{\text{RI}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{\text{DCD}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register: This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

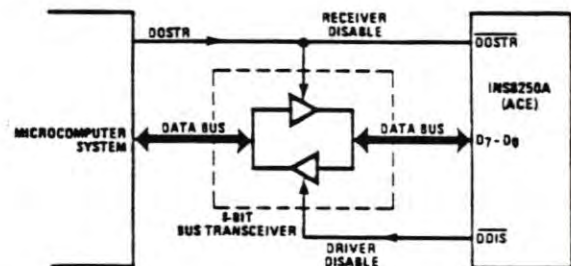
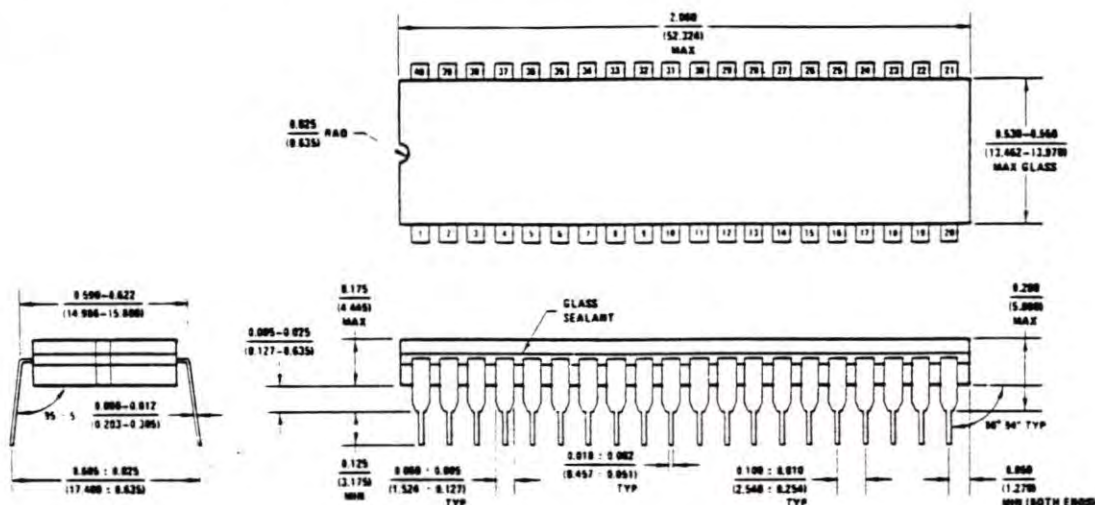
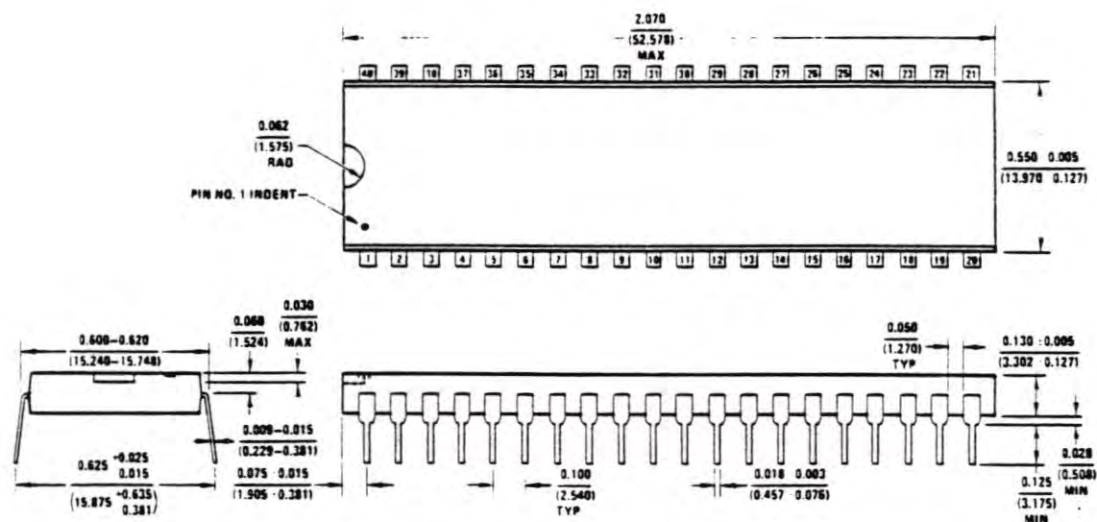


FIGURE 2. Typical Interface for a High-Capacity Data Bus

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number INS8250AJ
NS Package Number J40B



Plastic Dual-In-Line Package (N)
Order Number INS8250AN
NS Package Number N40X

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**MOTOROLA**

SEMICONDUCTORS

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64K BIT DYNAMIC RAM

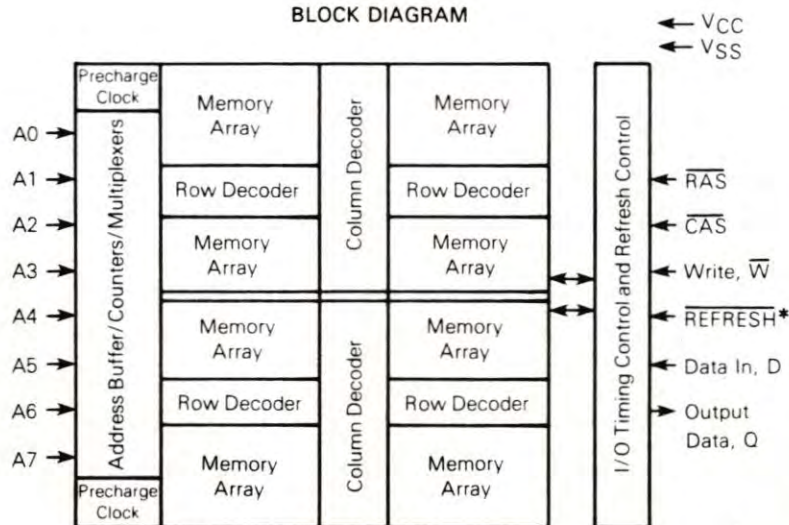
The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation ($\pm 10\%$)
- Full Power Supply Range Capabilities
- Maximum Access Time
 - MCM6665A-12 = 120 ns
 - MCM6665A-15 = 150 ns
 - MCM6665A-20 = 200 ns
- Low Power Dissipation
 - 302.5 mW Maximum (Active) (MCM6665A-15)
 - 22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate $< 0.1\%$ per 1000 Hours (See Soft Error Testing)

BLOCK DIAGRAM



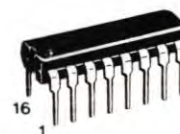
* Refresh Function Available on MCM6664A

MCM6665A

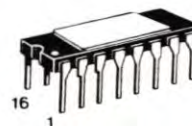
MOS

(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

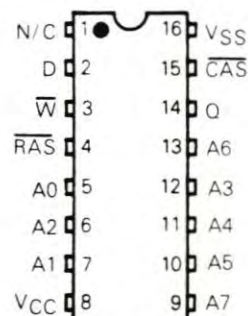


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES

A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{VCC}}$	Power (+5 V)
$\overline{\text{VSS}}$	Ground

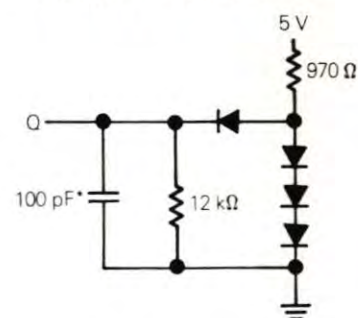
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	-2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	—	$V_{CC} + 1$	V	1
Logic 0 Voltage, All Inputs	V_{IL}	-1.0*	—	0.8	V	1

*The device will withstand undershoots to the -2 volt level with a maximum pulse width of 20 ns at the -1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	—	4.0	mA	5
V_{CC} Power Supply Current 6665A-12, $t_{RC} = 250$ ns 6665A-15, $t_{RC} = 270$ ns 6665A-20, $t_{RC} = 330$ ns	I_{CC1}	—	60 55 50	mA	4
V_{CC} Power Supply Current During \overline{RAS} only Refresh Cycles 6665A-12, $t_{RC} = 250$ ns 6665A-15, $t_{RC} = 270$ ns 6665A-20, $t_{RC} = 330$ ns	I_{CC3}	—	50 45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS} = 10 \mu\text{sec}$ 6665A-12, $t_{PC} = t_{RP} = 120$ ns 6665A-15, $t_{PC} = t_{RP} = 145$ ns 6665A-20, $t_{PC} = t_{RP} = 200$ ns	I_{CC4}	—	45 40 35	mA	4
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{I(L)}$	—	10	μA	—
Output Leakage Current (\overline{CAS} at logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{O(L)}$	—	10	μA	—
Output Logic 1 Voltage @ $I_{out} = -4$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out} = 4$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25^\circ\text{C}$, $V_{CC} = 5$ V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance \overline{RAS} , \overline{CAS} , \overline{WRITE}	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS} = V_{IH}$ to disable output)	C_O	5	7	pF	7

- NOTES:
1. All voltages referenced to V_{SS} .
 2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
 3. An initial pause of 100 μs is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is guaranteed.
 4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
 5. \overline{RAS} and \overline{CAS} are both at a logic 1.
 6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
 7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$



AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

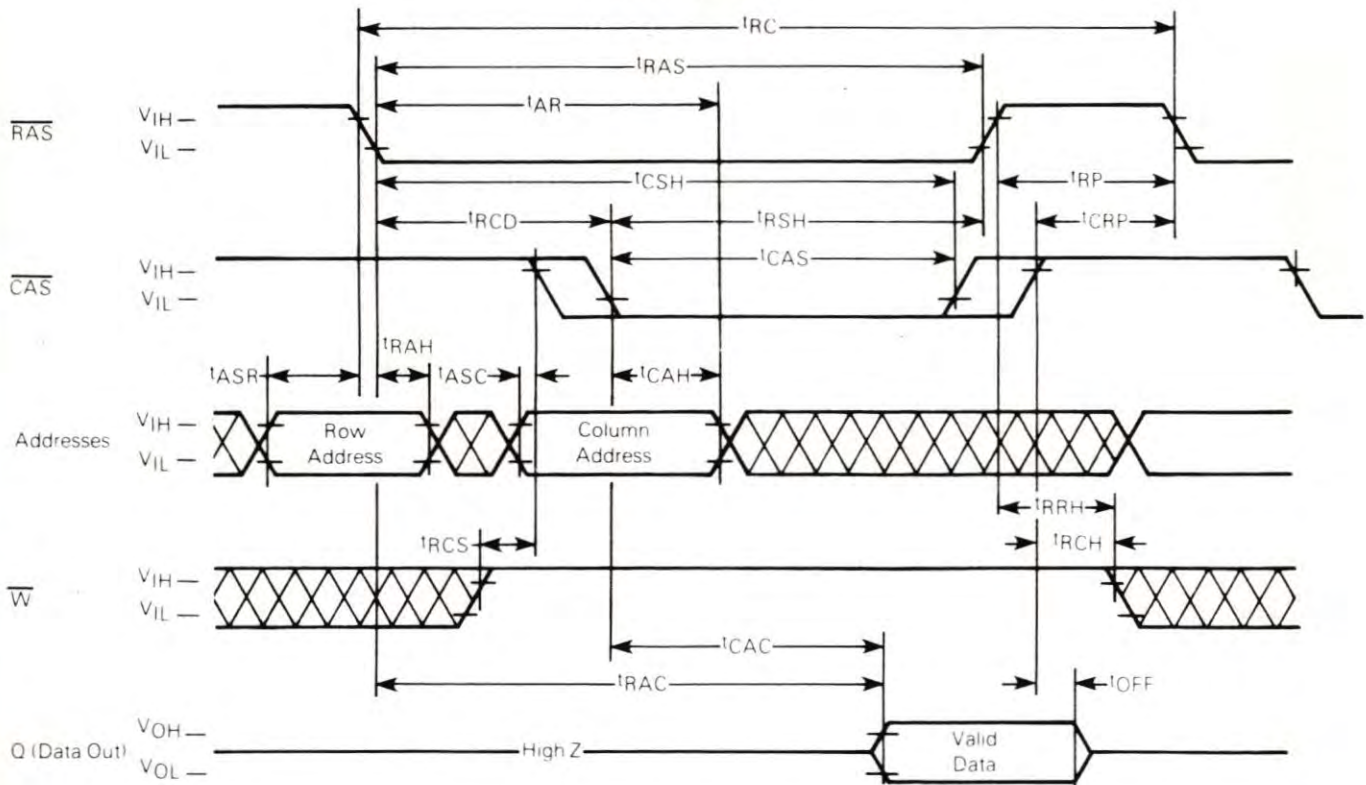
(Full Operating Voltage and Temperature Range Unless Otherwise Noted, See Notes 2, 3, 6, and Figure 1)

Parameter	Symbol	6665A-12		6665A-15		6665A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	—	270	—	330	—	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	—	280	—	345	—	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	—	120	—	150	—	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	—	60	—	75	—	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	—	100	—	120	—	ns	—
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	—
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	—
Row to Column Strobe Lead Time	t_{RCD}	25	60	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t_{RAH}	15	—	20	—	25	—	ns	—
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t_{CAH}	25	—	35	—	45	—	ns	—
Column Address Hold Time Referenced to \overline{RAS}	t_{AR}	85	—	95	—	120	—	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	—
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	14
Read Command Hold Time Referenced to \overline{RAS}	t_{RRH}	0	—	0	—	0	—	ns	14
Write Command Hold Time	t_{WCH}	25	—	35	—	45	—	ns	—
Write Command Hold Time Referenced to \overline{RAS}	t_{WCR}	85	—	95	—	120	—	ns	17
Write Command Pulse Width	t_{WP}	25	—	35	—	45	—	ns	—
Write Command to Row Strobe Lead Time	t_{RWL}	40	—	45	—	55	—	ns	—
Write Command to Column Strobe Lead Time	t_{CWL}	40	—	45	—	55	—	ns	—
Data in Setup Time	t_{DS}	0	—	0	—	0	—	ns	15
Data in Hold Time	t_{DH}	25	—	35	—	45	—	ns	15
Data in Hold Time Referenced to \overline{RAS}	t_{DHR}	85	—	95	—	120	—	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	—10	—	—10	—	—10	—	ns	—
\overline{RAS} Hold Time	t_{RSH}	60	—	75	—	100	—	ns	—
Refresh Period	t_{RFSH}	—	2.0	—	2.0	—	2.0	ms	—
WRITE Command Setup Time	t_{WCS}	—10	—	—10	—	—10	—	ns	16
\overline{CAS} to WRITE Delay	t_{CWD}	40	—	45	—	55	—	ns	16
\overline{RAS} to WRITE Delay	t_{RWD}	100	—	120	—	155	—	ns	16
\overline{CAS} Hold Time	t_{CSH}	120	—	150	—	200	—	ns	—
\overline{CAS} Precharge Time (Page Mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	—
Page Mode Cycle Time	t_{PC}	120	—	145	—	200	—	ns	—

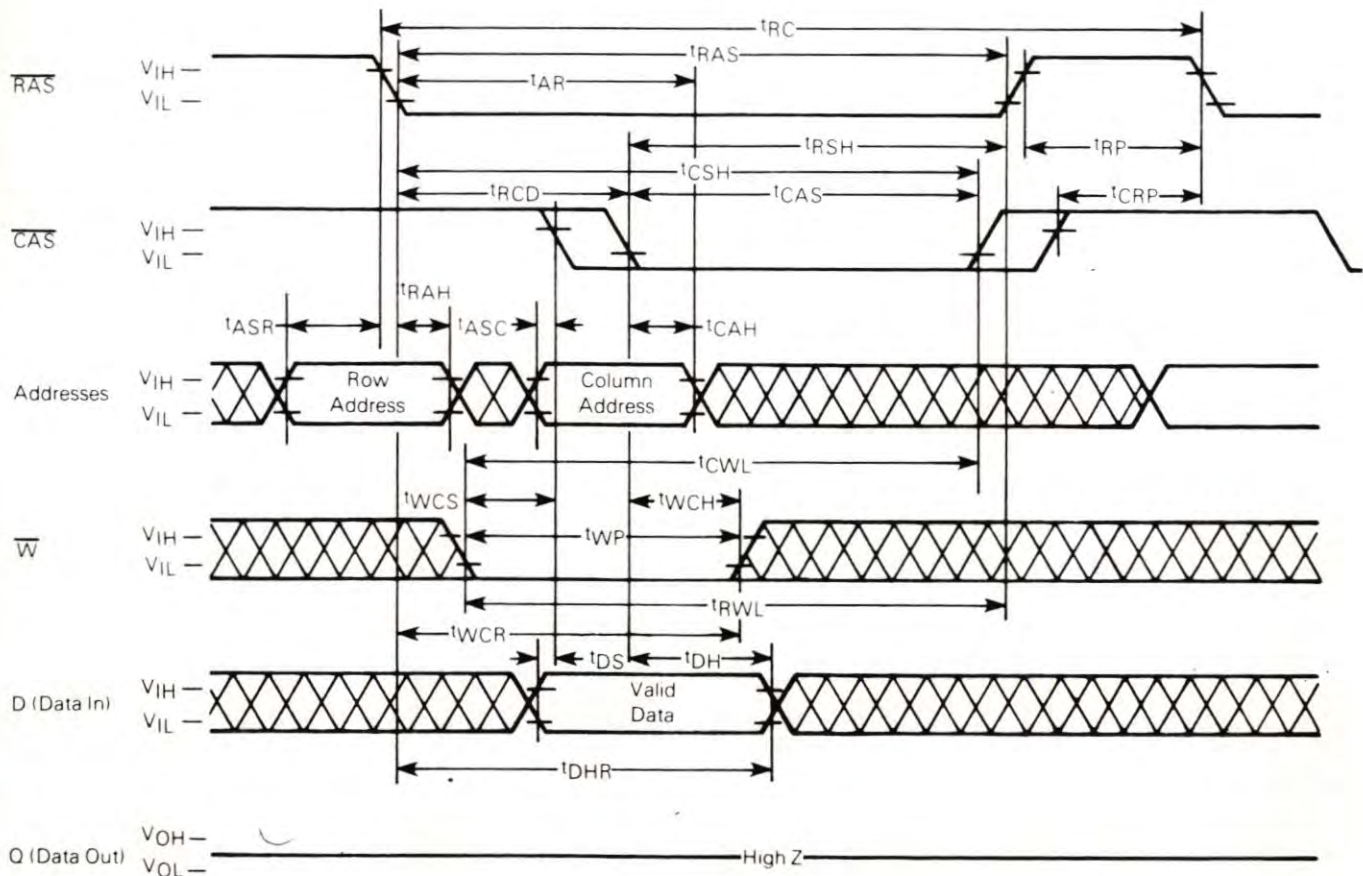
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$.
11. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
12. Measured with a current load equivalent to 2 TTL ($-200 \mu\text{A}$, $+4 \text{ mA}$) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0 \text{ V}$ and $V_{OL} = 0.8 \text{ V}$.
13. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to \overline{CAS} leading edge in random write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write cycles.
16. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. $t_{AR} \text{ min} \leq t_{AR} = t_{RCD} + t_{CAH}$
 $t_{DHR} \text{ min} \leq t_{DHR} = t_{RCD} + t_{DH}$
 $t_{WCR} \text{ min} \leq t_{WCR} = t_{RCD} + t_{WCH}$
18. $t_{off}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.



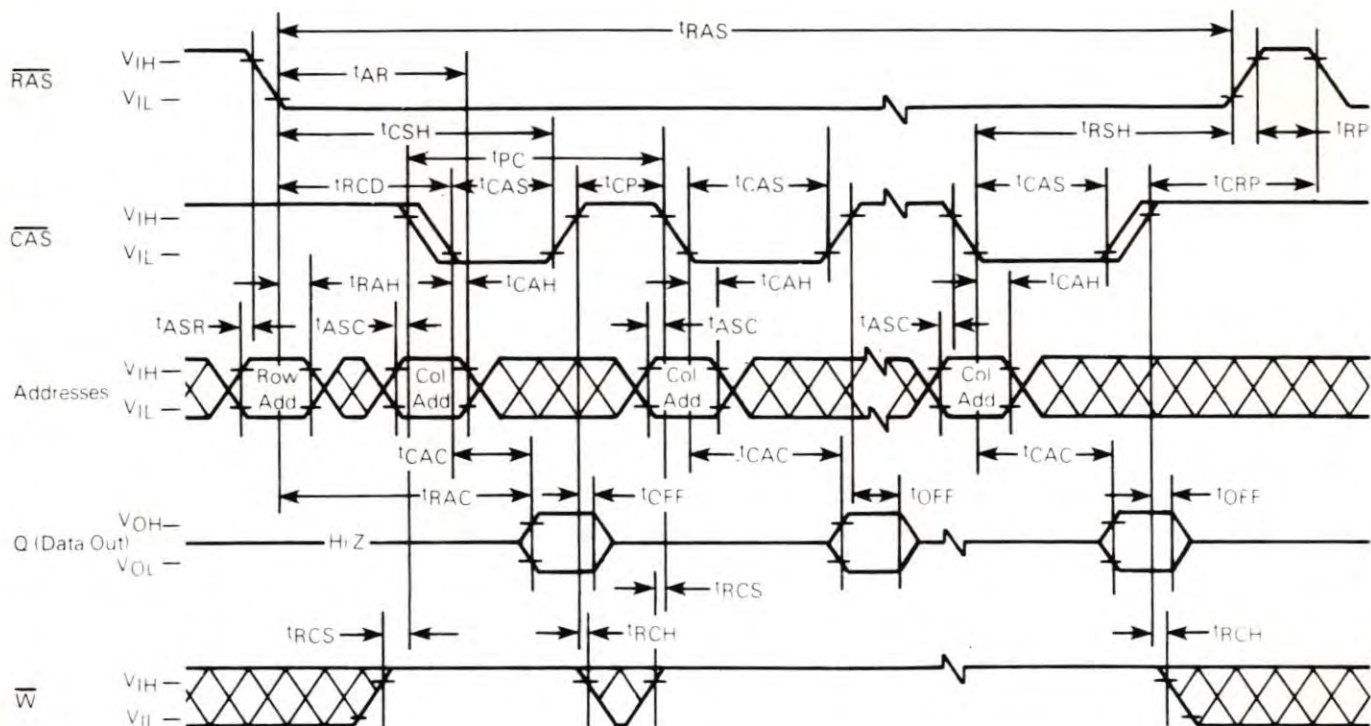
READ CYCLE TIMING



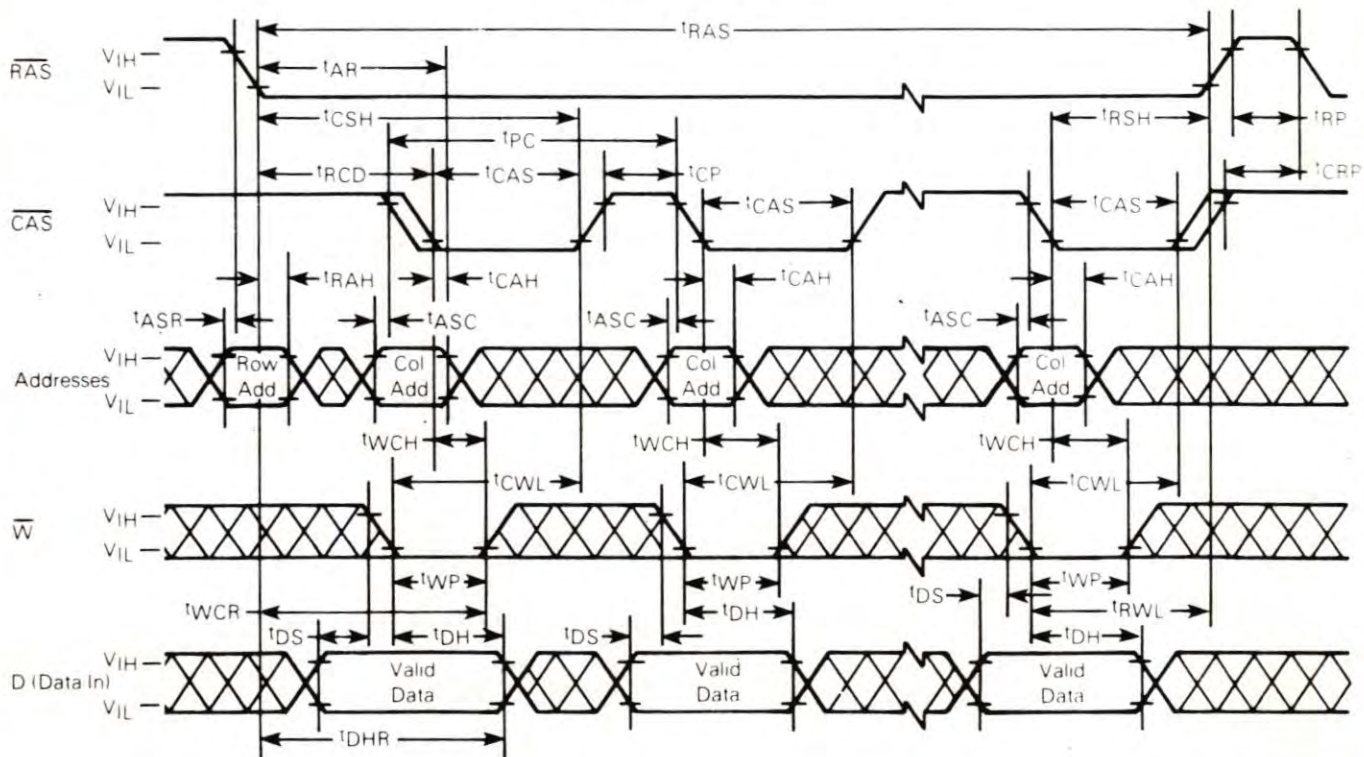
WRITE CYCLE TIMING



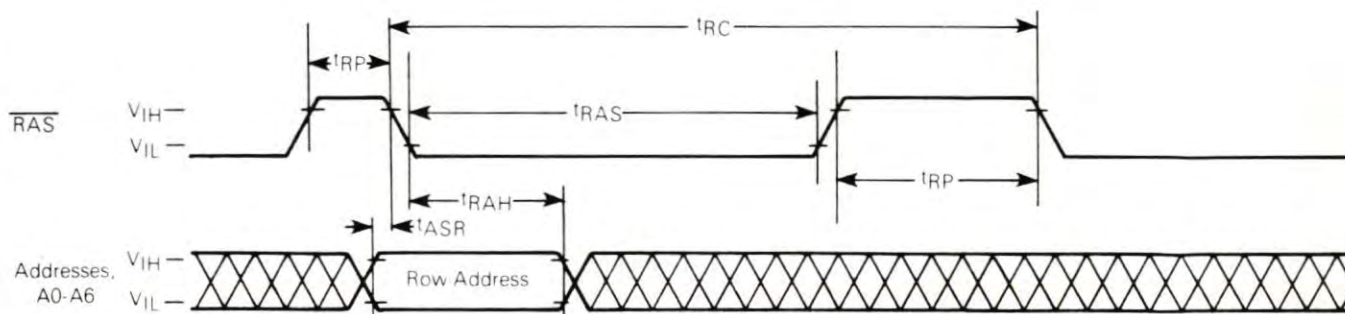
PAGE MODE READ CYCLE



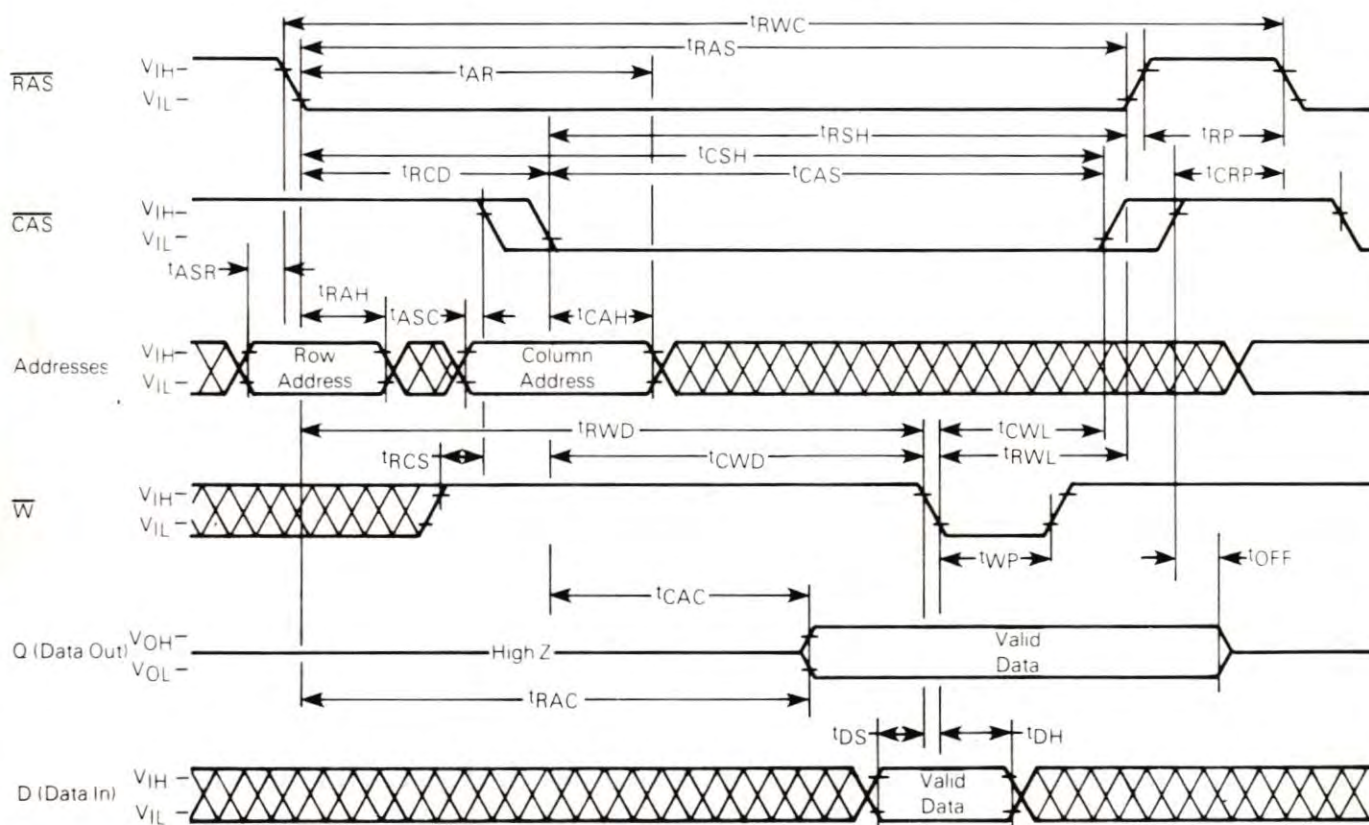
PAGE MODE WRITE CYCLE



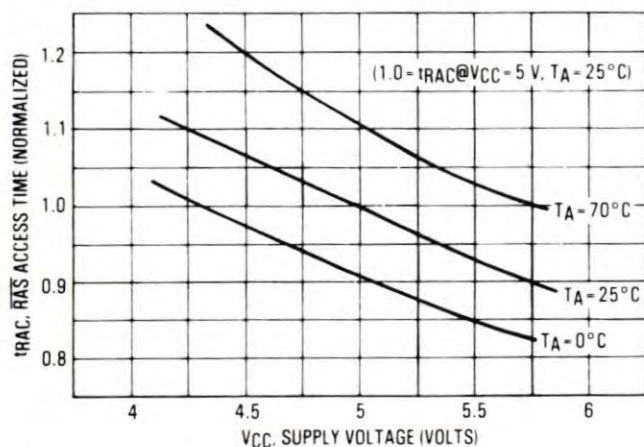
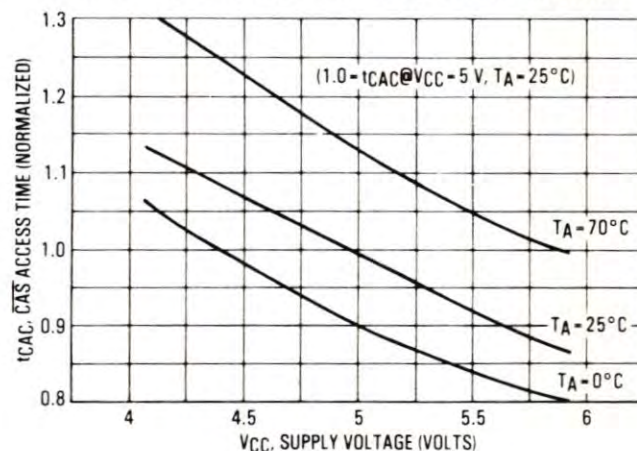
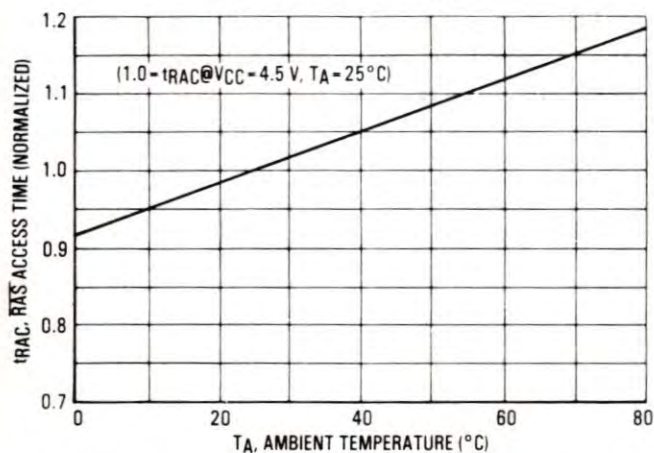
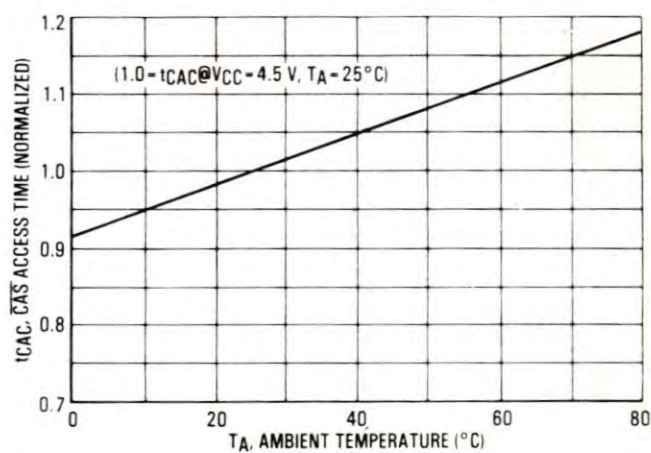
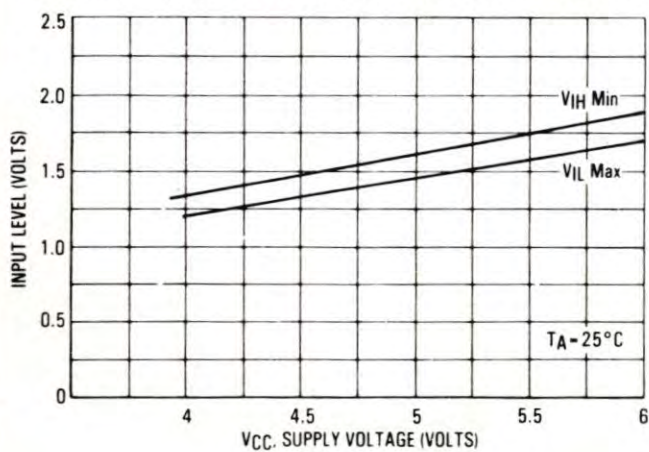
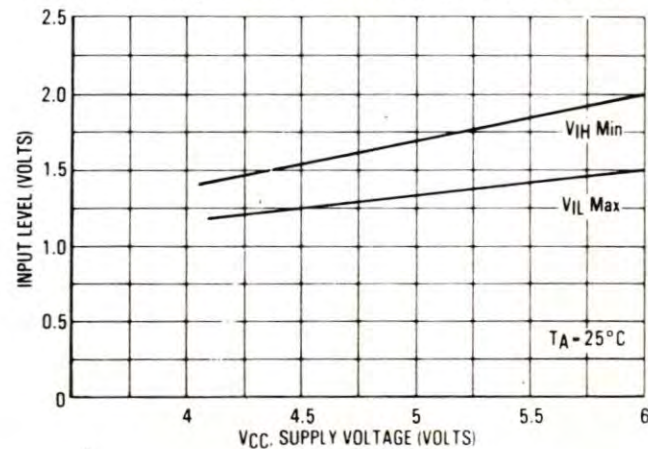
RAS-ONLY REFRESH CYCLE
 (Data-in and Write are Don't Care, CAS is HIGH)



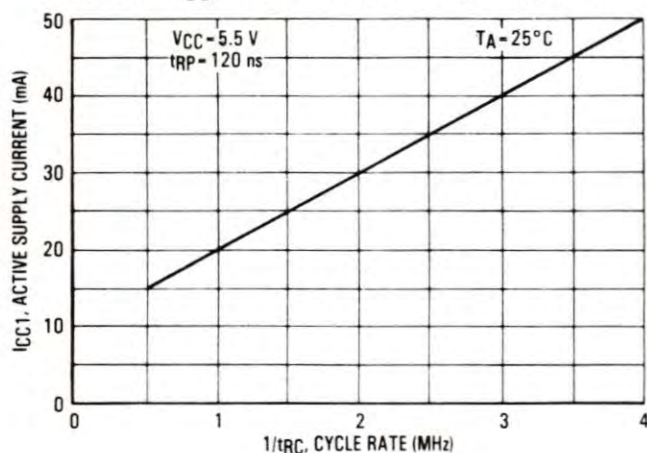
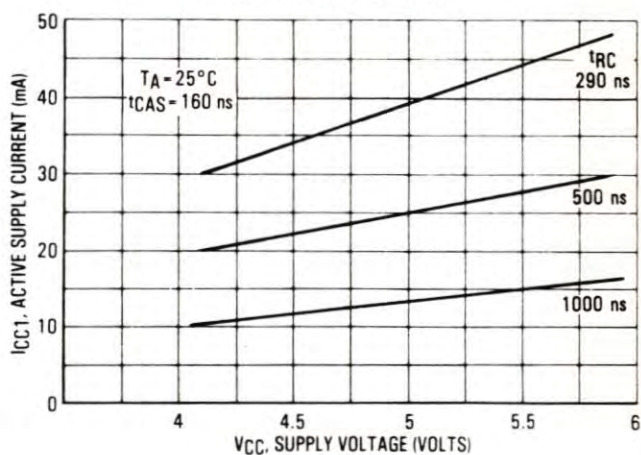
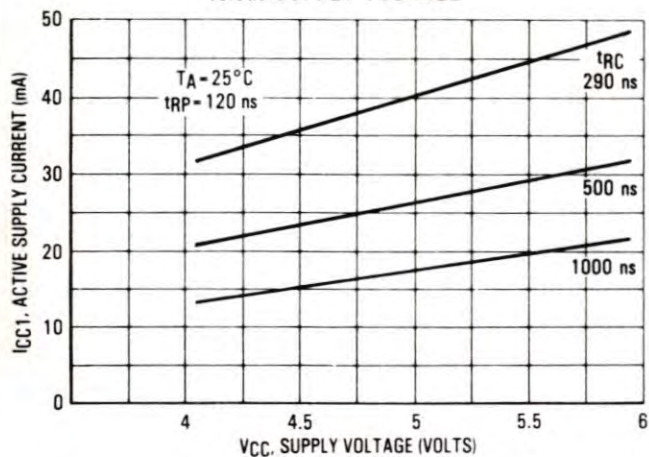
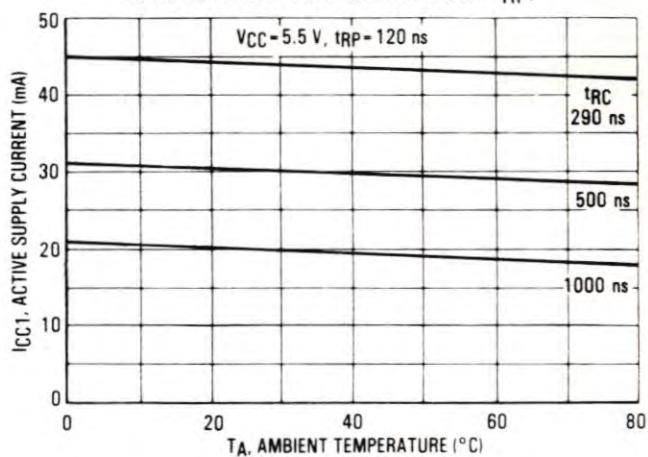
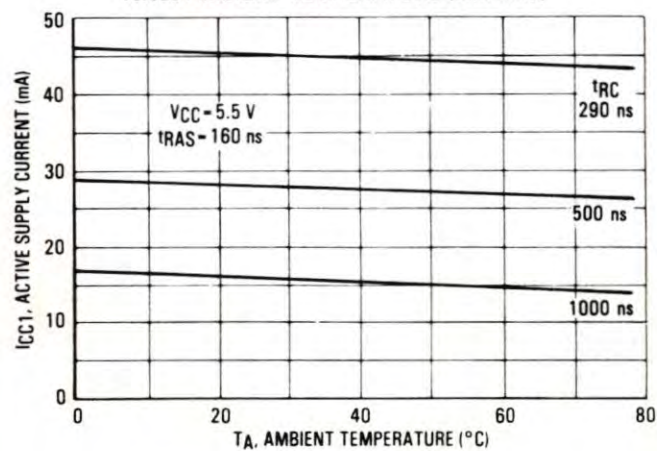
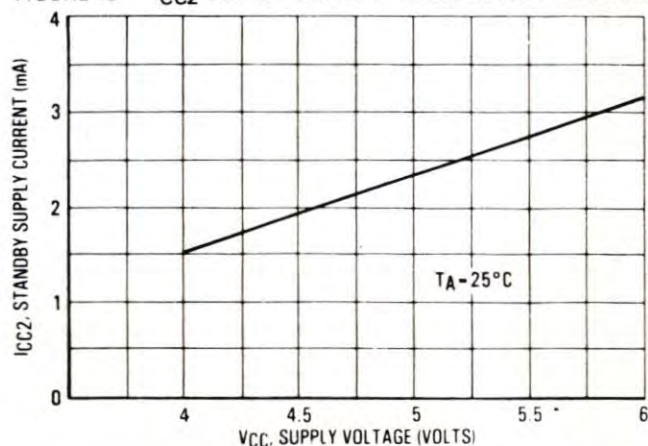
READ-WRITE/READ-MODIFY-WRITE CYCLE



TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{\text{RAS}}$ ACCESS TIME versus SUPPLY VOLTAGEFIGURE 3 — $\overline{\text{CAS}}$ ACCESS TIME versus SUPPLY VOLTAGEFIGURE 4 — $\overline{\text{RAS}}$ ACCESS TIME versus AMBIENT TEMPERATUREFIGURE 5 — $\overline{\text{CAS}}$ ACCESS TIME versus AMBIENT TEMPERATUREFIGURE 6 — $\overline{\text{RAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGEFIGURE 7 — $\overline{\text{CAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATEFIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGEFIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGEFIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{AS})FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — I_{CC2} STANDBY CURRENT
versus AMBIENT TEMPERATURE

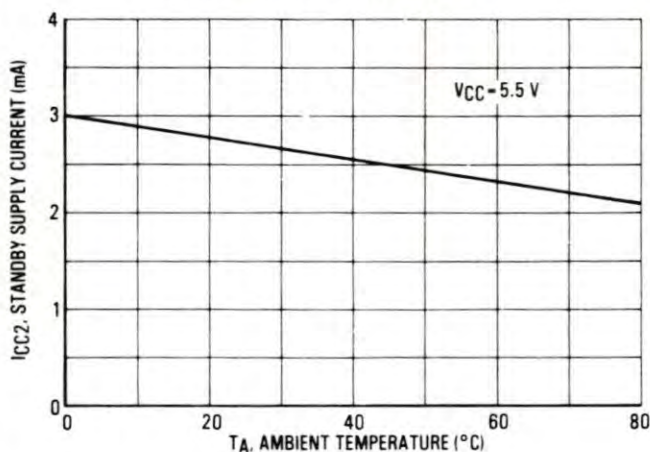


FIGURE 15 — I_{CC3} SUPPLY CURRENT versus CYCLE RATE

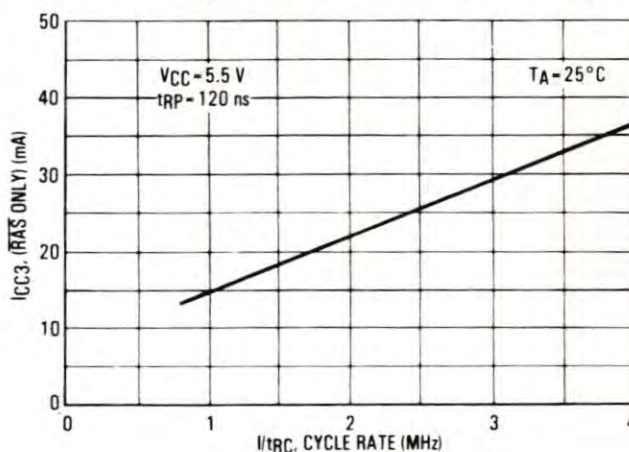


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

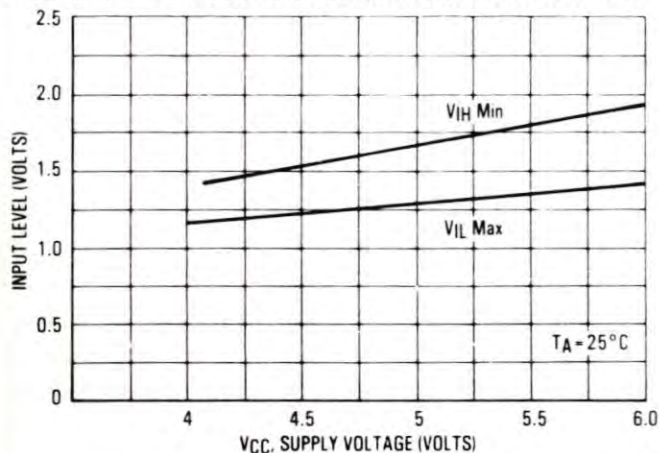
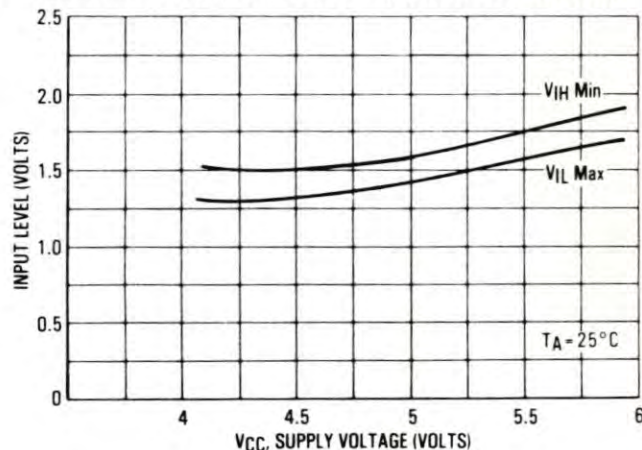


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

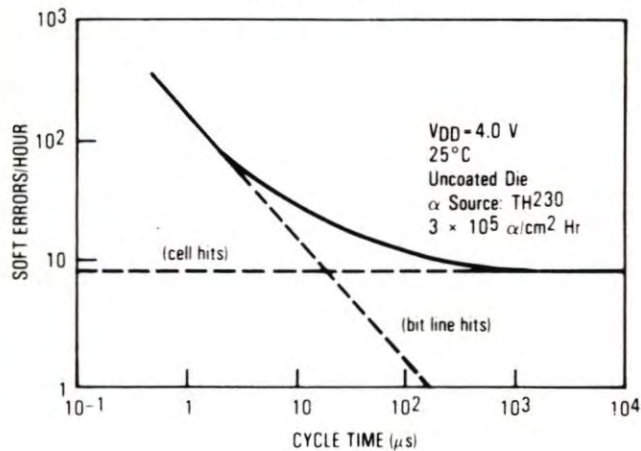
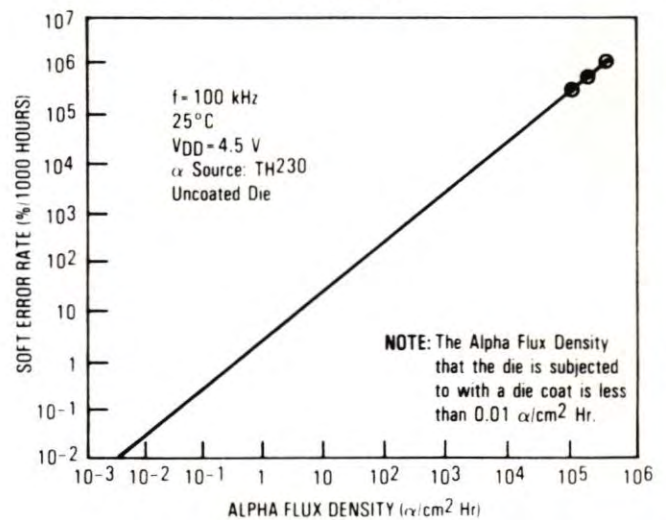
Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm²/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm²/hr) placed over un-

coated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

- 1) Cycle time: 1 microsecond for read, write and refresh cycles
- 2) Refresh Rate: 1 millisecond
- 3) Voltage: 5.0 V
- 4) Temperature: $30^\circ\text{C} \pm 2^\circ\text{C}$ (ambient temperature inside enclosure)
- 5) Elevation: Approximately 620 feet above mean sea level
- 6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.



FIGURE 18 — ACCELERATED SOFT ERROR
versus CYCLE TIMEFIGURE 19 — SOFT ERROR RATE versus
ALPHA FLUX DENSITY

CURRENT WAVEFORMS

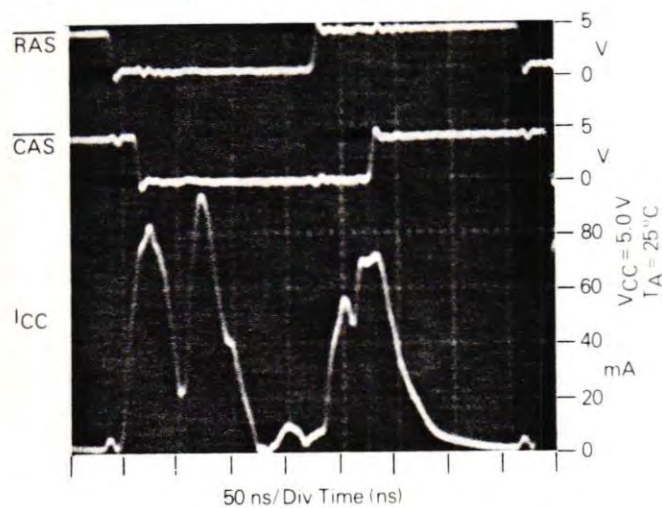
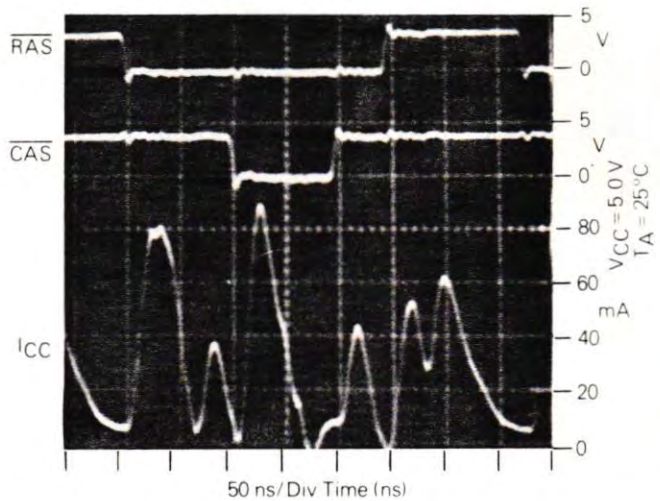
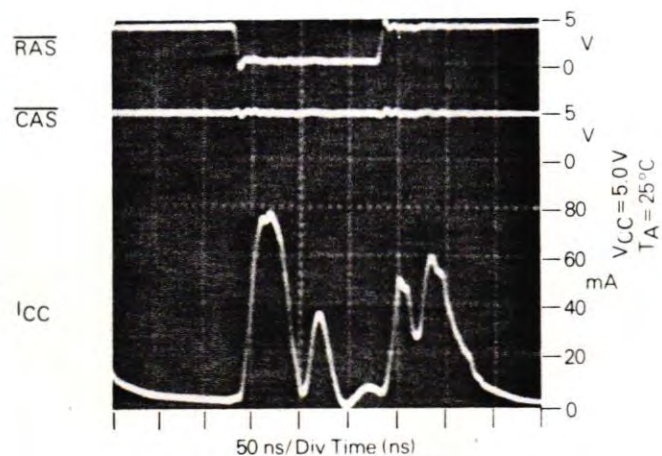
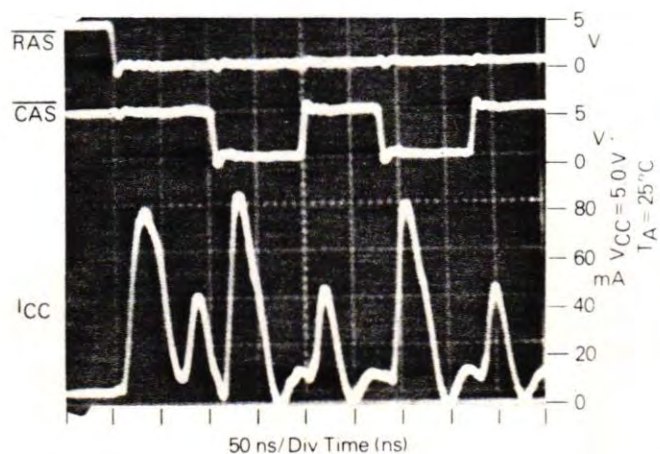
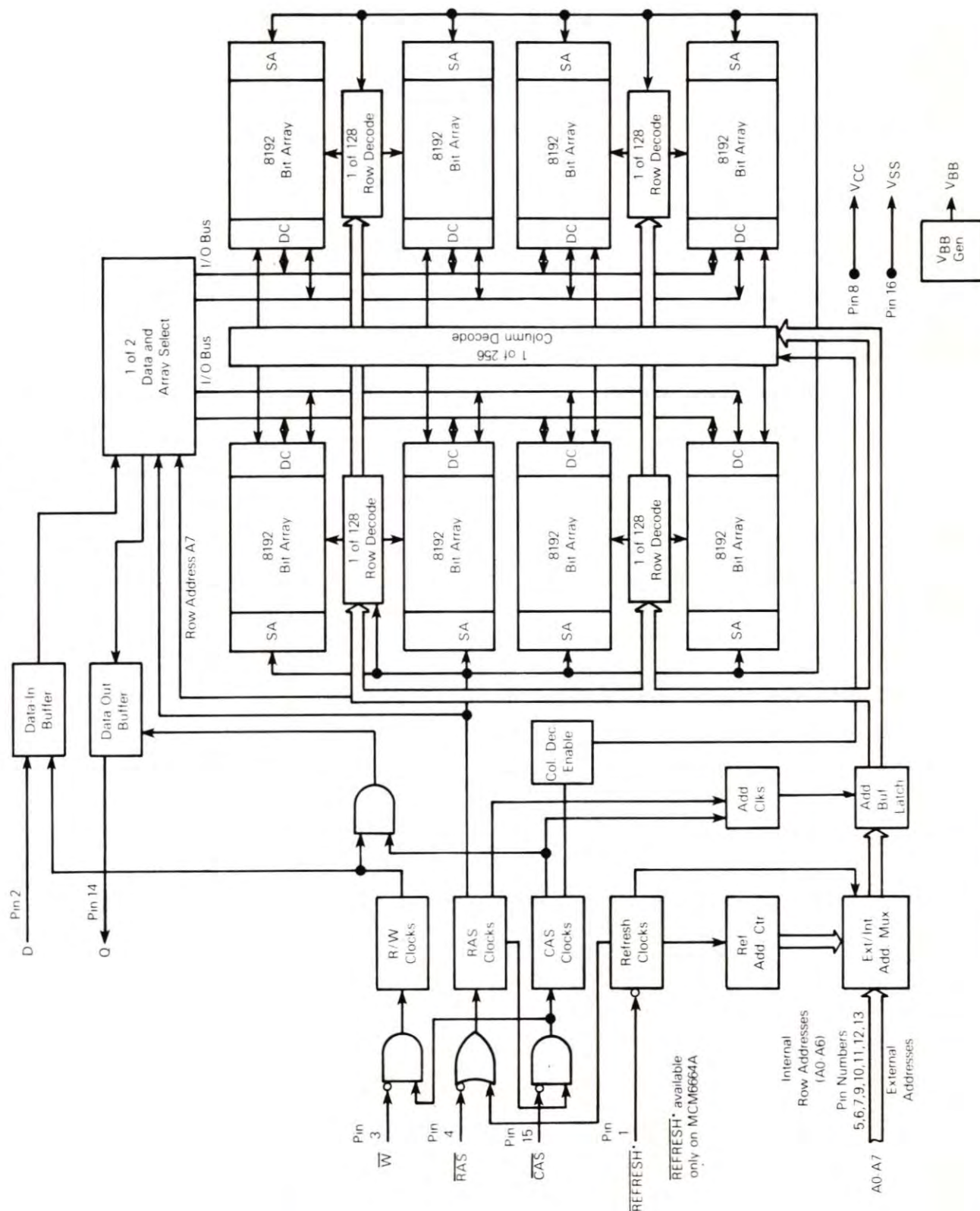
FIGURE 20 — $\overline{\text{RAS}}/\overline{\text{CAS}}$ CYCLEFIGURE 21 — LONG $\overline{\text{RAS}}/\overline{\text{CAS}}$ CYCLEFIGURE 22 — $\overline{\text{RAS}}$ ONLY CYCLE

FIGURE 23 — PAGE MODE CYCLE





DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25, 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column

address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called " t_{RCD} ," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the \overline{CAS} clock, and the other is the \overline{RAS} only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the \overline{RAS} clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate it from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the \overline{RAS} clock transitioning from V_{IH} to the V_{IL} level. The \overline{CAS} clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the \overline{RAS} and \overline{CAS} clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the \overline{CAS} clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, \overline{RAS} , $\overline{CAS} = V_{CC}$

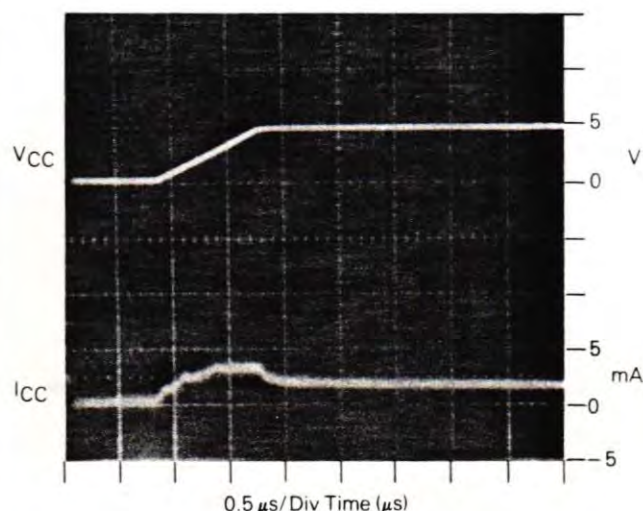
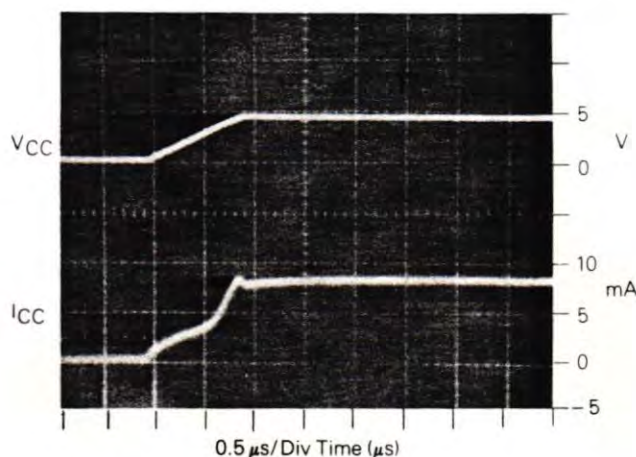


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, \overline{RAS} , $\overline{CAS} = V_{SS}$



the t_{RCD} maximum specification for an access (data valid) from the \overline{RAS} clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the \overline{CAS} clock active transition will determine read access time. The external \overline{CAS} signal is ignored until an internal \overline{RAS} signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the \overline{CAS} clock will allow the external \overline{CAS} signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the \overline{CAS} clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the \overline{RAS} clock and the minimum (t_{CAS}) period for the \overline{CAS} clock. The \overline{RAS} clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the \overline{CAS} clock is active; the output will switch to the three-state mode when the \overline{CAS} clock goes inactive. The \overline{CAS} clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write (\overline{W}) input must be held at the V_{IH} level from the time the \overline{CAS} clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write (\overline{W}) clock must go active (V_{IL} level) at or before the \overline{CAS} clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the \overline{CAS} clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that \overline{RAS} and \overline{CAS} clocks need to be active after the write operation has started (\overline{W} clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the \overline{CAS} goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write (\overline{W}) clock can occur much later in time with respect to the active transition of the \overline{CAS} clock. This time could be as long as 10 microseconds — [$t_{RWL} + t_{RP} + 2T_1$].

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write (\overline{W}) clock prevents the \overline{CAS} clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write (\overline{W}) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write (\overline{W}) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD} , t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write (\overline{W}) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write (\overline{W}) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular \overline{RAS} clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the \overline{RAS} clock active while cycling the \overline{CAS} clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one \overline{RAS} clock active operation. These are the refresh interval of the device ($2 \text{ ms}/128 = 15.6 \text{ microseconds}$) and the maximum active time specification for the \overline{RAS} clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the \overline{RAS} clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the \overline{RAS} clock is reset.

The page cycle is always initiated with a row address being provided and latched by the \overline{RAS} clock, followed by the column address and \overline{CAS} clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter \overline{CAS} cycles (t_{PC}). The \overline{CAS} cycle time (t_{PC}) consists of the \overline{CAS} clock active time (t_{CAS}), and \overline{CAS} clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

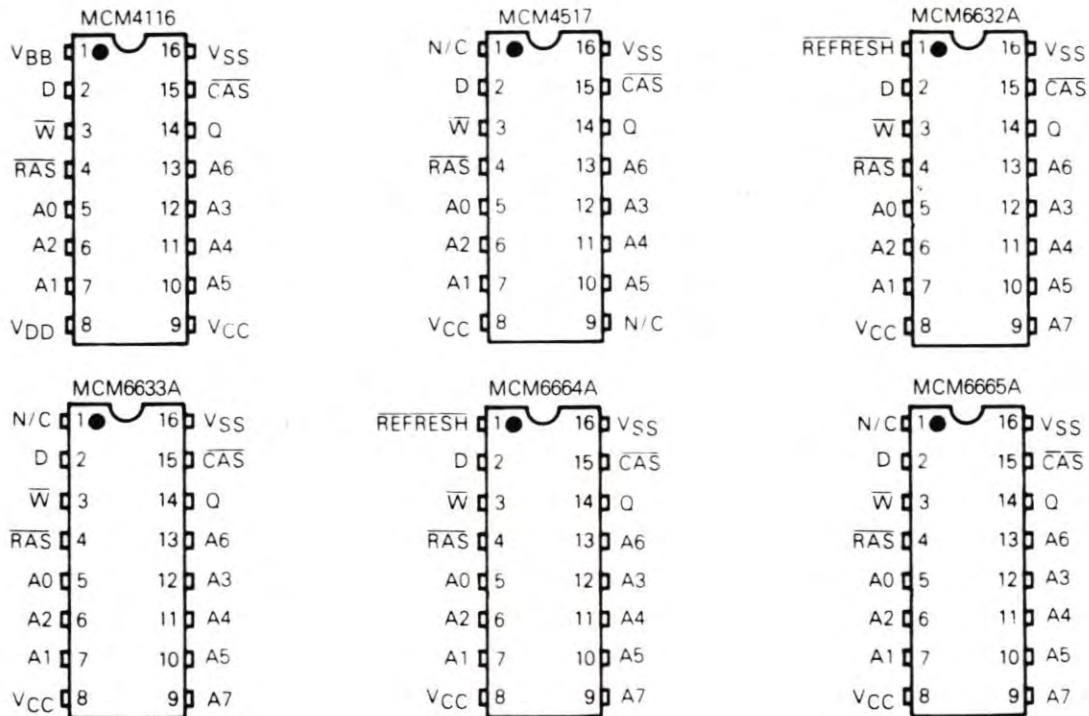
The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to



degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{\text{RAS}}$ Only Refresh — When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

PIN ASSIGNMENT COMPARISON

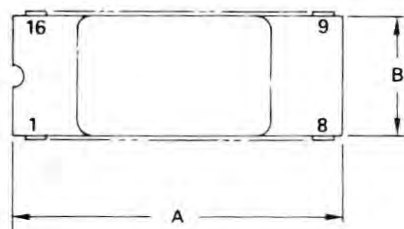


PIN VARIATIONS

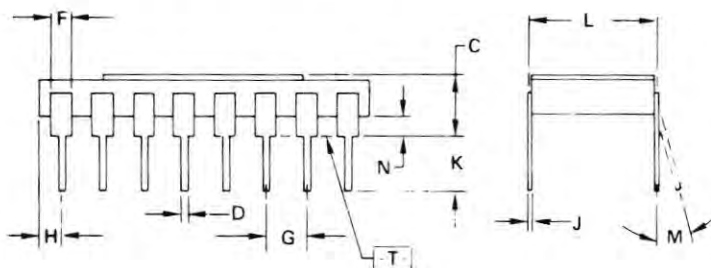
PIN NUMBER	MCM4116	MCM4517	MCM6632A	MCM6663A	MCM6664A	MCM6665A
1	$V_{BB}(-5\text{ V})$	N/C	REFRESH	N/C	REFRESH	N/C
8	$V_{DD}(+12\text{ V})$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	$V_{CC}(+5\text{ V})$	N/C	A7	A7	A7	A7



PACKAGE DIMENSIONS



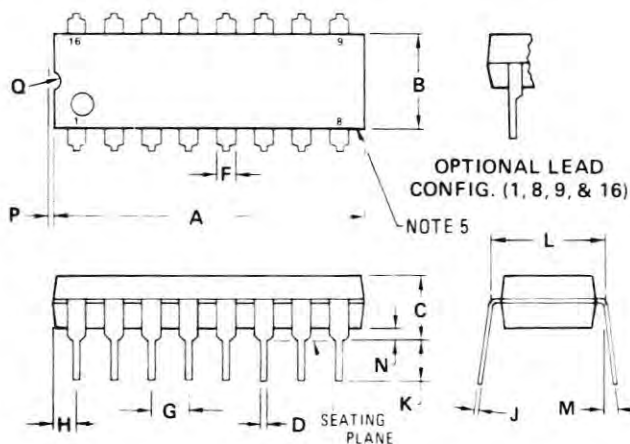
L SUFFIX
CERAMIC PACKAGE
CASE 690-13



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.38	1.52	0.015	0.060

NOTES:

1. A AND B ARE DATUMS.
2. T IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).
 $\phi 0.25 (0.010) \text{ T A B}$
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.



MCM6665A BIT ADDRESS MAP

Row Address A7 A6 A5 A4 A3 A2 A1 A0
Column Address A7 A6 A5 A4 A3 A2 A1 A0

Pin 8

Column Addresses

Row		Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
Column Addresses		FE	254	1	1	1	1	1	1	1	0
		FF	255	1	1	1	1	1	1	1	1
		FC	252	1	1	1	1	1	1	0	0
		FD	253	1	1	1	1	1	1	0	1
		FA	250	1	1	1	1	1	0	1	0
		FB	251	1	1	1	1	1	0	1	1
		F8	248	1	1	1	1	1	0	0	0
		F9	249	1	1	1	1	1	0	0	1
		C0	192	1	1	0	0	0	0	0	0
		C1	193	1	1	0	0	0	0	0	1
		BF	191	1	0	1	1	1	1	1	1
		BE	190	1	0	1	1	1	1	1	0
		83	131	1	0	0	0	0	0	1	1
		82	130	1	0	0	0	0	0	1	0
		81	129	1	0	0	0	0	0	0	1
		80	128	1	0	0	0	0	0	0	0
		7E	126	0	1	1	1	1	1	1	0
		7F	127	0	1	1	1	1	1	1	1
		7C	124	0	1	1	1	1	1	0	0
		42	66	0	1	0	0	0	0	1	0
		43	67	0	1	0	0	0	0	1	1
		40	64	0	1	0	0	0	0	0	0
		41	65	0	1	0	0	0	0	0	1
		3F	63	0	0	1	1	1	1	1	1
		3E	62	0	0	1	1	1	1	1	0
		3D	61	0	0	1	1	1	1	0	1
		04	4	0	0	0	0	0	1	0	0
		03	3	0	0	0	0	0	0	1	1
		02	2	0	0	0	0	0	0	1	0
		01	1	0	0	0	0	0	0	0	1
		00	0	0	0	0	0	0	0	0	0

Row Addresses		Hex	Dec	A7	A6	A5	A4	A3	A2	A1	A0
Pin 16		7E	126	1	1	1	1	1	1	1	0
		7F	127	1	1	1	1	1	1	1	1
		FC	252	1	1	1	1	1	1	0	0
		FD	253	1	1	1	1	1	1	0	1
		FA	250	1	1	1	1	1	0	1	0
		FB	251	1	1	1	1	1	0	1	1
		F8	248	1	1	1	1	1	0	0	0
		F9	249	1	1	1	1	1	0	0	1
		C0	192	1	1	0	0	0	0	0	0
		C1	193	1	1	0	0	0	0	0	1
		BF	191	1	0	1	1	1	1	1	1
		BE	190	1	0	1	1	1	1	1	0
		83	131	1	0	0	0	0	0	1	1
		82	130	1	0	0	0	0	0	1	0
		81	129	1	0	0	0	0	0	0	1
		80	128	1	0	0	0	0	0	0	0

$$\text{Data Stored} = D_{in} \oplus A0X \oplus A1Y$$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.



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**MOTOROLA**

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Product Preview

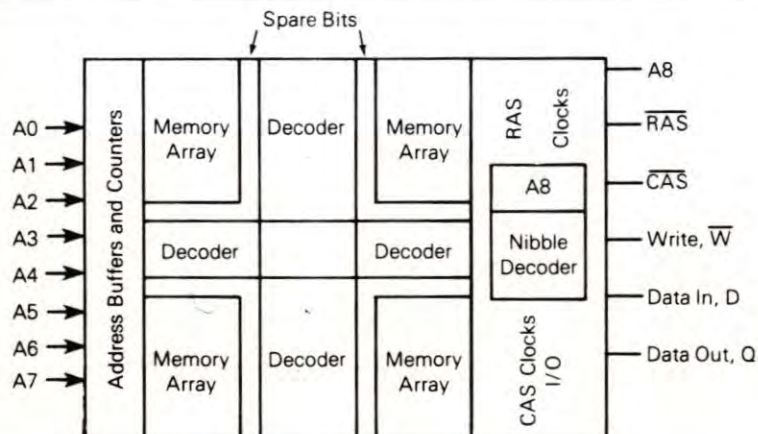
256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using laser fuse redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{\text{CAS}}$ allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{\text{RAS}}$ -only refresh mode, a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ automatic refresh is available. Another special feature of the MCM6256 is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. Nibble mode address is controlled by the addresses on pin 1 (A8 row and A8 column).

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation ($\pm 10\%$)
- Maximum Access Time:
MCM6256-10 = 100 ns
MCM6256-12 = 120 ns
MCM6256-15 = 150 ns
- Low Power Dissipation:
70 mA maximum (Active) MCM6256-10
4 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{\text{RAS}}$ -Only Refresh Mode
- Automatic ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
20 ns Access Time
40 ns Cycle Time

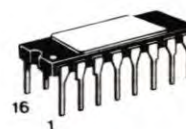


MCM6256

MOS

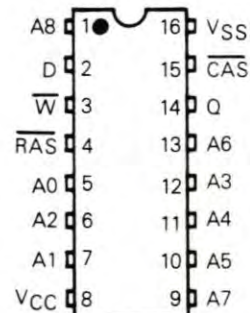
(N-CHANNEL, SILICON-GATE)

262,144 BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES

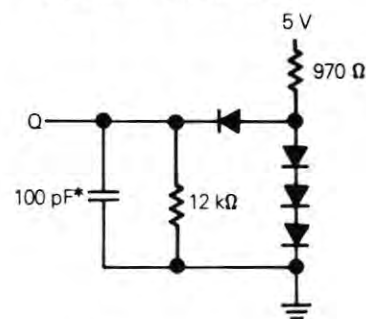
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	-2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current (Short Circuit)	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD


*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	—	$V_{CC} + 1$	V	1
Logic 0 Voltage, All Inputs	V_{IL}	-1.0*	—	0.8	V	1

*The device will withstand undershoots to the -2 volt level with a maximum pulse width of 20 ns at the -1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Output Not Loaded)					
Standby	I_{CC2}	—	4	mA	5
Standby (Data Out (Q) Enable)	I_{CC5}	—	5	mA	—
V_{CC} Power Supply Current					
MCM6256-10, $t_{RC} = 200$ ns	I_{CC1}	—	70	mA	4
MCM6256-12, $t_{RC} = 220$ ns		—	65	mA	
MCM6256-15, $t_{RC} = 260$ ns		—	55	mA	
V_{CC} Power Supply Current During \overline{RAS} only Refresh Cycles					
MCM6256-10, $t_{RC} = 200$ ns	I_{CC3}	—	50	mA	4
MCM6256-12, $t_{RC} = 220$ ns		—	46	mA	
MCM6256-15, $t_{RC} = 260$ ns		—	40	mA	
V_{CC} Power Supply Current During Automatic (\overline{CAS} Before \overline{RAS}) Refresh					
MCM6256-10, $t_{RC} = 200$ ns	I_{CC4}	—	50	mA	4
MCM6256-12, $t_{RC} = 220$ ns		—	46	mA	
MCM6256-15, $t_{RC} = 260$ ns		—	40	mA	
V_{CC} Power Supply Current During Nibble Mode					
MCM6256-10, $t_{NC} = 40$ ns at $t_{RC} = 340$ ns	I_{CC6}	—	TBD	mA	4
MCM6256-12, $t_{NC} = 50$ ns at $t_{RC} = 390$ ns					
MCM6256-15, $t_{NC} = 60$ ns at $t_{RC} = 460$ ns					
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$) (Any Input)	$I_{I(L)}$	—	10	μA	—
Output Leakage Current (\overline{CAS} at logic 1, $0 \leq V_{out} \leq 5.5$)	$I_{O(L)}$	—	10	μA	—
Output Logic 1 Voltage @ $I_{out} = -5$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out} = 4.2$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25^\circ C$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A8), D	C_{I1}	—	TBD	pF	7
Input Capacitance \overline{RAS} , \overline{WRITE}	C_{I2}	—	TBD	pF	7
Input Capacitance, \overline{CAS}	C_{I3}	—	TBD	pF	7
Output Capacitance (Q), ($\overline{CAS} = V_{IH}$ to disable output)	C_O	—	TBD	pF	7

NOTES: 1. All voltages referenced to V_{SS} .

2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .

3. An initial pause of 100 μs is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation guaranteed.



MOTOROLA Semiconductor Products Inc.

AC OPERATING CONDITIONS AND CHARACTERISTICS (Read Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted. See Notes 2, 3, 6, and Figure 1)

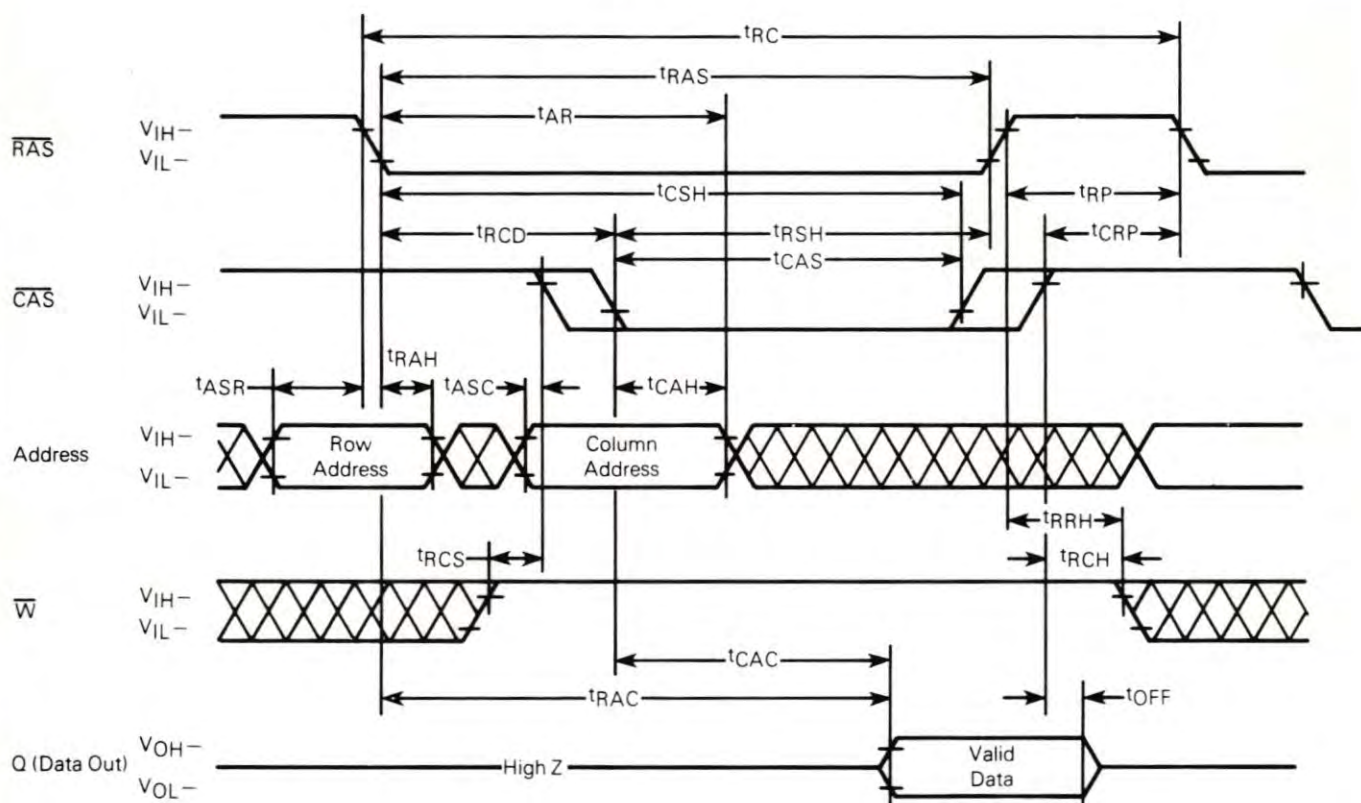
READ CYCLE

Parameter	Symbol	MCM6256-10		MCM6256-12		MCM6256-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	200	—	220	—	260	—	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	—	100	—	120	—	150	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	—	50	—	60	—	75	ns	11, 12
Row Address Strobe Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	—
Column Address Strobe Pulse Width	t_{CAS}	50	—	60	—	75	—	ns	—
Refresh Period	t_{RFSH}	—	4	—	4	—	4	ms	—
Row Address Strobe Precharge Time	t_{RP}	90	—	90	—	100	—	ns	—
Column to Row Strobe Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	—
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	60	25	75	ns	13
\overline{RAS} Hold Time	t_{RSH}	50	—	60	—	75	—	ns	—
CAS Hold Time	t_{CSH}	100	—	120	—	150	—	ns	—
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t_{RAH}	15	—	20	—	20	—	ns	—
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t_{CAH}	25	—	30	—	30	—	ns	—
Column Address Hold Time Referenced to \overline{RAS}	t_{AR}	75	—	90	—	105	—	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	2
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	—
Read Command Hold Time	t_{RCH}	TBD	—	TBD	—	TBD	—	ns	14
Read Command Hold Time Referenced to \overline{RAS}	t_{RRH}	TBD	—	TBD	—	TBD	—	ns	14
Output Buffer and Turn-Off Delay	t_{OFF}	0	25	0	30	0	30	ns	18

4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. \overline{RAS} and \overline{CAS} are both at a logic 1.
6. The transition time specification applies for input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$
8. The specifications for t_{RC} (min), t_{RWC} (min), and nibble cycle time (t_{NC}) are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$) is assured.
9. AC measurements are made with $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
11. Assumes that $t_{RCD} = t_{RCD}(\text{max})$.
12. Measured with a current load equivalent to 2 TTL ($-200 \mu\text{A}$, $+4 \text{ mA}$) loads and 100 pF ($V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.8 \text{ V}$).
13. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled by t_{CAC} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to \overline{CAS} leading edge in random write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write cycles.
16. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. $t_{RCD} + t_{CAH} \geq t_{AR}(\text{min})$, $t_{RCD} + t_{DH} \geq t_{DHR}(\text{min})$, $t_{RCD} + t_{WCH} \geq t_{WCR}(\text{min})$.
18. $t_{off}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.



READ CYCLE TIMING



AC OPERATING CONDITIONS AND CHARACTERISTICS (Write and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted. See Notes 2, 3, 6, and Figure 1)

WRITE CYCLE

Parameter	Symbol	MCM6256-10		MCM6256-12		MCM6256-15		Units	Note
		Min	Max	Min	Max	Min	Max		
WRITE Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	16
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	—
Write Command Hold Time Referenced to \overline{RAS}	t_{WCR}	85	—	100	—	120	—	ns	17
Write Command Pulse Width	t_{WP}	20	—	25	—	30	—	ns	—
Write Command to Row Strobe Lead Time	t_{RWL}	40	—	45	—	50	—	ns	—
Write Command to Column Strobe Lead Time	t_{CWL}	40	—	45	—	50	—	ns	—
Data in Setup Time	t_{DS}	0	—	0	—	0	—	ns	15
Data in Hold Time	t_{DH}	20	—	25	—	30	—	ns	15
Data In Hold Time Referenced to \overline{RAS}	t_{DHR}	85	—	100	—	120	—	ns	17

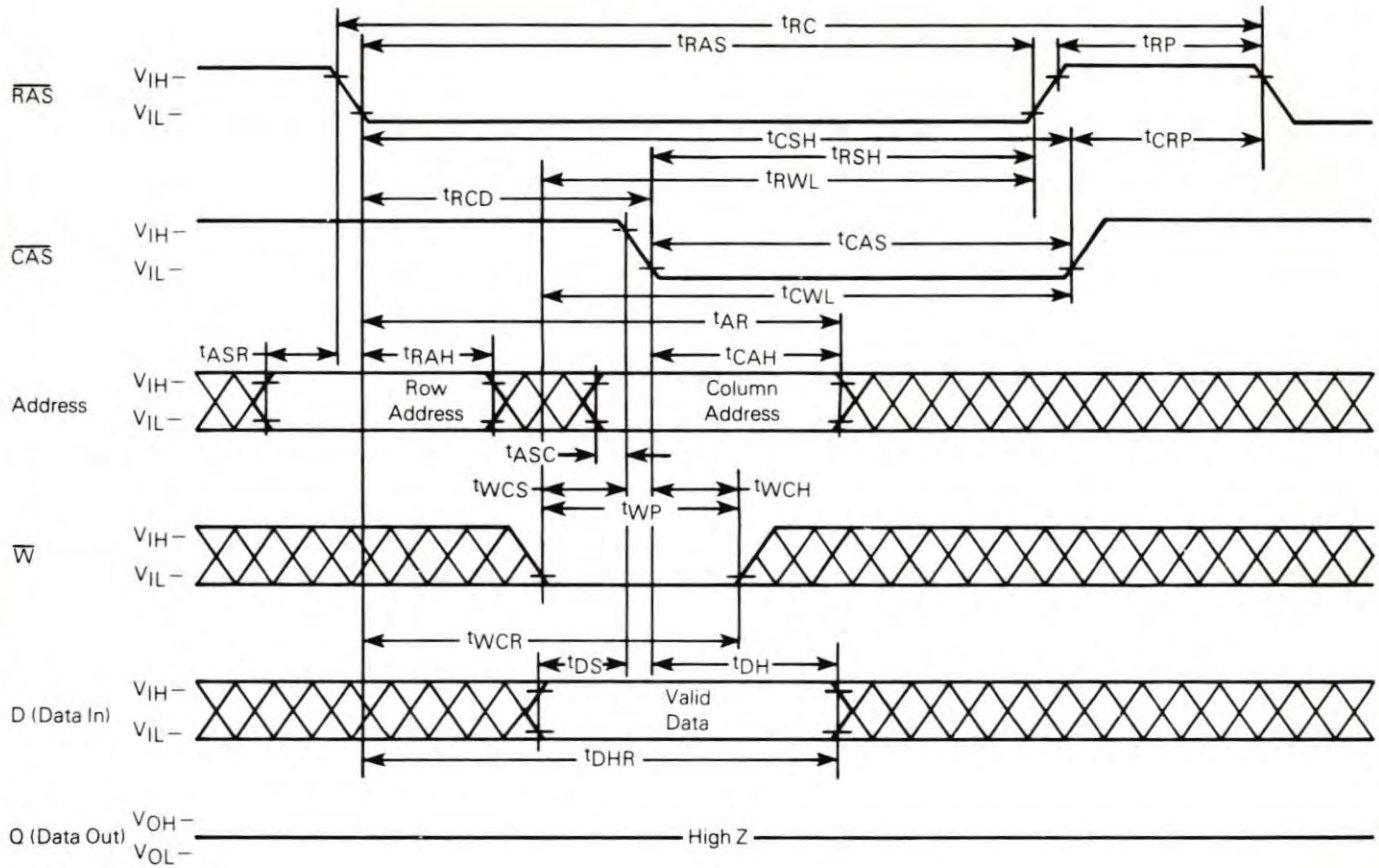
READ-MODIFY-WRITE CYCLE

Parameter	Symbol	MCM6256-10		MCM6256-12		MCM6256-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWL}	245	—	270	—	315	—	ns	8, 9
\overline{CAS} to \overline{WRITE} Delay	t_{CWD}	50	—	60	—	75	—	ns	16
\overline{RAS} to \overline{WRITE} Delay	t_{RWD}	100	—	120	—	150	—	ns	16
RMW Cycle \overline{RAS} Pulse Width	t_{RRW}	145	10000	170	10000	205	10000	ns	—
RMW Cycle \overline{CAS} Pulse Width	t_{CRW}	95	—	110	—	130	—	ns	—

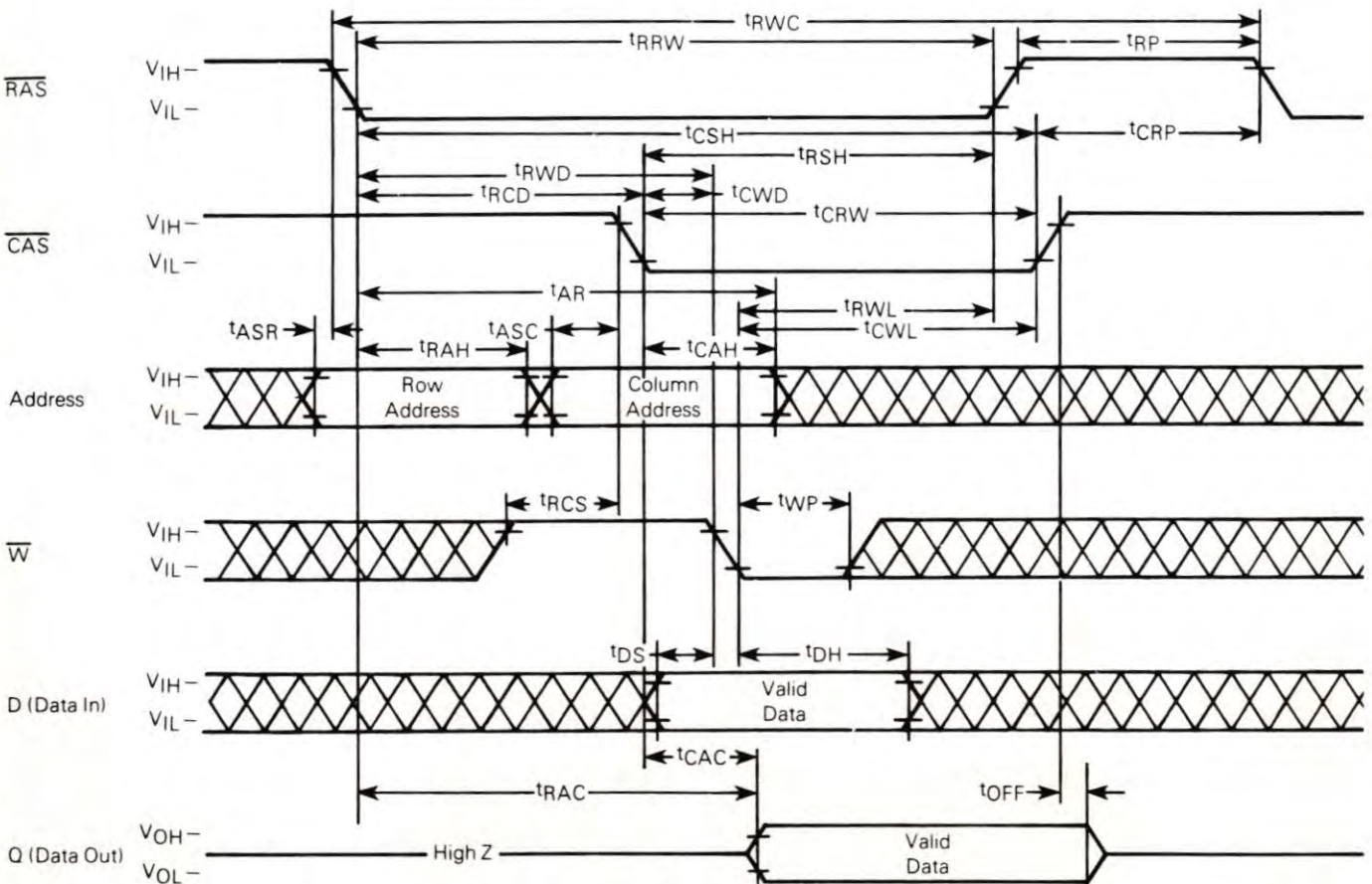


MOTOROLA Semiconductor Products Inc.

EARLY WRITE CYCLE



READ-MODIFY-WRITE OR LATE WRITE CYCLE



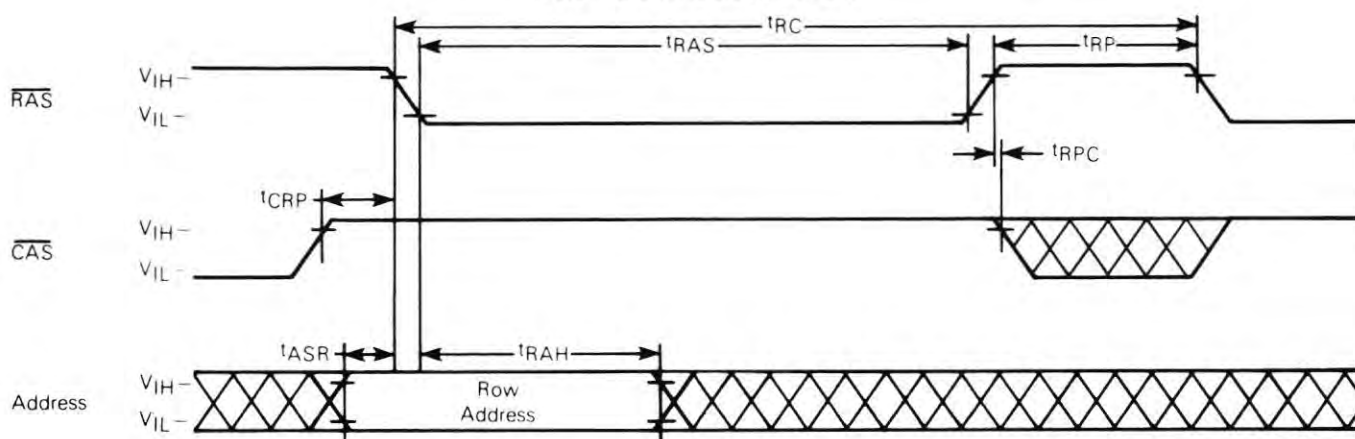
MOTOROLA Semiconductor Products Inc.

AC OPERATING CONDITIONS AND CHARACTERISTICS (Refresh Cycles)
 (Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

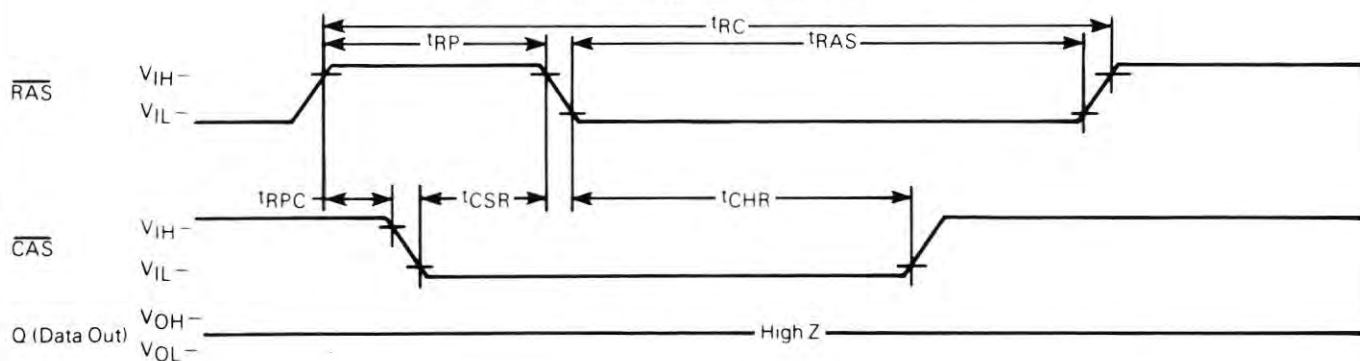
REFRESH CYCLE

Parameter	Symbol	MCM6256-10		MCM6256-12		MCM6256-15		Unit
		Min	Max	Min	Max	Min	Max	
Column Address Strobe Setup Time for Auto Refresh	t_{CSR}	10	—	10	—	10	—	ns
Column Address Strobe Hold Time for Auto Refresh	t_{CHR}	30	—	30	—	30	—	ns
Precharge to \overline{CAS} Active Time	t_{RPC}	0	—	0	—	0	—	ns

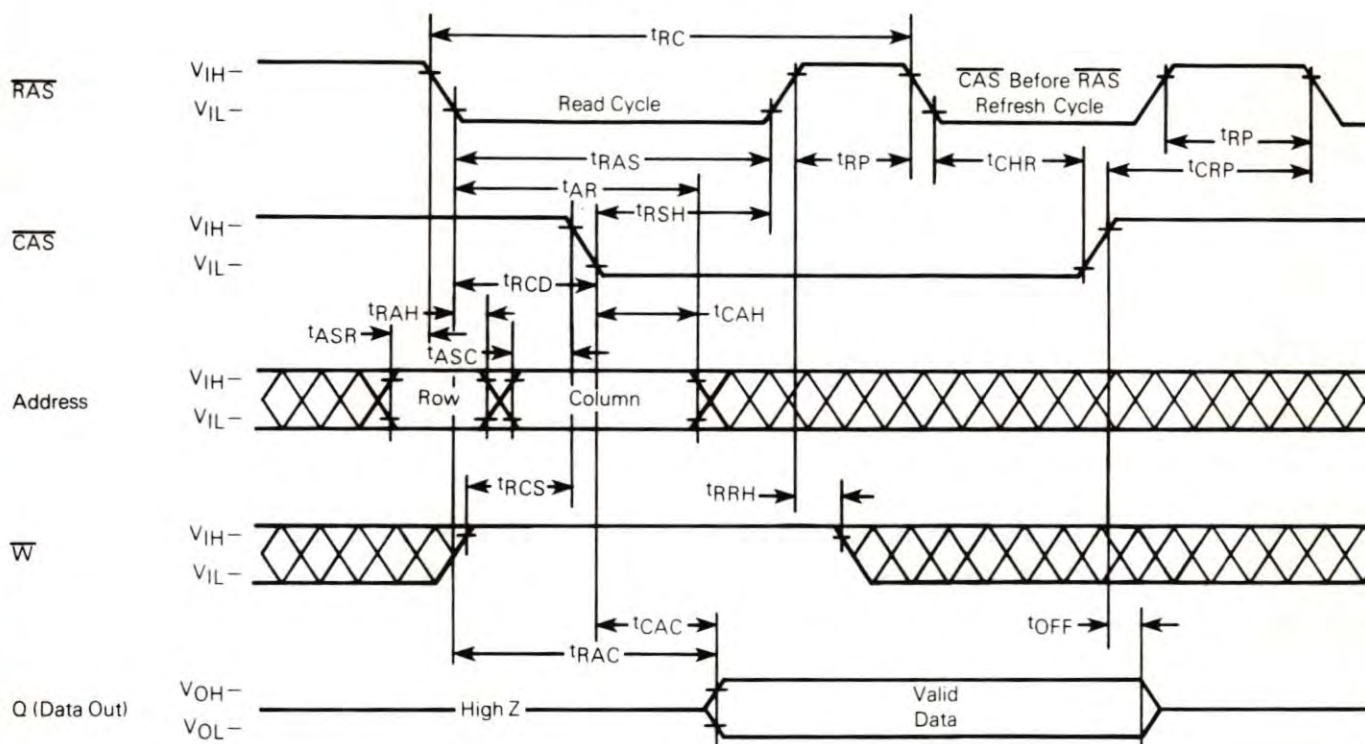
\overline{RAS} ONLY REFRESH CYCLE
 (Data-In and Write are Don't Care)



AUTOMATIC (\overline{CAS} BEFORE \overline{RAS}) REFRESH CYCLE
 (Data-In and Write are Don't Care)



HIDDEN REFRESH CYCLE



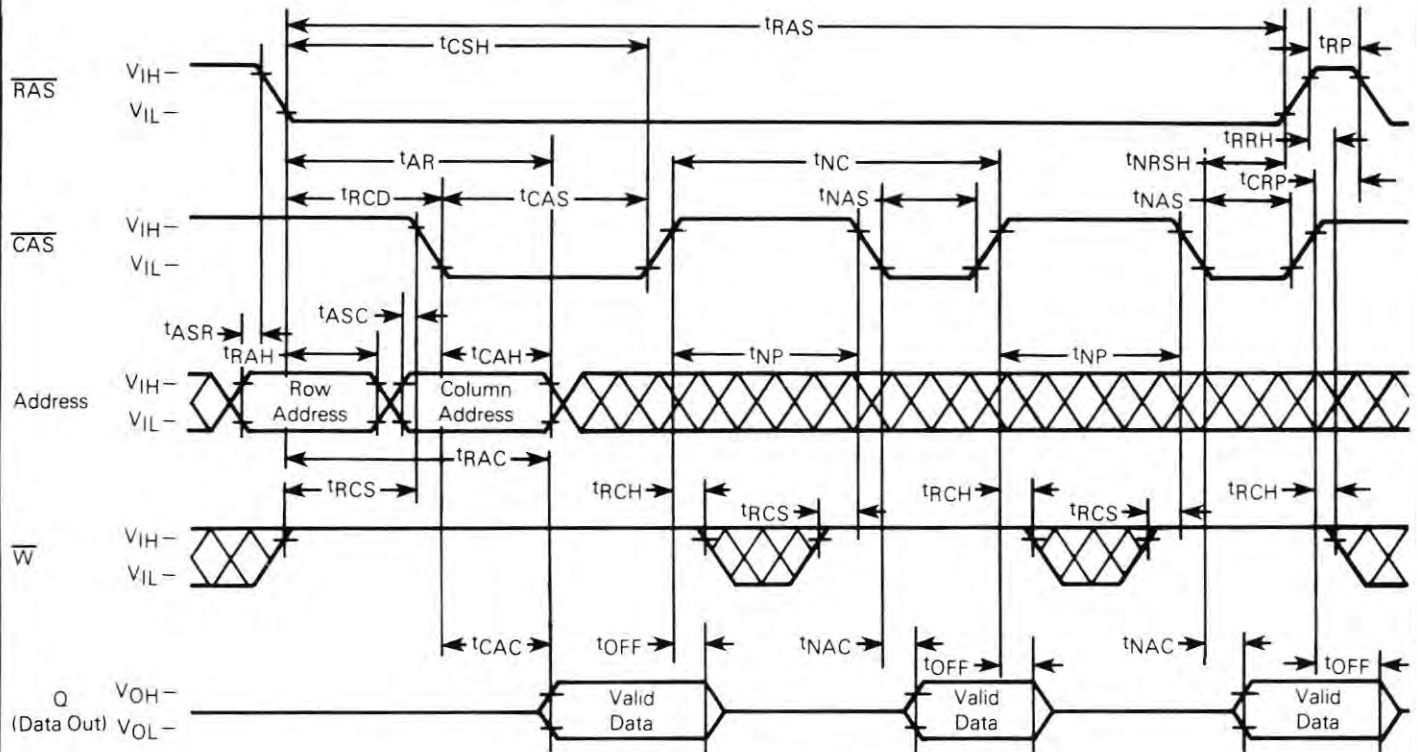
AC OPERATING CONDITIONS AND CHARACTERISTICS (Nibble Mode Cycle)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

NIBBLE MODE CYCLE

Parameter	Symbol	MCM6256-10		MCM6256-12		MCM6256-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Nibble Mode Cycle Time	t_{NC}	40	—	50	—	60	—	ns	8, 9
Nibble Mode Access Time	t_{NAC}	20	—	25	—	30	—	ns	12
Nibble Mode Setup Time	t_{NAS}	20	—	25	—	30	—	ns	—
Nibble Mode Precharge Time	t_{NP}	10	—	15	—	20	—	ns	—
Nibble Mode \overline{RAS} Hold Time	t_{NRSH}	20	—	25	—	30	—	ns	—
Nibble Mode \overline{CAS} to \overline{WRITE} Delay	t_{NCWD}	20	—	25	—	30	—	ns	—
Nibble Mode RMW \overline{CAS} Pulse Width	t_{NCRW}	45	—	55	—	65	—	ns	—
Nibble Mode \overline{WRITE} to \overline{CAS} Lead Time	t_{NCWL}	20	—	25	—	30	—	ns	—
Nibble Mode Write \overline{RAS} Hold Time	t_{NWRH}	40	—	45	—	55	—	ns	—

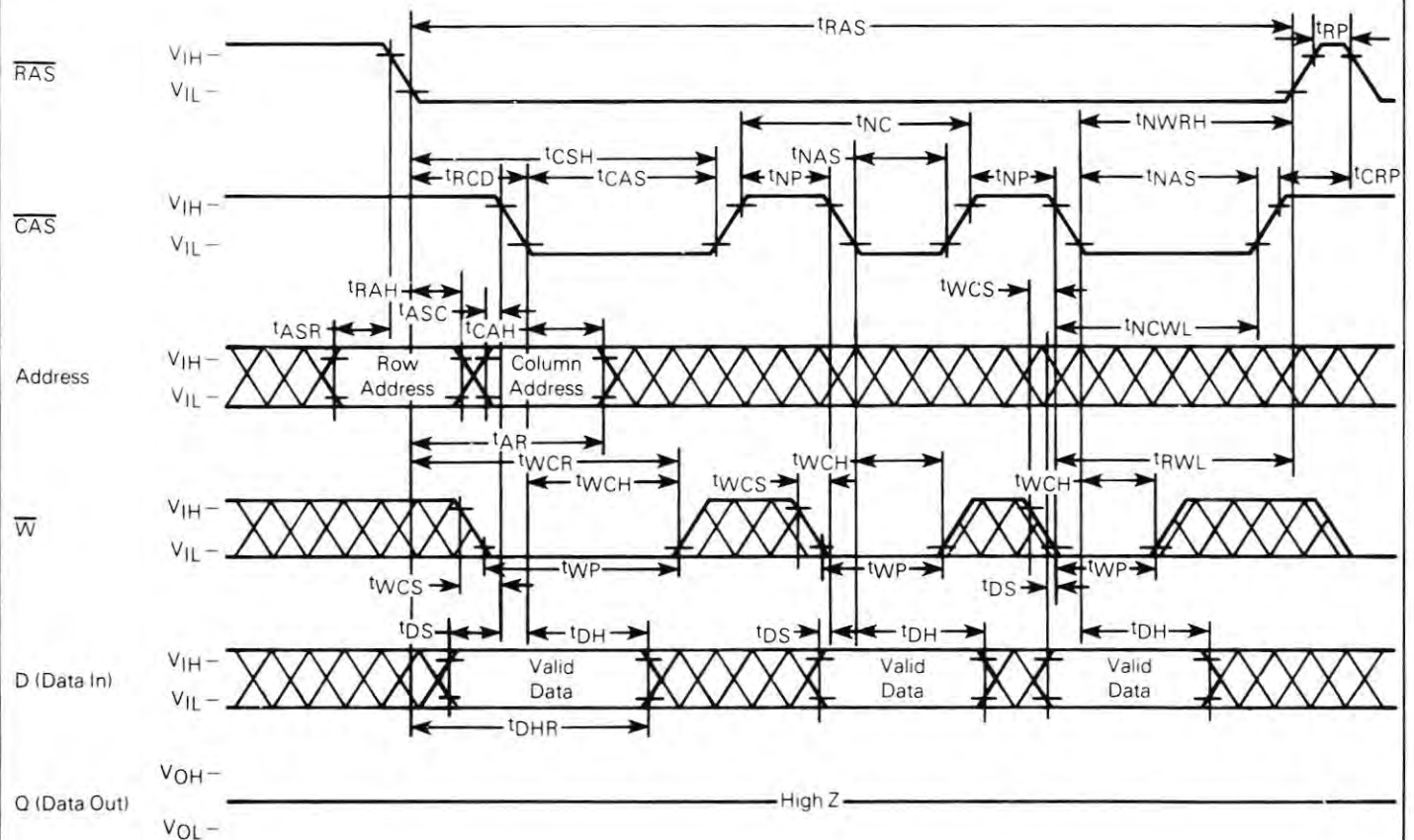


NIBBLE MODE READ CYCLE*



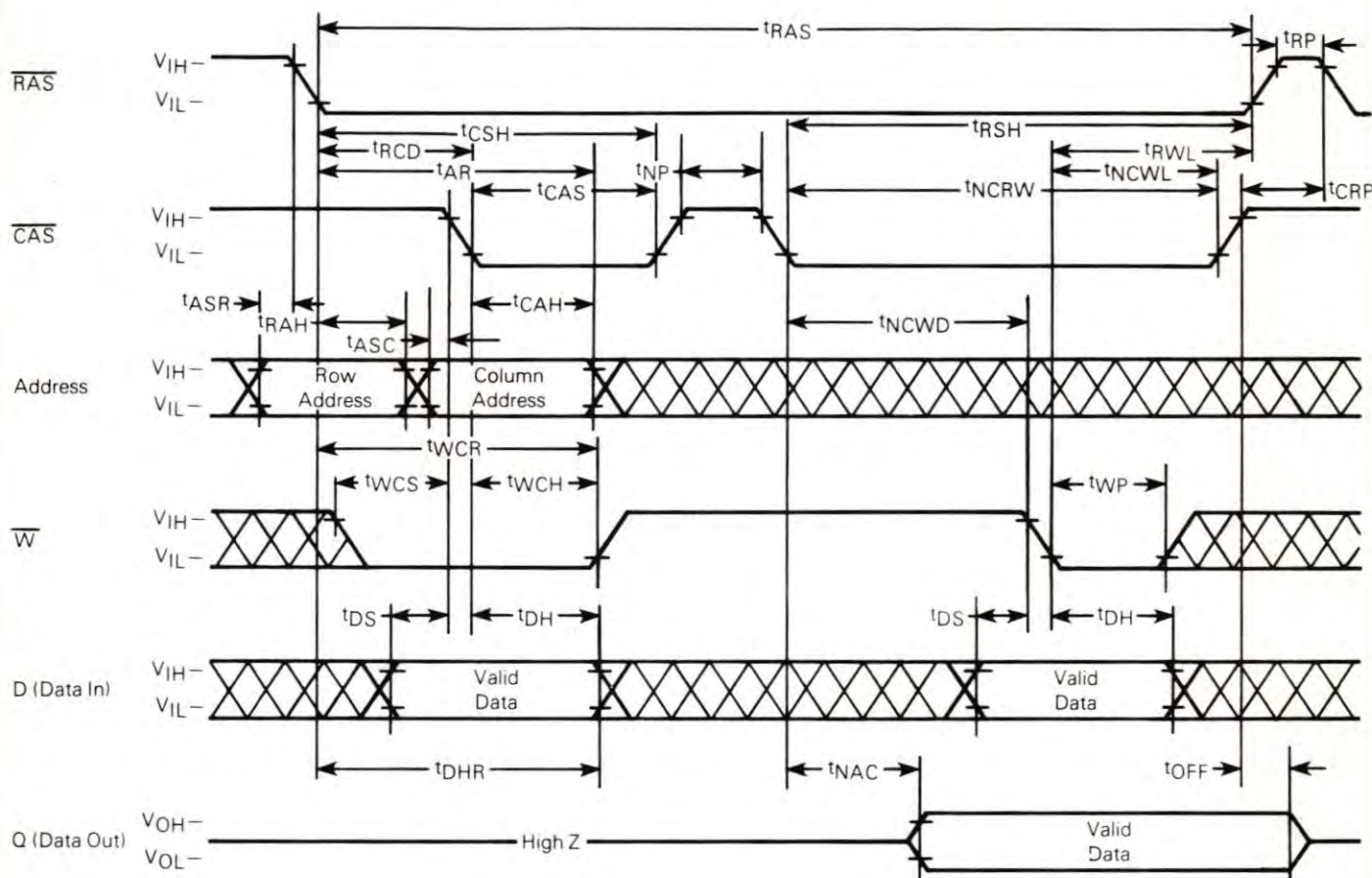
*Pin 1 at Row Time and Column Time Determine the Starting Address of the Nibble Cycle.

NIBBLE MODE WRITE CYCLE (EARLY WRITE)



MOTOROLA Semiconductor Products Inc.

NIBBLE MODE READ-MODIFY-WRITE



DEVICE INITIALIZATION

Since the 256K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "tRCD," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the RAS only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the RAS clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called nibble mode, allows the user to address 4 bits of data (serially) at a very high data rate.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a nibble mode read cycle, a read-while-



cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{\text{RAS}}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{\text{CAS}}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{\text{CAS}}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{\text{RAS}}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{\text{CAS}}$ clock active transition will determine read access time. The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gating feature on the $\overline{\text{CAS}}$ clock will allow the external $\overline{\text{CAS}}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{\text{RAS}}$ clock and the minimum (t_{CAS}) period for the $\overline{\text{CAS}}$ clock. The $\overline{\text{RAS}}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{\text{CAS}}$ clock is active; the output will switch to the three-state mode when the $\overline{\text{CAS}}$ clock goes inactive. To perform a read cycle, the write ($\overline{\text{W}}$) input must be held at the V_{IH} level from the time the $\overline{\text{CAS}}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{\text{W}}$) clock must go active (V_{IL} level) at or before the $\overline{\text{CAS}}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{\text{CAS}}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks need to be active after the write operation has started ($\overline{\text{W}}$) clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{\text{CAS}}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late

write cycle is that in a late write cycle the write ($\overline{\text{W}}$) clock can occur much later in time with respect to the active transition of the $\overline{\text{CAS}}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_i]$.

At the start of an early write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because of the active transition of the write ($\overline{\text{W}}$) clock prevents the $\overline{\text{CAS}}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{\text{W}}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{\text{W}}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD} , t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{\text{W}}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assure that data out does occur. In this case, the data in is set up with respect to write ($\overline{\text{W}}$) clock active edge.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 ms. This is accomplished by sequentially cycling through the 256 row address locations every 4 ms (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with that particular row decoded.

$\overline{\text{RAS}}$ -Only Refresh — One method to ensure data retention is to employ the $\overline{\text{RAS}}$ -only refresh scheme. In this refresh method, the system must perform a $\overline{\text{RAS}}$ -only cycle on all 256 row addresses every 4 ms. The row addresses are latched with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and must be inactive or at a V_{IH} level.



AUTOMATIC ($\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$) REFRESH

This refresh cycle is initiated when $\overline{\text{RAS}}$ falls, after $\overline{\text{CAS}}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{\text{CAS}}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{\text{CAS}}$ is held active (hidden refresh).

NIBBLE MODE CYCLES

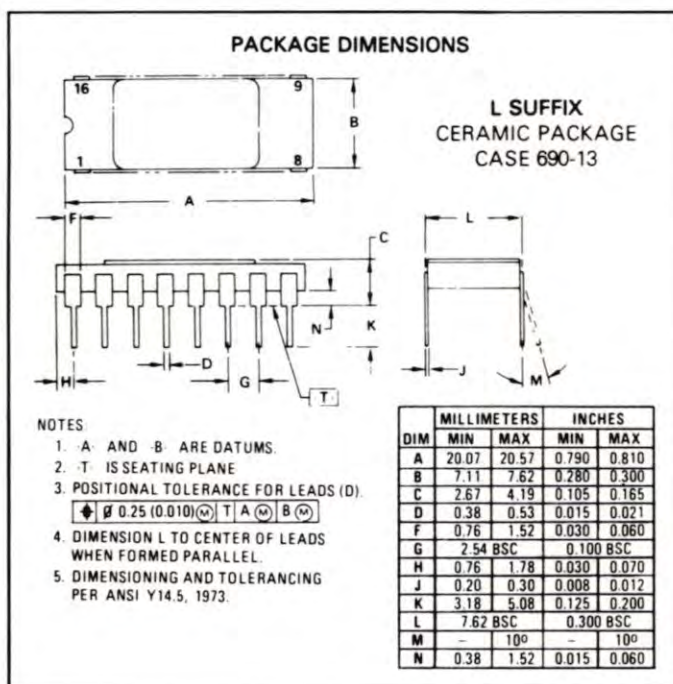
Nibble Mode Operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ can be cycled up and then down, to read or

write the next three pages at a high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycle. From then on, the falling edge of $\overline{\text{CAS}}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).

→[0,0]→[0,1]→[1,0]→[1,1]→

Pin one (A8) determines the starting point of the circular 4-bit nibble. Row A8 and Column A8 provide the two binary bits needed to select one of four bits. The user can start the nibble mode at any one of the four bits, from then on, successive bits come out in a binary fashion; 00→01→10→11 with Row A8 being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{\text{RAS}}$ is kept low.



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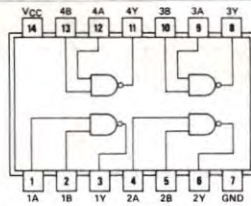
E-77

NP-352

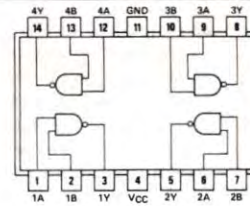
**QUADRUPLE 2-INPUT
POSITIVE-NAND GATES**

00

positive logic:
 $Y = \overline{AB}$



SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)

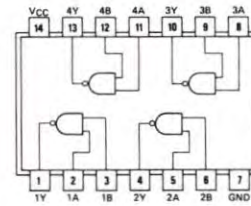


SN5400 (W)
SN54H00 (W)
SN54L00 (T)

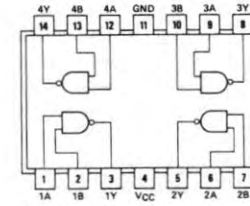
**QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS**

01

positive logic:
 $Y = \overline{AB}$



SN5401 (J) SN7401 (J, N)
SN54LS01 (J, W) SN74LS01 (J, N)

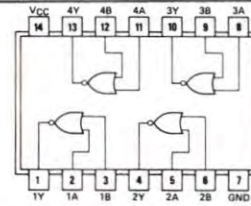


SN5401 (W)
SN54H01 (W)
SN54L01 (T)

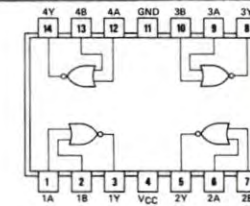
**QUADRUPLE 2-INPUT
POSITIVE-NOR GATES**

02

positive logic:
 $Y = \overline{A+B}$



SN5402 (J) SN7402 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)



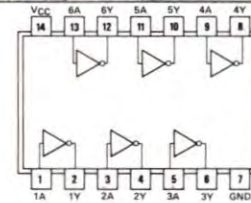
SN5402 (W)
SN54L02 (T)

See page 6-8

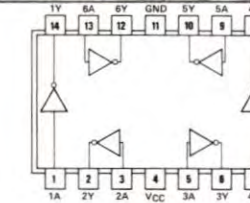
HEX INVERTERS

04

positive logic:
 $Y = \overline{A}$



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)

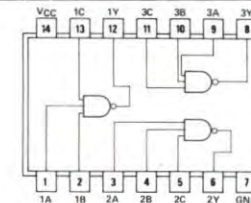


SN5404 (W)
SN54H04 (W)
SN54L04 (T)

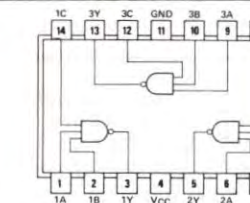
**TRIPLE 3-INPUT
POSITIVE-NAND GATES**

10

positive logic:
 $Y = \overline{ABC}$



SN5410 (J) SN7410 (J, N)
SN54H10 (J) SN74H10 (J, N)
SN54L10 (J) SN74L10 (J, N)
SN54LS10 (J, W) SN74LS10 (J, N)
SN54S10 (J, W) SN74S10 (J, N)

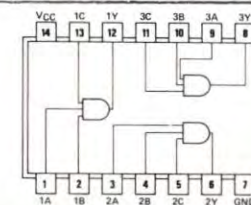


SN5410 (W)
SN54H10 (W)
SN54L10 (T)

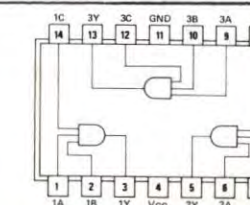
**TRIPLE 3-INPUT
POSITIVE-AND GATES**

11

positive logic:
 $Y = ABC$



SN54H11 (J) SN74H11 (J, N)
SN54LS11 (J, W) SN74LS11 (J, N)
SN54S11 (J, W) SN74S11 (J, N)

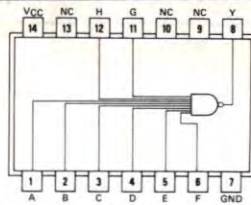


SN54H11 (W)

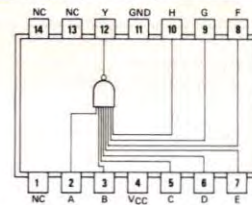
8-INPUT POSITIVE-NAND GATES

30

positive logic:
 $Y = ABCDEFGH$



SN5430 (J) SN7430 (J, N)
SN54H30 (J) SN74H30 (J, N)
SN54L30 (J) SN74L30 (J, N)
SN54LS30 (J, W) SN74LS30 (J, N)
SN54S30 (J, W) SN74S30 (J, N)



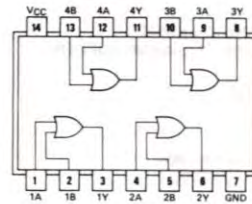
SN5430 (W)
SN54H30 (W)
SN54L30 (T)

NC—No internal connection

QUADRUPLE 2-INPUT POSITIVE-OR GATES

32

positive logic:
 $Y = A + B$



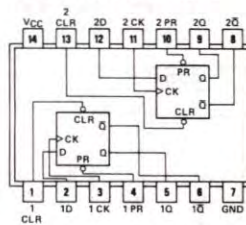
SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

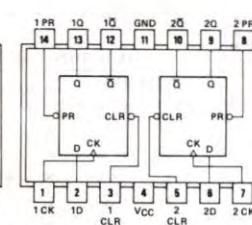
74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0



SN5474 (J) SN7474 (J, N)
SN54H74 (J) SN74H74 (J, N)
SN54L74 (J) SN74L74 (J, N)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)



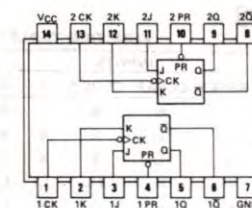
SN5474 (W)
SN54H74 (W)
SN54L74 (T)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

113

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	H	L
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	\bar{Q}_0

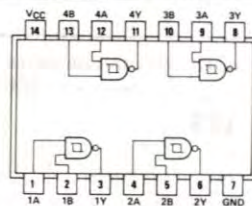


SN54LS113A (J, W) SN74LS113A (J, N)
SN54S113 (J, W) SN74S113 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

132

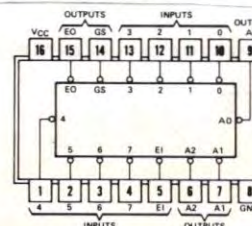
positive logic:
 $Y = \overline{AB}$



SN54132 (J, W) SN74132 (J, N)
SN54LS132 (J, W) SN74LS132 (J, N)
SN54S132 (J, W) SN74S132 (J, N)

8-LINE-TO-3-LINE OCTAL PRIORITY ENCODERS

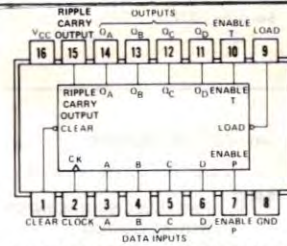
148



SN54148 (J, W) SN74148 (J, N)
SN54LS148 (J, W) SN74LS148 (J, N)

SYNCHRONOUS 4-BIT COUNTERS

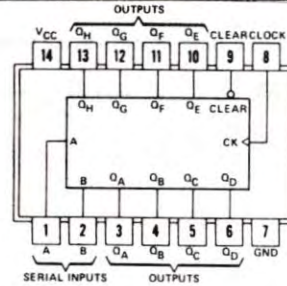
- 160** DECADE, DIRECT CLEAR
- 161** BINARY, DIRECT CLEAR
- 162** DECADE, SYNCHRONOUS CLEAR
- 163** BINARY, SYNCHRONOUS CLEAR



SN54160 (J, W)	SN74160 (J, N)
SN54LS160A (J, W)	SN74LS160A (J, N)
SN54161 (J, W)	SN74161 (J, N)
SN54LS161A (J, W)	SN74LS161A (J, N)
SN54162 (J, W)	SN74162 (J, N)
SN54LS162A (J, W)	SN74LS162A (J, N)
SN54S162 (J, W)	SN74S162 (J, N)
SN54163 (J, W)	SN74163 (J, N)
SN54LS163A (J, W)	SN74LS163A (J, N)
SN54S163 (J, W)	SN74S163 (J, N)

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS

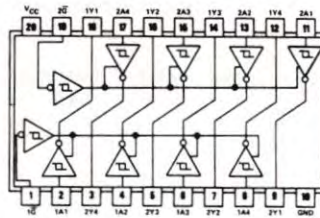
- 164** ASYNCHRONOUS CLEAR



SN54164 (J, W)	SN74164 (J, N)
SN54L164 (J, T)	SN74L164 (J, N)
SN54LS164 (J, W)	SN74LS164 (J, N)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

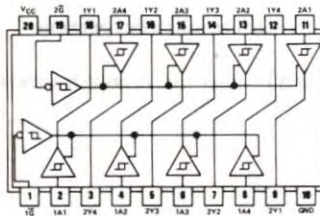
- 240** INVERTED 3-STATE OUTPUTS



SN54LS240 (J)	SN74LS240 (J, N)
SN54S240 (J)	SN74S240 (J, N)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

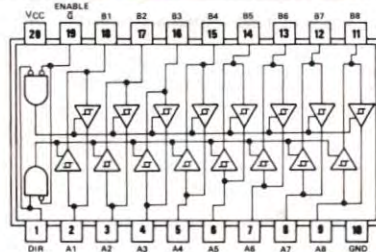
- 244** NONINVERTED 3-STATE OUTPUTS



SN54LS244 (J)	SN74LS244 (J, N)
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OCTAL BUS TRANCEIVERS

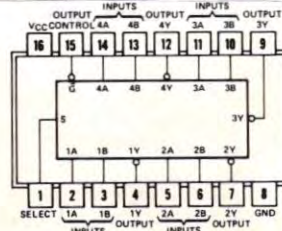
- 245** NONINVERTED 3-STATE OUTPUTS



SN54LS245 (J)	SN74LS245 (J, N)
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QUAD DATA SELECTORS/MULTIPLEXERS

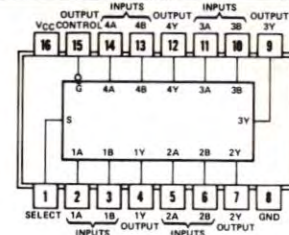
- 258** INVERTED 3-STATE OUTPUTS



SN54LS258A (J, W)	SN74LS258A (J, N)
SN54S258 (J, W)	SN74S258 (J, N)

QUAD DATA SELECTORS/MULTIPLEXERS

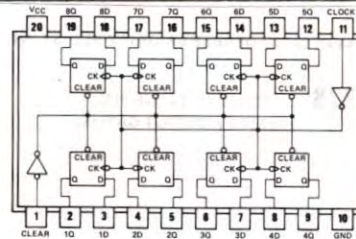
257 NONINVERTED 3-STATE OUTPUTS



SN54LS257A (J, W) SN74LS257A (J, N)
SN54S257 (J, W) SN74S257 (J, N)

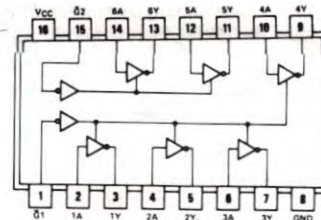
OCTAL D-TYPE FLIP-FLOPS

273 COMMON CLOCK SINGLE-RAIL OUTPUTS



SN54273 (J) SN74273 (J, N)
SN54LS273 (J) SN74LS273 (J, N)

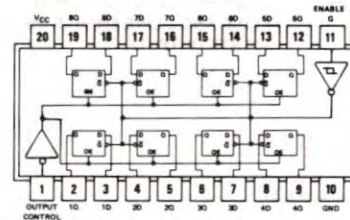
368 INVERTED DATA OUTPUTS 4-LINE AND 2-LINE ENABLE INPUTS 3-STATE OUTPUTS



SN54368A (J, W) SN74368A (J, N)
SN54LS368A (J, W) SN74LS368A (J, N)

OCTAL D-TYPE LATCHES

373 3-STATE OUTPUTS COMMON OUTPUT CONTROL COMMON ENABLE



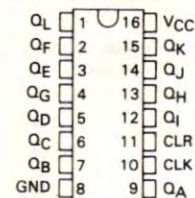
SN54LS373 (J) SN74LS373 (J, N)
SN54S373 (J) SN74S373 (J, N)

4040

description

This device is an asynchronous 12-stage binary counter with the outputs of all stages available externally. A high level at CLR asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at CLK.

SN74HC4040 ... J OR N PACKAGE (TOP VIEW)



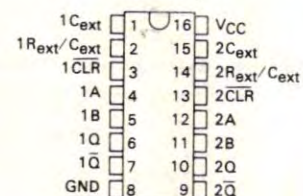
4538

DUAL PRECISION MONOSTABLE

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	L	L	H
H	L	H	L	H

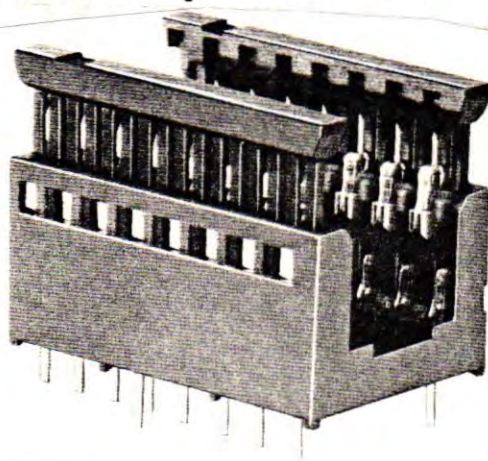
SN74HC4538 ... J OR N PACKAGE (TOP VIEW)



16-POSITION STACKED DIP SOCKET

For 4K, 16K, and 64K Dynamic RAMS

Patents Pending
Patents Approved



CAM actuated LIF socket

The contacts of the Stacked DIP Socket are cam operated, which significantly lowers IC insertion forces (ICs are installed using a standard insertion/extraction tool). The operating cam has three distinct positions:

Position #1 is "cam up," which disengages the upper and lower contacts, allowing insertion or extraction of either IC. Position #2 engages the lower contacts. In this position the upper IC may be inserted or extracted without affecting the electrical integrity of the lower IC. Position #3 is "cam down," which engages both the upper and lower IC packages.

The upper IC package is supported in the Stacked DIP Socket by mounting clips that serve several functions. They provide a means of supporting the leads of the upper IC against the normal forces of the upper contacts, while at the same time providing positive clearance for air flow over the lower IC package.

If maximum clearance between the upper and lower packages is desired, the leads of the lower device should be trimmed to a length of .100"-.125" from the seating plane of the package. The sockets have the flexibility to accept packages with leads as short as .100" and as long as .150", on centers of .300" \pm .010" (16, 18, 20 pin sockets) or .600" \pm .010" (24 and 28 pin sockets).

Memory isolation—16 position

In the 16-position Stacked DIP Sockets for Dynamic RAMs, the upper IC can be selected independently of the lower IC through the use of independent contacts for the upper and lower Row Address Strobe (RAS) and upper and lower Column Address Strobe (CAS). In standard configurations, RAS is pin #4 and CAS is pin #15. All other contacts are electrically paralleled.

Design

- Stack two 16-position Dynamic RAMs, one above the other
- Upper IC RAS (pin #4) and CAS (pin #15) electrically isolated from lower IC RAS and CAS
- Cam operated; low insertion and extraction forces
- Positive mechanical stop ensures air flow over lower IC
- Low profile, cost saving, double packaging capacity
- Integral decoupling capacitor circuit lowers power supply noise (optional)

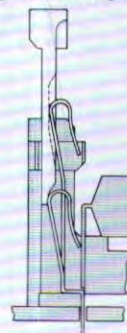
Performance

- | | |
|---|--|
| • Contact Resistance (Avg.): | Upper contact—
6.0 milliohm
Lower contact—
4.5 milliohm |
| • Capacitance—
Pin to Pin (Avg.): | 1 pf. |
| • Dielectric Strength: | 1000 VDC (sea level) |
| • Operating Temperature:
(without capacitor circuit) | –55°C to 105°C
(U.L. approved to 105°C) |
| (with capacitor circuit) | +10°C to 85°C |
| • Insertion Force (Avg.): | 2.4 lbs. with cams up |
| • Flammability Rating: | 94 V-0 |

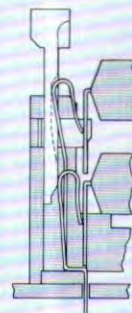
Materials

- | | |
|------------------|--|
| • Insulation: | Glass reinforced thermoplastic |
| • Contacts: | Beryllium copper, plated with 150 μ in. tin over 50 μ in. nickel |
| • Mounting Clip: | Brass |

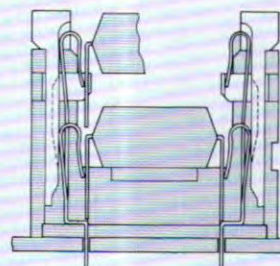
Principle of Operation



POSITION #1
Cam up



POSITION #2
Engages the lower contacts.



POSITION #3
Cam down

THOMAS & BETTS CORPORATION

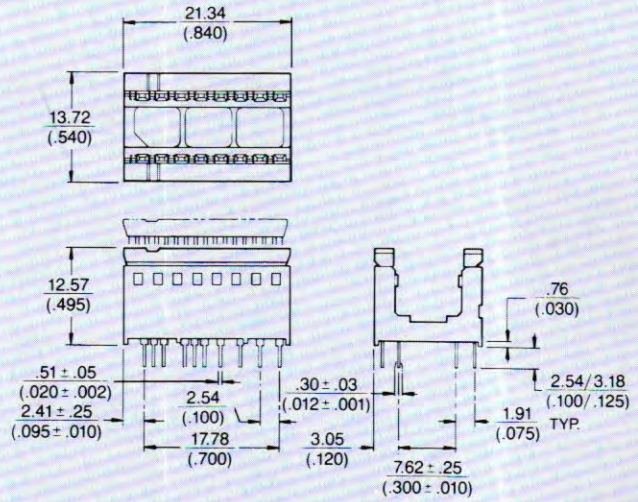
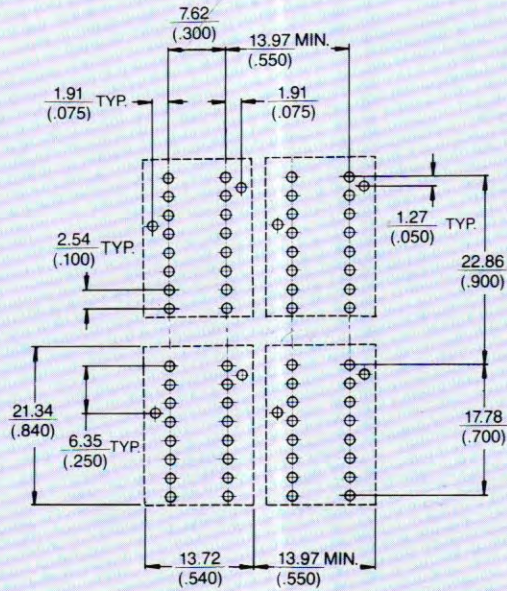
Ansley Electronics Division

920 Route 202 • Raritan, N.J. 08869
(201) 469-4000 • Telex 844-372
In Canada: Electronics Division,
Thomas & Betts, Ltd., P.O. Box 30,
Iberville, Quebec J2X 2M9 • (514) 878-9601

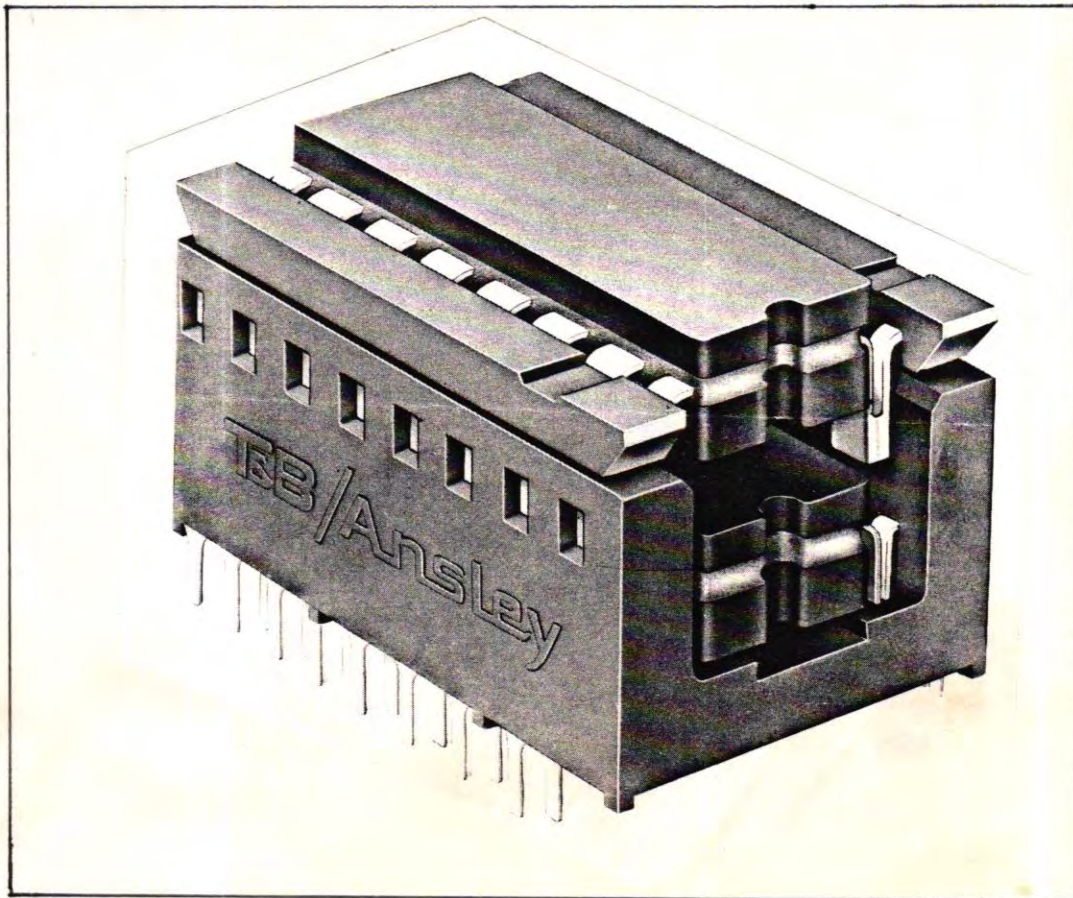
This information provided courtesy of Ansley Electronics Div., T & B Corp.

Recommended Hole Pattern

Dimensions are shown in $\frac{\text{MM}}{\text{inches}}$



Hole Diameters .038" \pm .003" All tolerances \pm .005" unless noted



APPENDIX F

H-1000 MEMORY EXPANSION CONNECTOR

P501

Ground - 1	*	*	11 - Ground
D0 - 2	*	*	12 - D8
D1 - 3	*	*	13 - D9
D2 - 4	*	*	14 - D10
D3 - 5	*	*	15 - D11
D4 - 6	*	*	16 - D12
D5 - 7	*	*	17 - D13
D6 - 8	*	*	18 - D14
D7 - 9	*	*	19 - D15
Ground - 10	*	*	20 - Ground

P507

+5vdc - 1	*	*	26 - +5vdc
Ground - 2	*	*	27 - Ground
A0 - 3	*	*	28 - A13
A1 - 4	*	*	29 - A14
A2 - 5	*	*	30 - A15
A3 - 6	*	*	31 - A16
A4 - 7	*	*	32 - A19
A5 - 8	*	*	33 - A18
A6 - 9	*	*	34 - A17
A7 - 10	*	*	35 - /A0
A8 - 11	*	*	36 - /MEMDIS (Memory Disable)
A9 - 12	*	*	37 - /RESET
A10 - 13	*	*	38 - /HALT
A11 - 14	*	*	39 - /BMREQ (Memory Request)
A12 - 15	*	*	40 - /BIORQ (I/O Request)
MEM0 - 16	*	*	41 - /BWR (Write Request)
MEM1 - 17	*	*	42 - /BRD (Read Request)
/RD5 - 18	*	*	43 - HALTA (Halt Acknowledge)
/RD6 - 19	*	*	44 - 8 MHZ CLOCK
/RD7 - 20	*	*	45 - /RFSH (Refresh Request)
+12vdc - 21	*	*	46 - +12vdc
-12vdc - 22	*	*	47 - -12vdc
+5vdc - 23	*	*	48 - +5vdc
+12vdc - 24	*	*	49 - +12vdc
Ground - 25	*	*	50 - Ground

APPENDIX G

SUGGESTED READING

The following publications are suggested if you would like to learn more about programming the H-1000, or how the H-1000 works. They are available at most good electronics or computer stores, or can be ordered by mail.

The 8086 Book by Russel Rector and George Alexy, from
Osborne/McGraw-Hill, Berkeley CA.

iAPX86,88 User Manual by Intel Corporation, Literature Department,
3065 Bowers Avenue, Santa Clara CA 95051.

Microprocessor and Peripheral Handbook by Intel Corporation,
Literature Department, 3065 Bowers Avenue, Santa Clara, CA
95051.

Z80 Programming for Logic Design by Adam Osborne et.al.,
Osborne/McGraw-Hill, Berkeley CA.

Z80 Programming Manual from Mostek Corporation, Carrolton TX.

The TTL Data Book for Design Engineers by Texas Instruments Inc.,
Dallas TX.

1981 Supplement to the TTL Data Book by Texas Instruments Inc.,
Dallas TX.