Z80 Wait State Experiments on H8 Bus

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All tests run using the MicroTran Fortran-80 Math Library Test Program (TIME.ABS)
HDOS 2.0, 64K, H8 bus populated as shown at right
Memory Wait States tested using 64K RAM on the bus, located in card slot immediately behind the Z80 v4 CPU
One-Shot Wait State Generator adjusted for minimum wait time to support stable operation at 16MHz
Memory Delay: 200ns (for M1, MemRD, MemWR cycles)
I/O Delay: 650ns (for IORD, IOWR cycles)

H8 Bus Population

1	Z80 v4 CPU
2	64K RAM (only for memory wait state tests)
3	H8-4 Serial Card
4	(open)
5	Wait State Generator proto mini-card
6	82C55 Parallel I/O Card
7	(open)
8	H17/37/67 Storage Controller Card

CPU Speed	Memory Plus I/O Waits	I/O Waits	No Waits
2MHz	62.08	62.08	62
	24.46	24.48	24.44
4MHz	29.76	27.14	27.1
	11.76	10.68	10.68
8MHz	15.96	12.76	12.74
	6.28	5.02	5.02
10MHz	13.84	10.32	10.32
	5.46	4.08	4.06
16MHz	11.14	6.18	FAIL
	4.38	2.42	FAIL

e^x

	2	4	8	10	16
Memory+I/O Waits	62.08	29.76	15.96	13.84	11.14
I/O Waits Only	62.08	27.14	12.76	10.32	6.18
No Waits	62	27.1	12.74	10.32	FAIL
Linear	49.44	24.72	12.36	9.888	6.18

ATAN(x)

	2	4	8	10	16
Memory + I/O Waits	24.46	11.76	6.28	5.46	4.38
I/O Waits Only	24.48	10.68	5.02	4.08	2.42
No Waits	24.44	10.68	5.02	4.06	FAIL
Linear	19.36	9.68	4.84	3.872	2.42