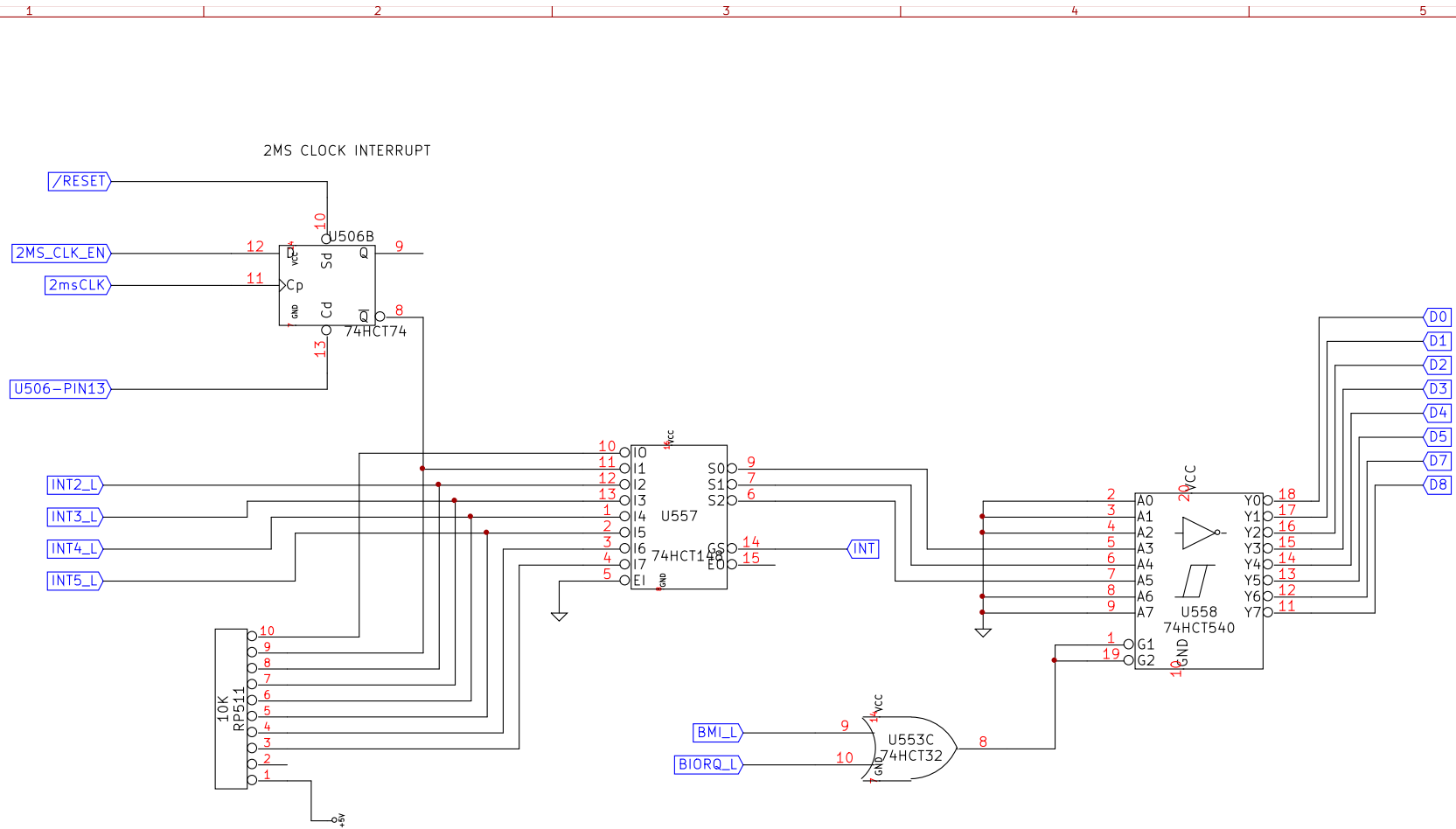
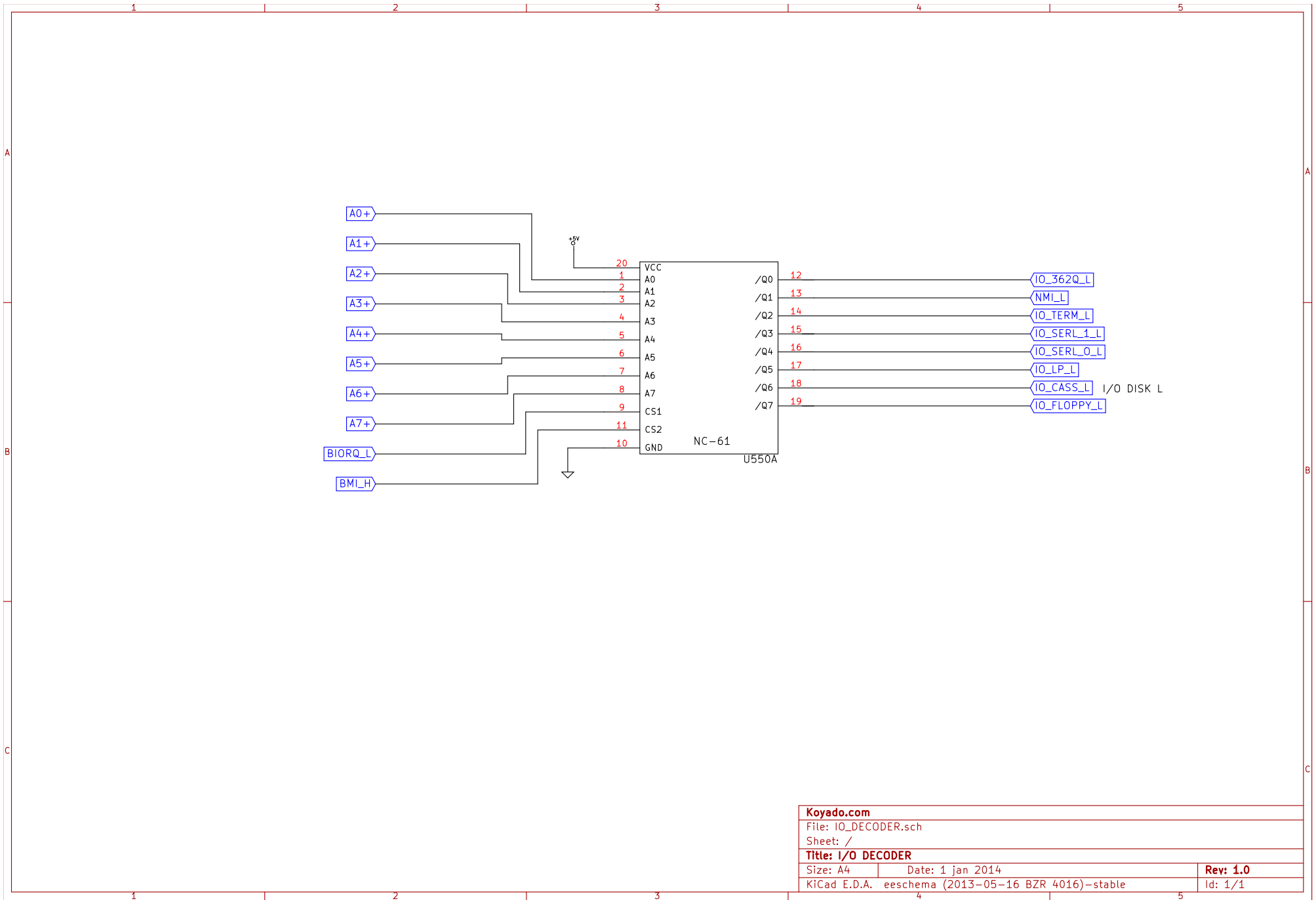


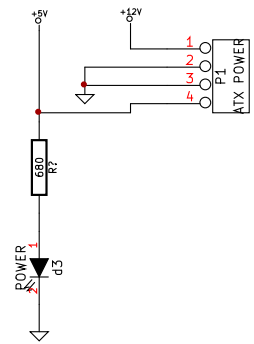
<b>Koyado.com</b>		
File: CONSOLE_SERIAL_PORT.sch		
Sheet: /		
<b>Title: CONSOLE SERIAL PORT</b>		
Size: A4	Date: 1 jan 2014	Rev: 1.0
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1



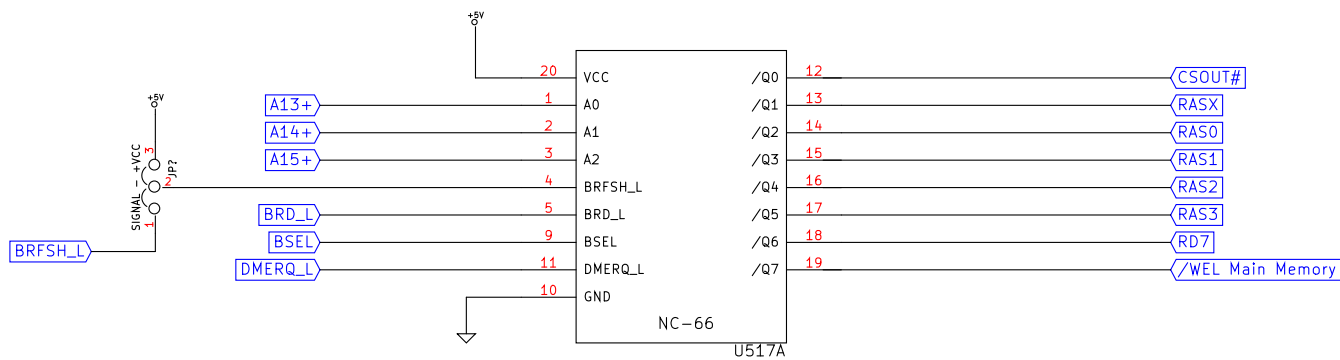
INTERRUPTS



<b>Koyado.com</b>		
File: IO_DECODER.sch		
Sheet: /		
<b>Title: I/O DECODER</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1

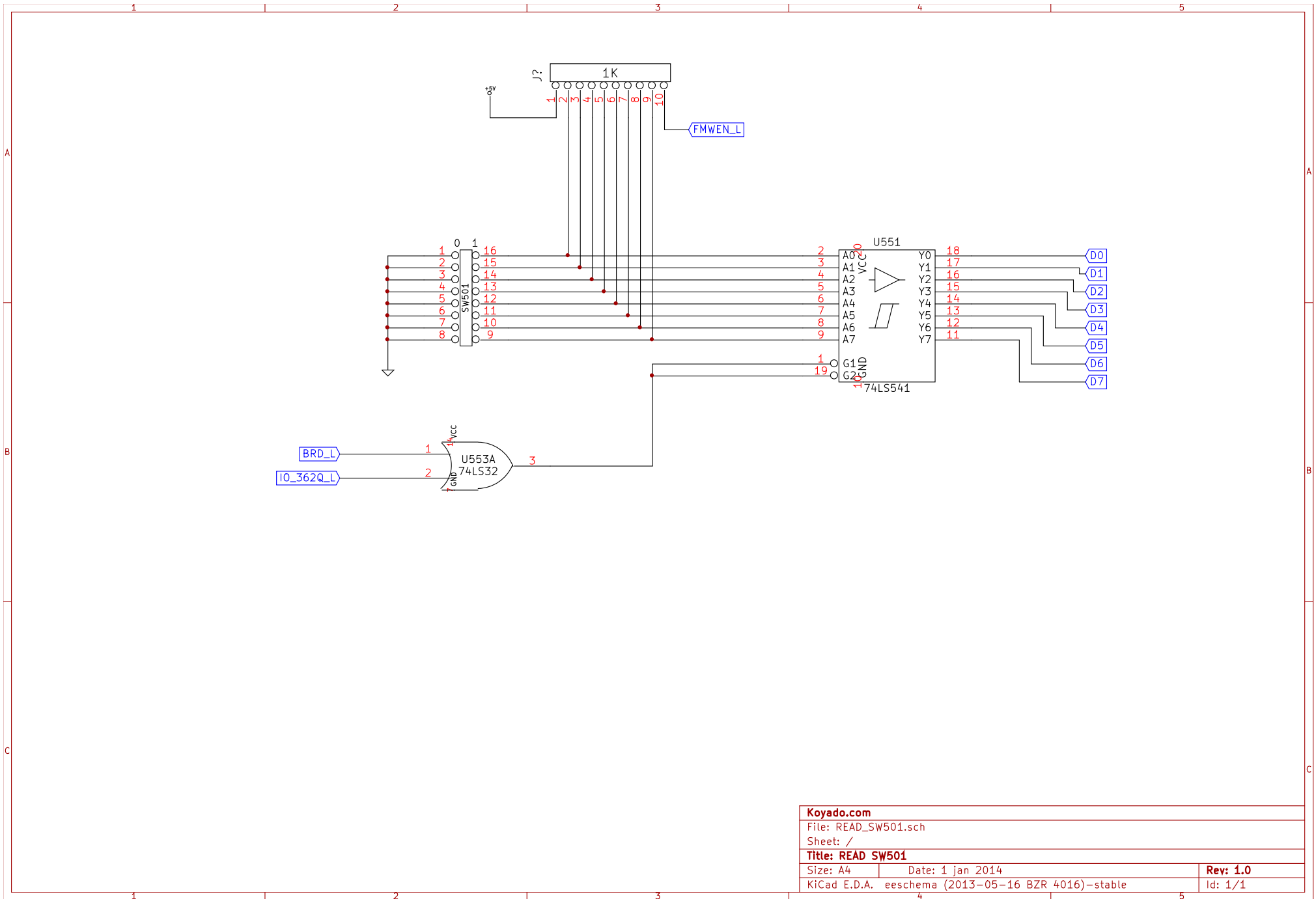


<b>Koyado.com</b>		
File: POWER.sch		
Sheet: /		
<b>Title: POWER</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eschema (2013-05-16 BZR 4016)-stable		Id: 1/1

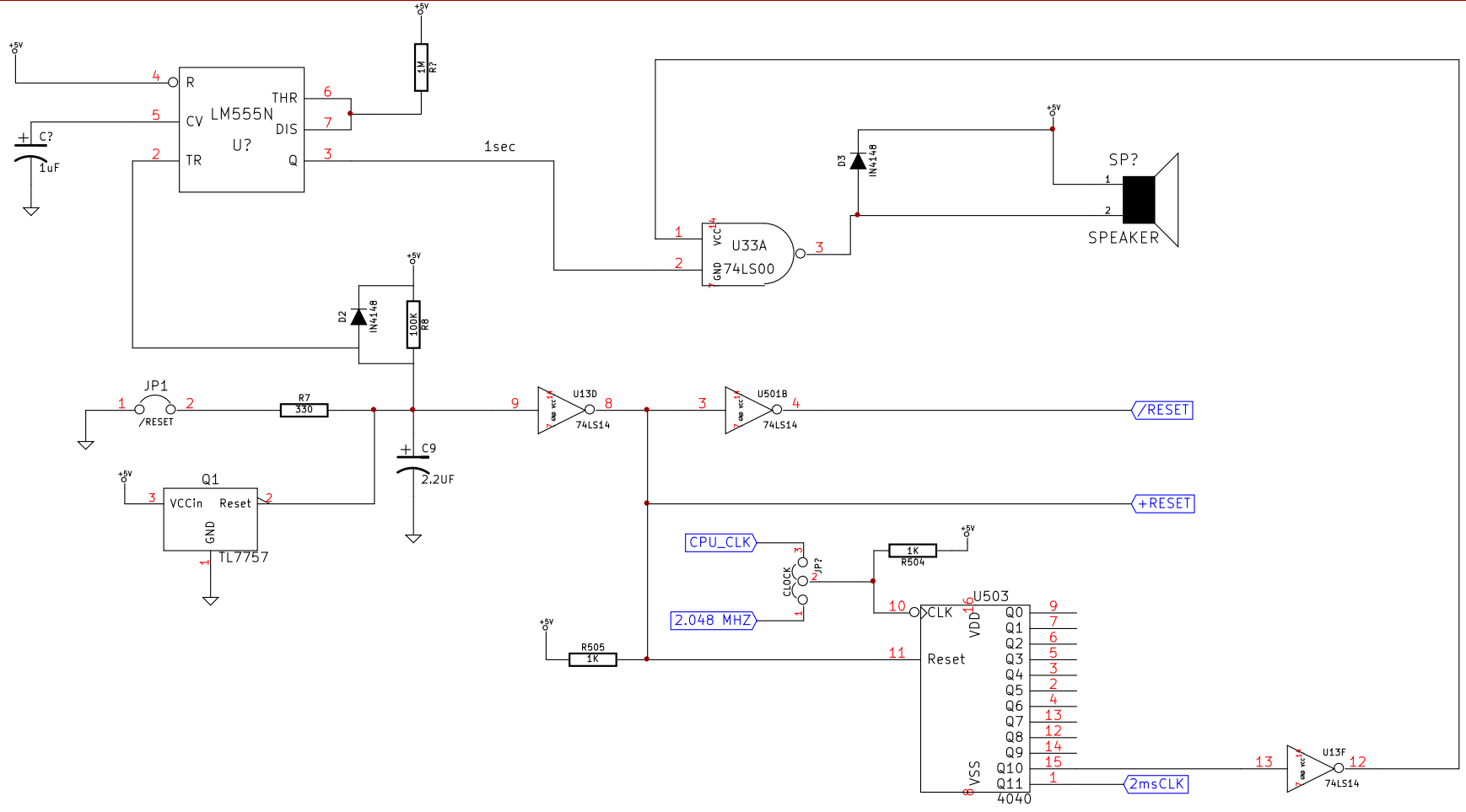


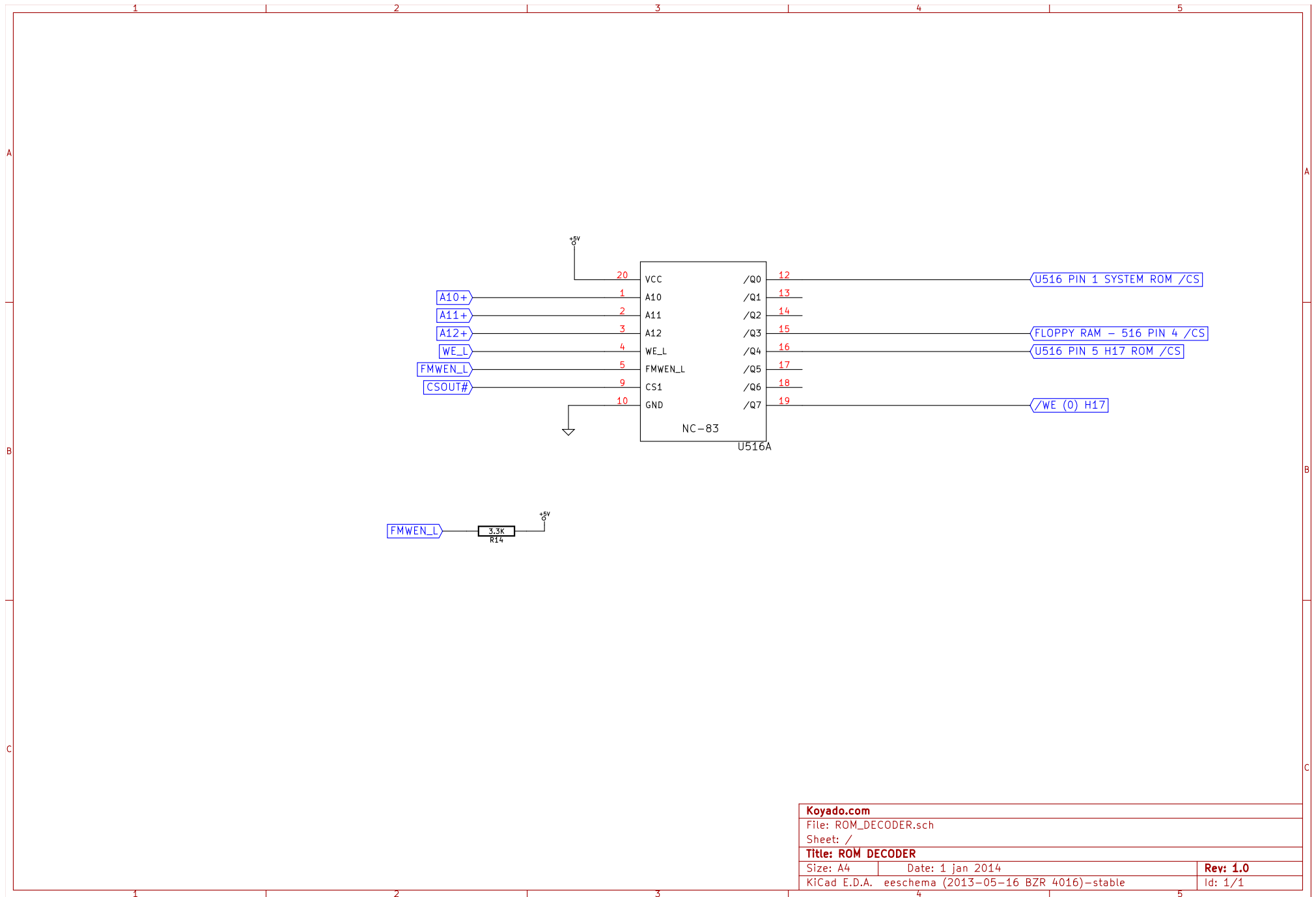
NOTE: BSEL is used to support 64K of RAM

<b>Koyado.com</b>		
File: RAM_DECODER.sch		
Sheet: /		
<b>Title: RAM DECODER</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1



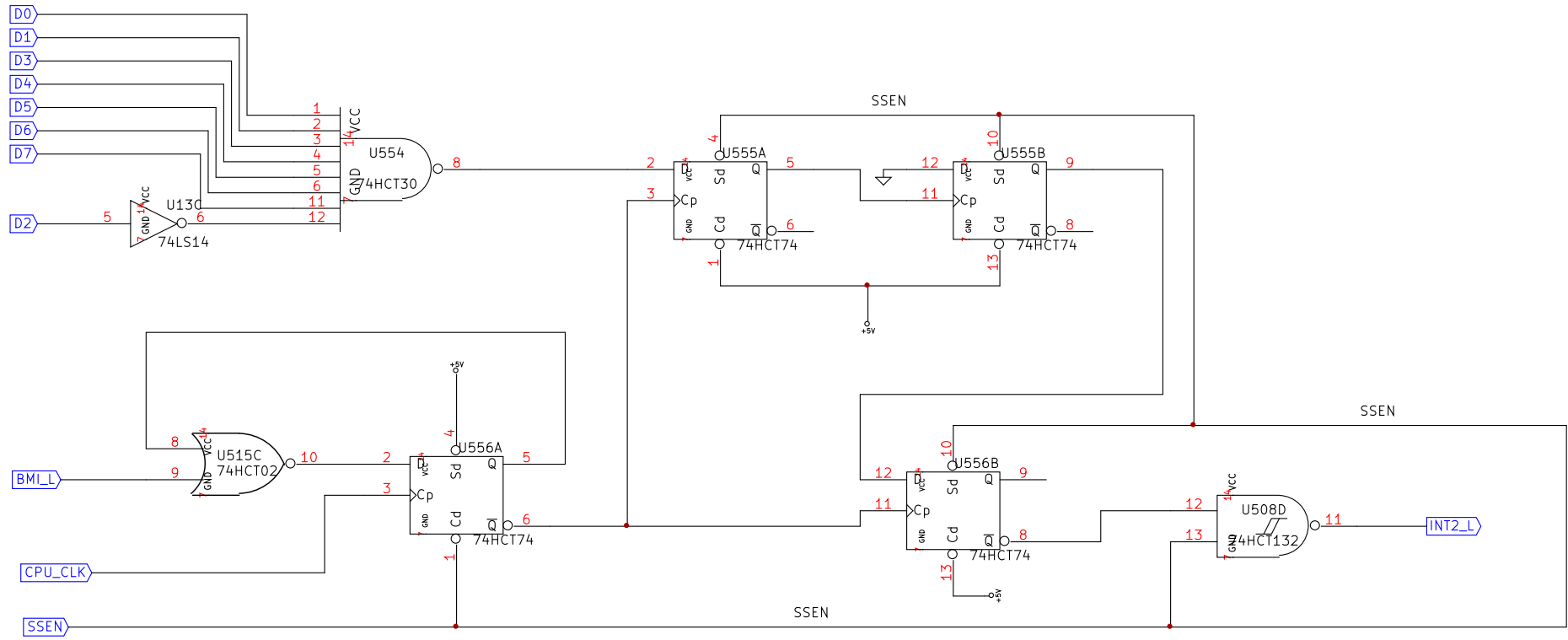
<b>Koyado.com</b>		
File: READ_SW501.sch		
Sheet: /		
<b>Title: READ SW501</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1





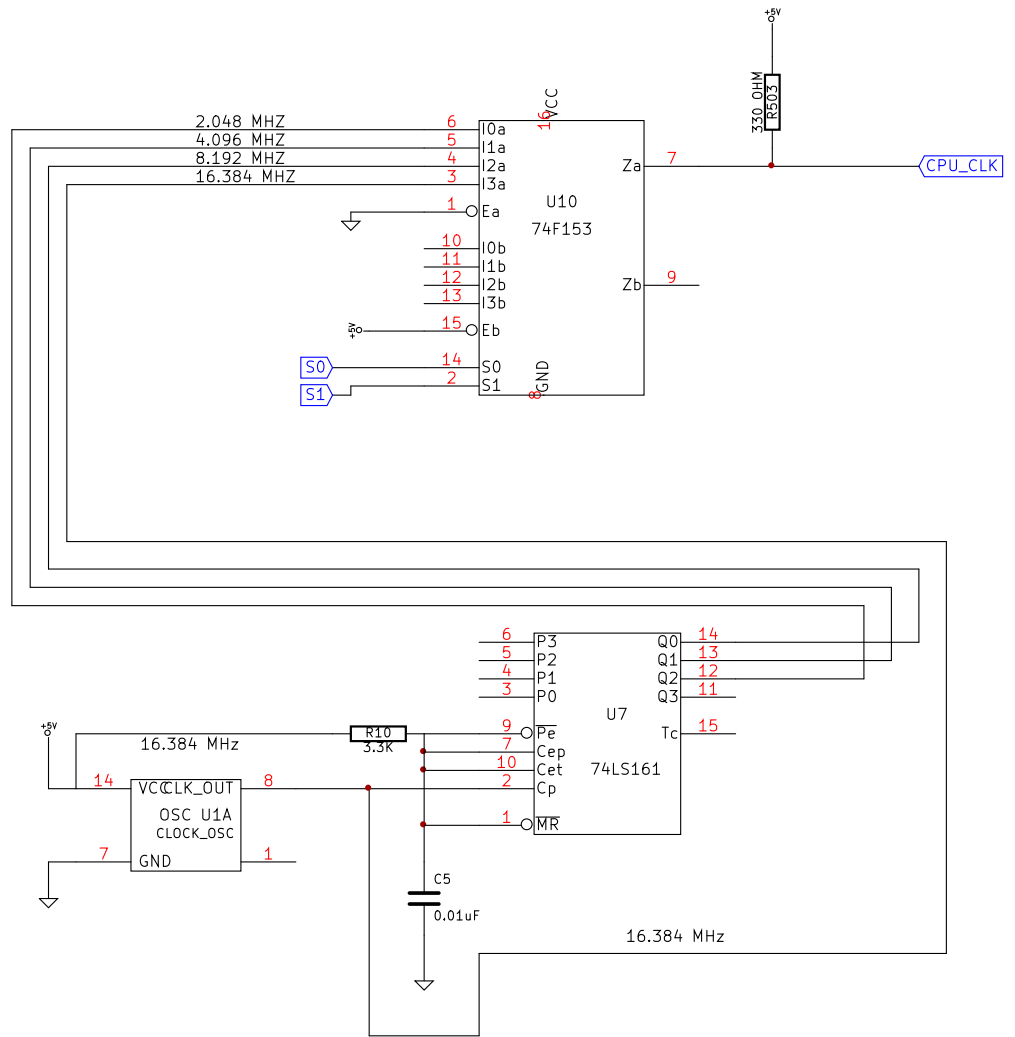
<b>Koyado.com</b>		
File: ROM_DECODER.sch		
Sheet: /		
<b>Title: ROM DECODER</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1



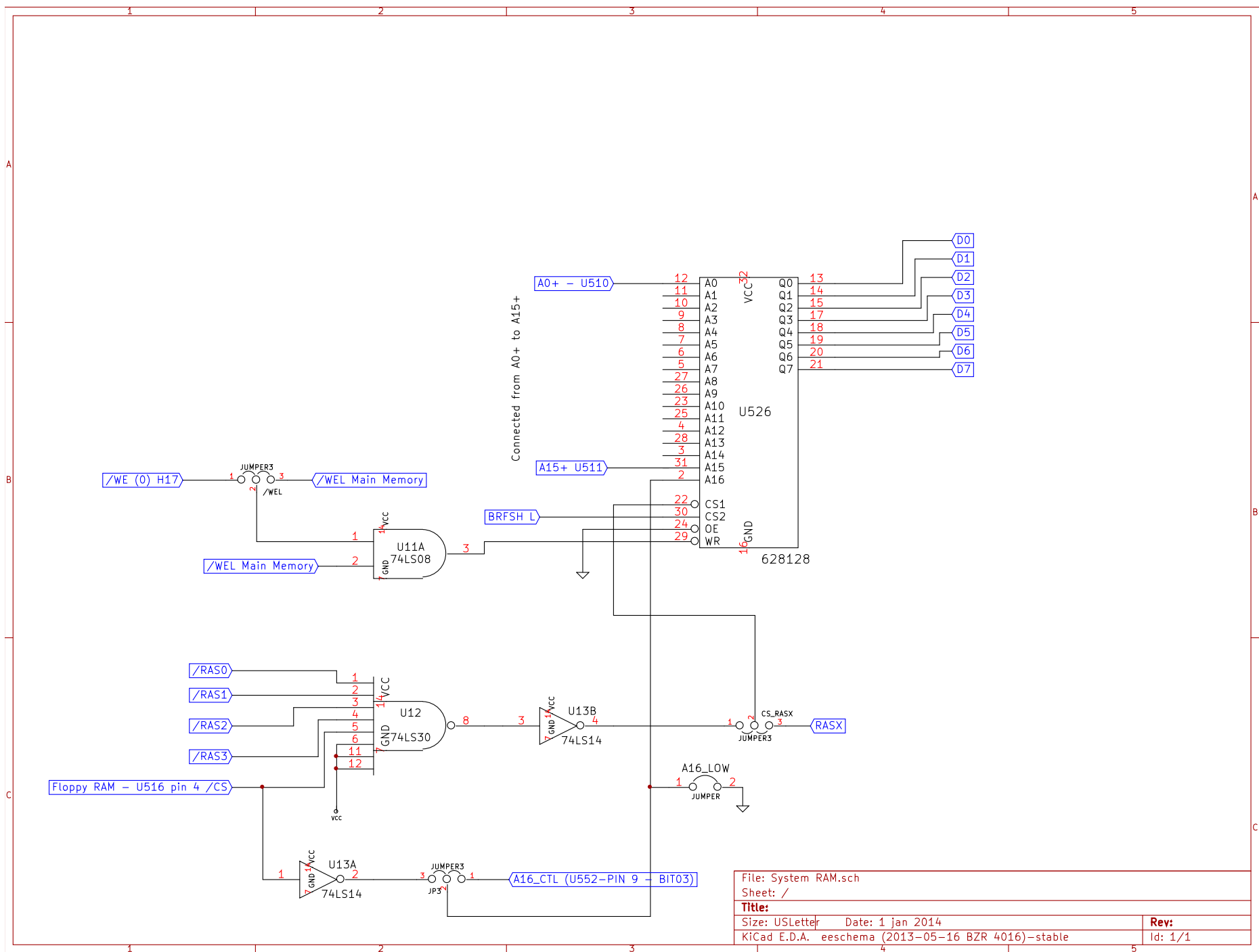


SINGLE STEP INTERRUPT

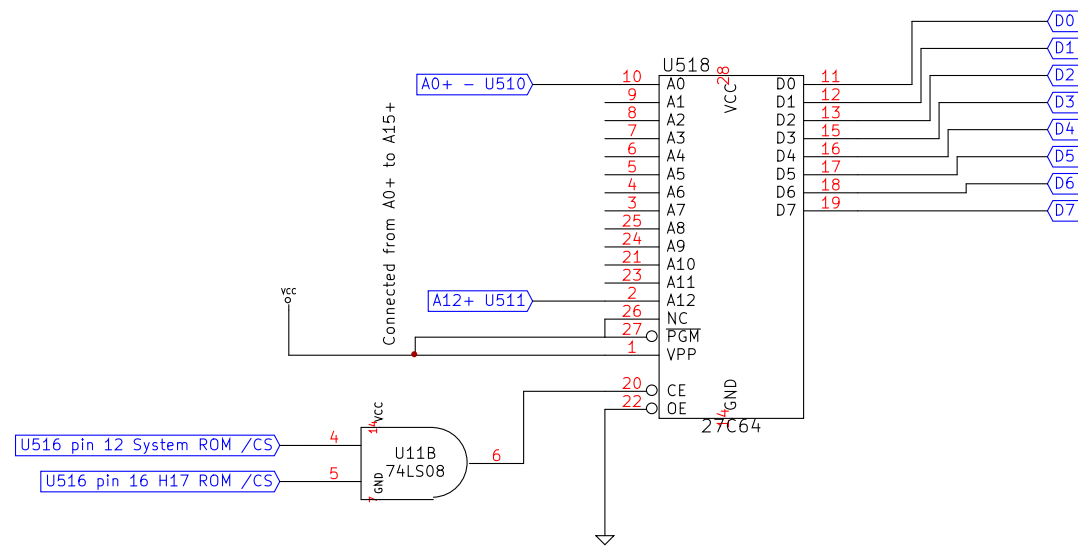
Koyado.com		
File: SINGLE_STEP_2MS_CLOCK.sch		
Sheet: /		
Title: SINGLE STEP & 2MS CLOCK		
Size: A4	Date: 1 jan 2014	Rev: 1.0
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1

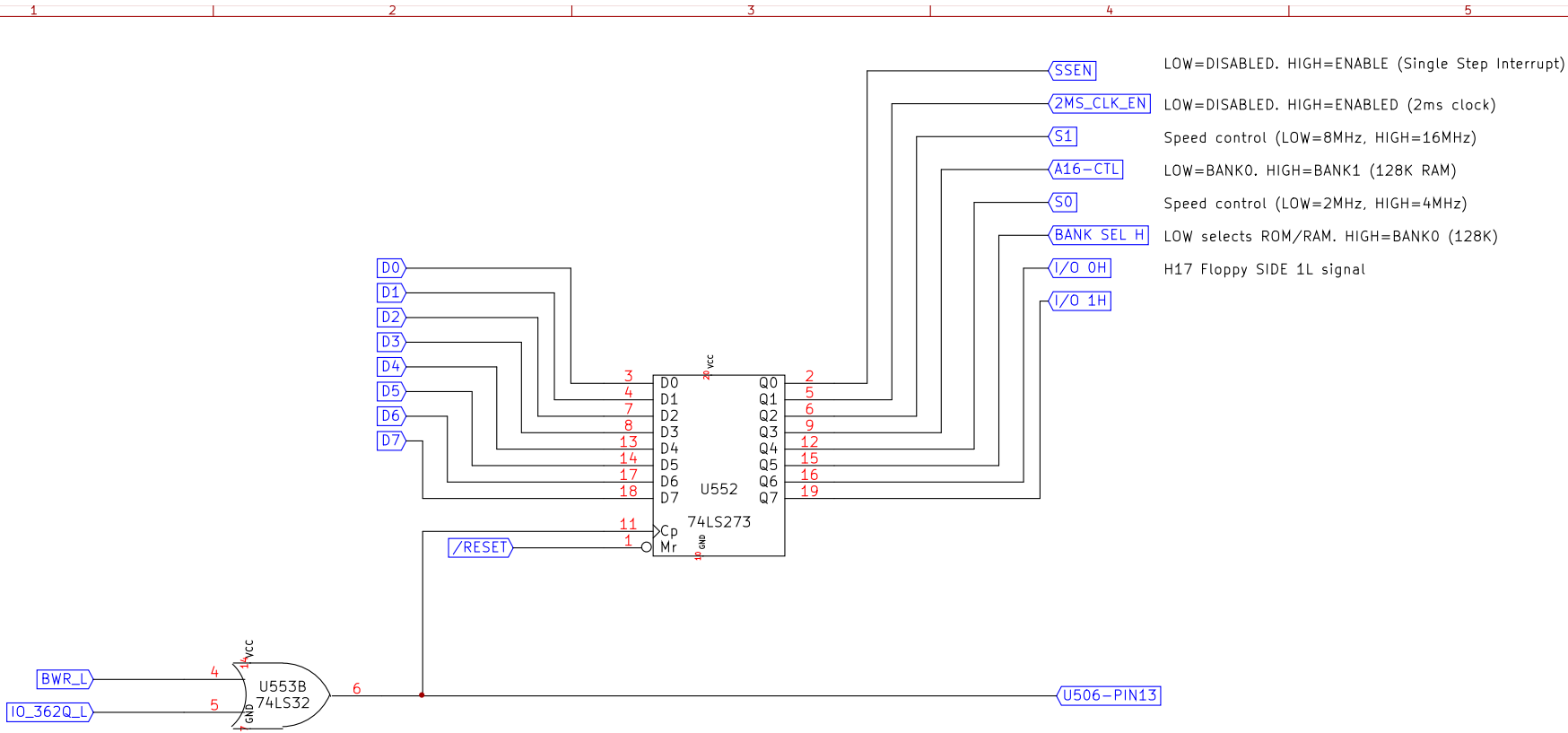


<b>Koyado.com</b>		
File: Speed_Clock.sch		
Sheet: /		
<b>Title: Z80 CPU System Clock</b>		
Size: A4	Date: 1 jan 2014	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1



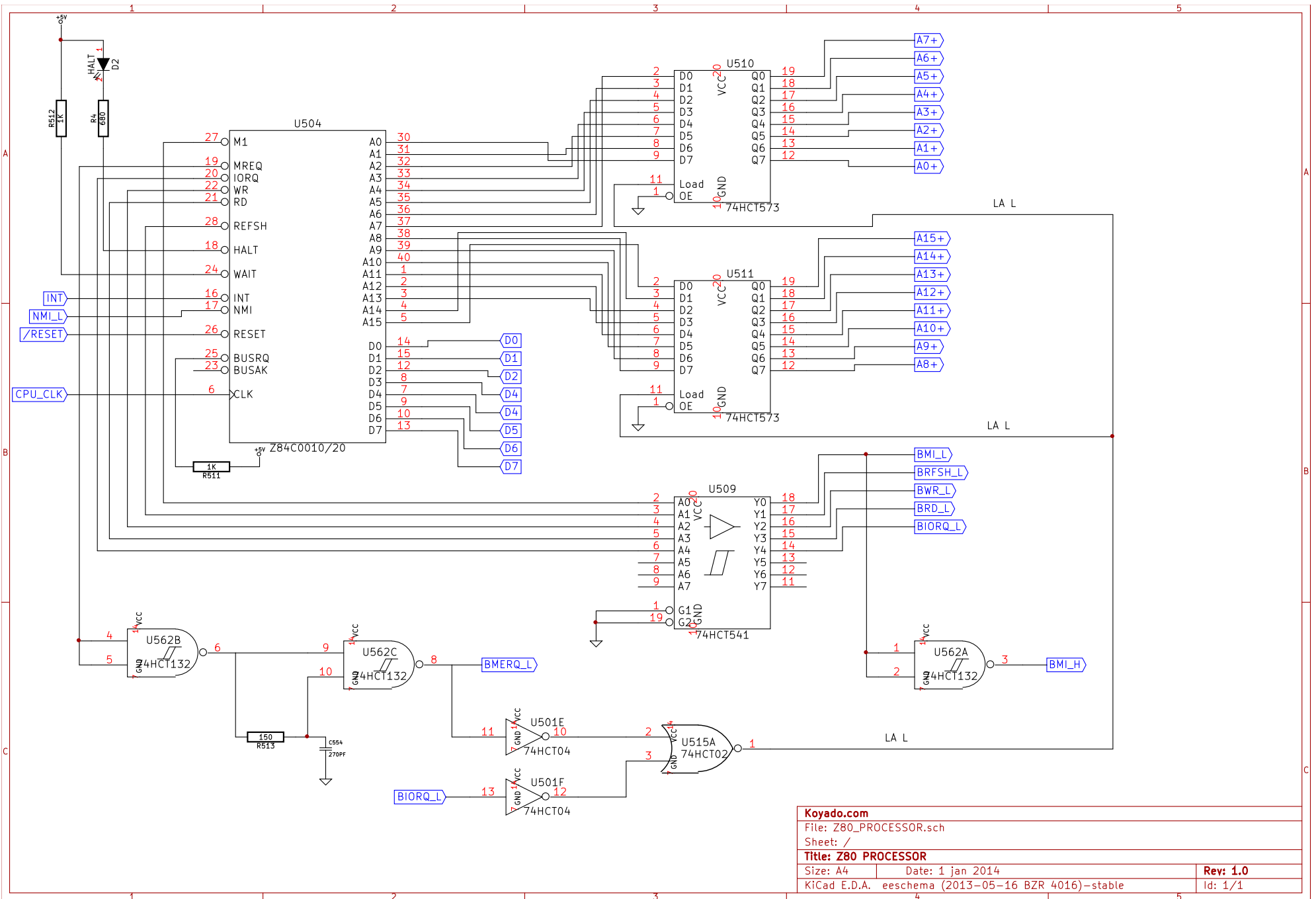
File: System RAM.sch	
Sheet: /	
<b>Title:</b>	
Size: USLetter	Date: 1 jan 2014
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable	Rev: 1/1





- SSEN LOW=DISABLED. HIGH=ENABLE (Single Step Interrupt)
- 2MS\_CLK\_EN LOW=DISABLED. HIGH=ENABLED (2ms clock)
- S1 Speed control (LOW=8MHz, HIGH=16MHz)
- A16-CTL LOW=BANK0. HIGH=BANK1 (128K RAM)
- S0 Speed control (LOW=2MHz, HIGH=4MHz)
- BANK\_SEL H LOW selects ROM/RAM. HIGH=BANK0 (128K)
- I/O 0H H17 Floppy SIDE 1L signal
- I/O 1H

<b>Koyado.com</b>		
File: WRITE_PORT_362Q.sch		
Sheet: /		
<b>Title: WRITE PORT 362Q</b>		
Size: A4	Date: 31 dec 2013	<b>Rev: 1.0</b>
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable		Id: 1/1



<b>Koyado.com</b>	
File: Z80_PROCESSOR.sch	
Sheet: /	
<b>Title: Z80 PROCESSOR</b>	
Size: A4	Date: 1 jan 2014
KiCad E.D.A. eeschema (2013-05-16 BZR 4016)-stable	
Rev: 1.0	
Id: 1/1	

