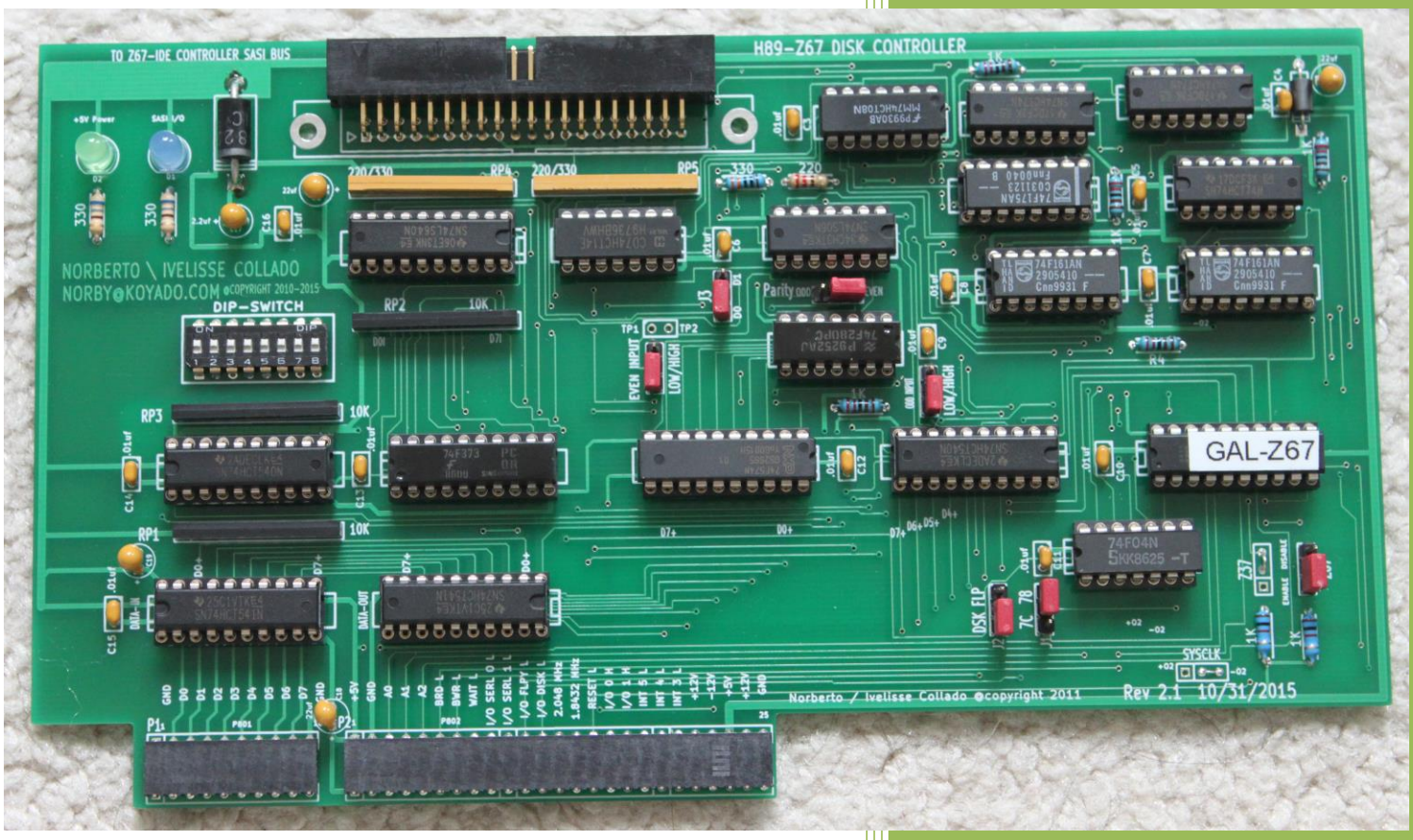
# 2015

# H89-Z67-DISK CONTROLLER REV 2.1




Norberto Collado

norby@koyado.com

4/12/2015

# Revision History and Disclaimer

| Revision History | | |
|---|---|---|
| **Revision** | **Date** | **Comments** |
| 1.0 | 03/02/2011 | Initial draft by Norberto Collado |
| 1.1 | 04/12/2015 | Update to support board Rev 2.1 |
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Another purpose of this document is to allow the surviving classic computers to continue to function. Without the proper software support, the hardware cannot be seen in action, and a piece of our digital history is lost. I have not included any material in this document which I believe has current commercial value. Most of the material in this document is the intellectual property of other companies or individuals. However many of the companies are no longer in existence, and I do not have current contact information to obtained permission to include them.

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Thank you for your understanding and consideration.

# Table of Contents

# Introduction

This document provides an overview on the H89-Z67 disk controller board design by Norberto Collado for the Heathkit H89 Computer.

# H89-Z67 DISK CONTROLLER

The H89-Z67 controller contains a standard SASI interface bus to boot from the Z67-IDE storage board. The H89-Z67 controller is operable at any CPU speed up to 10 MHz, and it supports two bootable IDE hard drives via the H89 System ROM. The H89-Z67 SASI DISK CONTROLLER mounts inside the H89 computer cabinet while attached to the Z67-IDE controller allowing IDE boot support.

Please refer to the following website to download supported IDE H89 Monitor;

http://koyado.com/Heathkit/Z67-IDE.html

2732a_444_84c_ide_mms_v1.hex.zip (H89 IDE Monitor ROM)

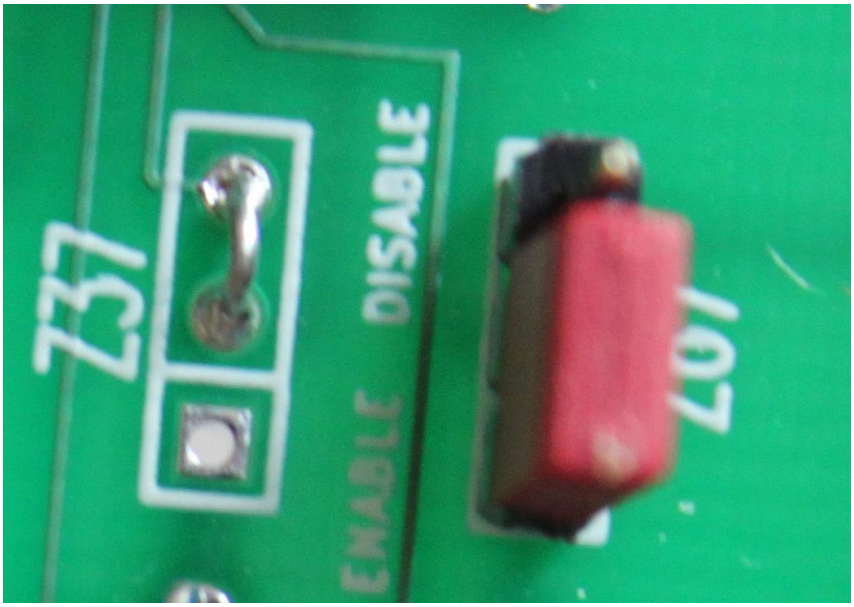
# CONTROLLER CARD PORTS CONFIGURATION

The following is a table summary of the controller ports configuration. Please refer to the H89 documentation for switch definition for proper port settings.
Documentation can be obtained at the following website;
http://www.lesbird.com/sebhc/index.html

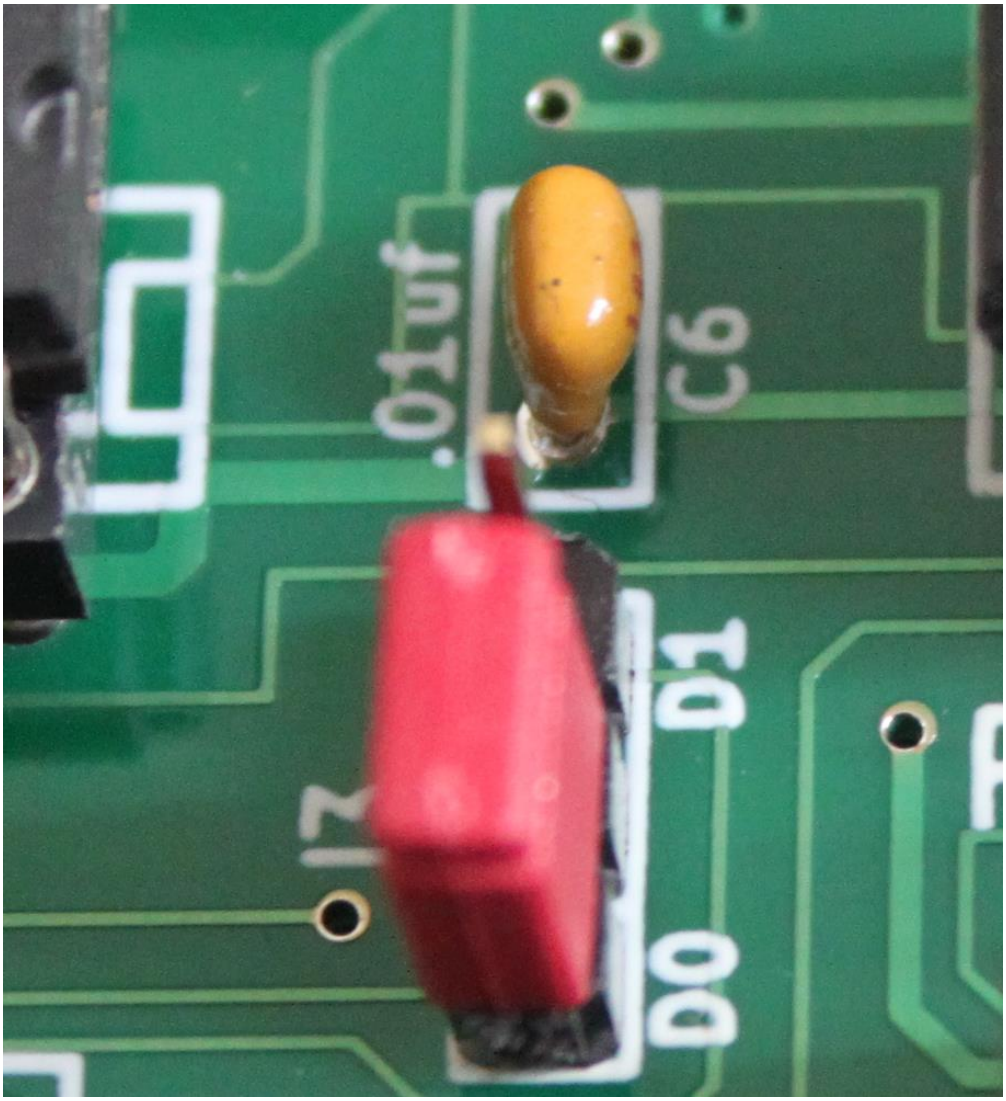
| CONTROLLER CARD | PORT | H89-Z67 PORT |
|---|---|---|
| H17 | 7CH (174Q) | 78H (170Q) |
| H89-Z37 | 78H (170Q) | 7CH (174Q) |
| H47 | 78H (170Q) | 7CH (174Q) |

# H89-Z67 Jumper Configuration

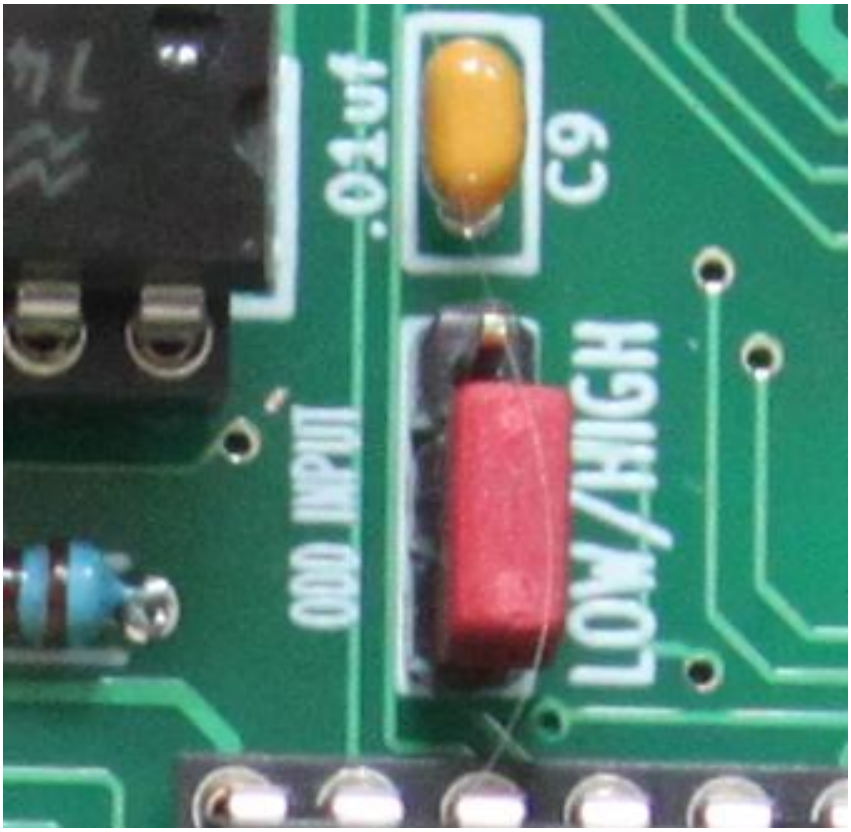
(  ) Z-37 Disabled (solder a bare wire across pin 2 and 3 as shown below)
(  ) Z-67 Enabled (solder a 3 pin header and insert jumper as shown below)



(  ) Solder on J3 a 3-pin header and insert jumper as shown below (D0).

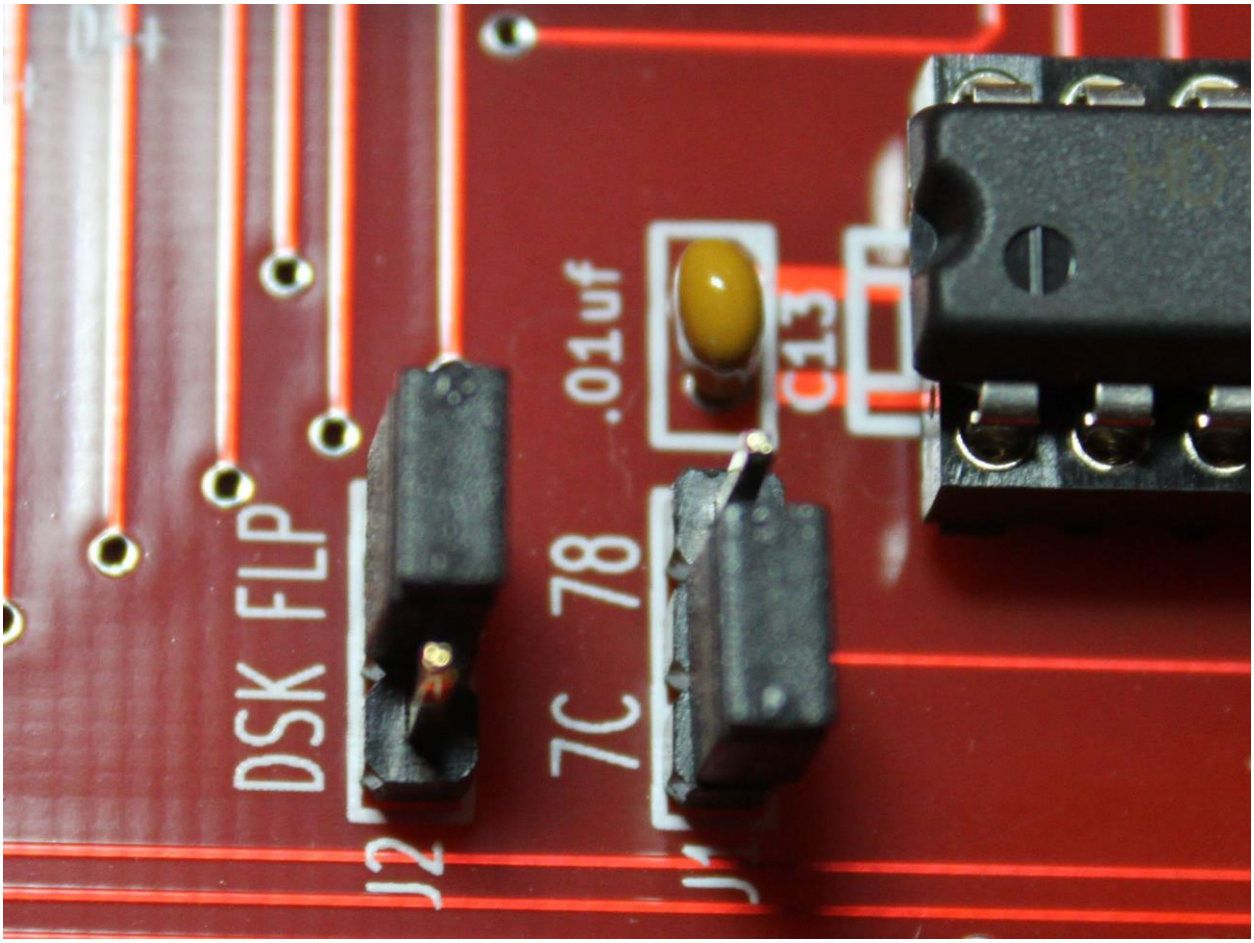


(  ) Insert Jumper across Parity header between pin 1 and 2 as shown (LOW Default).



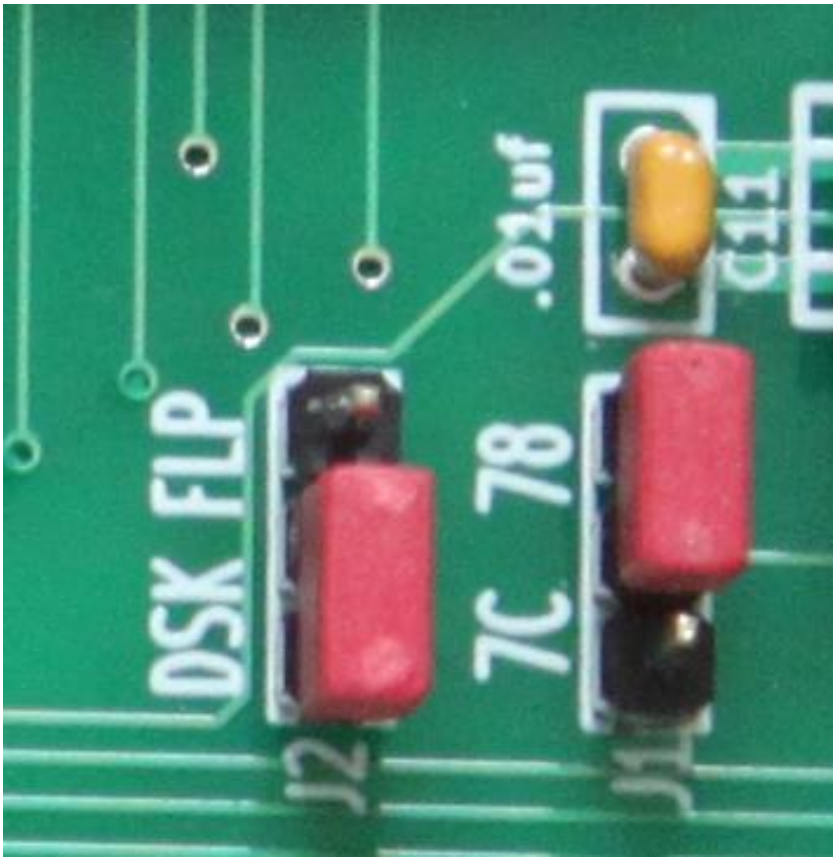
(  ) If inserting H89-Z67 board on P506 and P512 locations, then place a Jumper on J2 across pin 2 and 3 (FLP Signal)

(  ) If inserting H89-Z67 board on P506 and P512 locations, then place a Jumper on J1 across pin 1 and 2 (Address 7C hex))

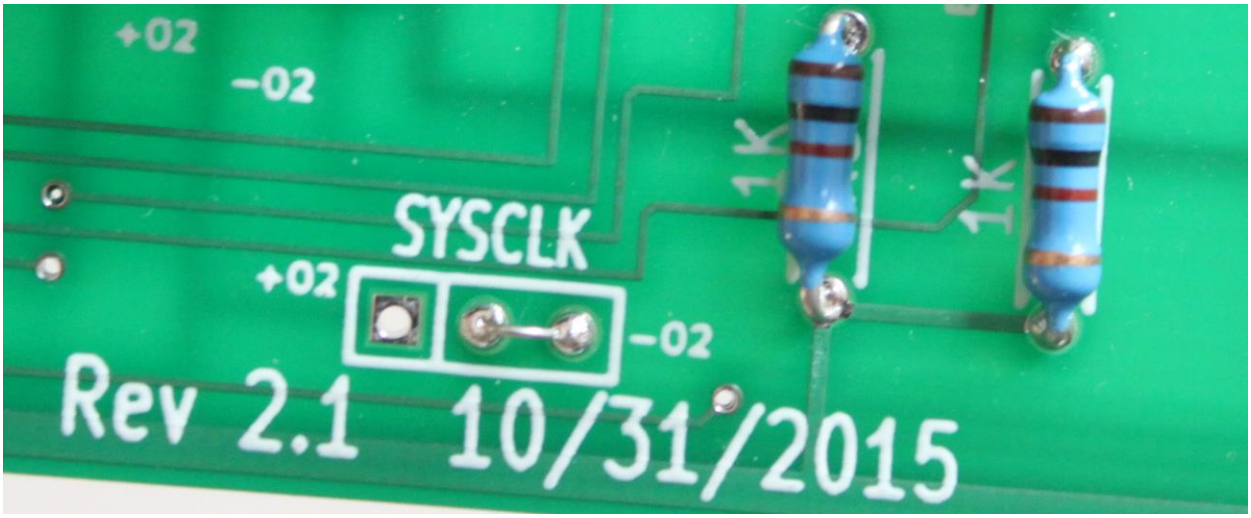


(  ) If inserting H89-Z67 board on P504 and P510 locations, then place a Jumper on J2 across pin 1 and 2 (DSK Signal)

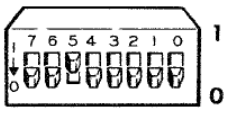
(  ) If inserting H89-Z67 board on P504 and P510 locations, then place a Jumper on J1 across pin 2 and 3 (Address 78 hex))



(  ) Solder on **SYSCLK** a bare wire across pin 2 and 3 as shown below.



# CPU DIP SWITCH SW501 SETUP




CPU DIP Switch SW501, located at the lower right of the Z-89/90 CPU Board, has eight sections (0 to 7) that may be set to either one or zero. These sections have the following functions:

| SECTIONS | SETTINGS | SETTING DEFINITION | SECTION DEFINITION |
|---|---|---|---|
| 1,0 | | 00 — Hard-sectored 5.25-inch disk.<br>01 — H/Z-47 eight-inch floppy.<br>10 — Z-67 Winchester.<br>11 — No device. | Selects the device located at port 07CH (174Q), plugs P506 and P512. |
| 3,2 | | 00 — Soft-sectored 5.25-inch disk.<br>01 — H/Z-47 eight-inch floppy.<br>10 — Z-67 Winchester.<br>11 — No device | Selects the device located at port 078H (170Q), plugs P504 and P510, or P505 and P511. |
| 4 | | 0 — Primary boot from device at 07CH.<br>1 — Primary boot from device at 078H. | Determines whether the primary boot device is at port 07CH (174Q) or at 078H (170Q). The port not configured as primary becomes the secondary device. |
| 5 | | 0 — Initiate memory test on power up.<br>1 — Disable memory test on power up. | Disables/enables memory diagnostic on power up. |
| 6 | | 0 — Set console baud rate at 9600 (normal).<br>1 — Sets console baud rate at 19,200 (not currently supported). | Sets console baud rate. |
| 7 | | 0 — Normal.<br>1 — Auto-boot on power up. | Sets auto-boot. |

# H89-Z67 SASI Bus Pin Assignment

## Z-67 Interface Bus Pin Assignment

The Z-67 interface is connected to the Z-67 controller through a 40-pin connector.

The pin assignments are as follows:

| Signal | Pin No. |
|---|---|
| DATA0 | 2 |
| DATA1 | 4 |
| DATA2 | 6 |
| DATA3 | 8 |
| DATA4 | 10 |
| DATA5 | 12 |
| DATA6 | 14 |
| DATA7 | 16 |
| PARITY | 18 |
| ——— | 20 (spare) |
| ——— | 22 (key) |
| ——— | 24 (spare) |
| BUSY | 26 |
| ACK | 28 |
| RST | 30 |
| MSG | 32 |
| SEL | 34 |
| C/D | 36 |
| REQ | 38 |
| I/O | 40 |

NOTE: All signals are active low and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5 volts and 330 ohms to ground.

# H89-Z67 Interface Register Definition

When booting from the H89-Z67 Disk Controller and after receiving an interrupt, the H89 computer sends either an **I/O FLPY** signal to pin 11 of P2 or an **I/O DSK** signal to pin 12 of P2 on the H89-Z67 Interface Board. Either of these signals will enable the GAL-Z67 address decoder on the H89-Z67 controller.

If **I/O FLPY** is used, the H89-Z67 controller is mounted in the right I/O port, that is, P512 and P506 on the H89 CPU Board. **Note: Please makes sure the rework is implemented. Refer to Page #29 for details.**

If **I/O DSK** is used, the H89-Z67 board is mounted in either of the remaining I/O ports, P511 and P505 or P510 and P504 on the H89 CPU Board.

The registers on eth H89-Z67 Disk Controller Board are listed below. The address given assumes that the board is installed at P504, P510 (addresses 170Q - 172Q or 0x78 – 0x7A). If the board is installed at P506, P512, add four to the above address as follows;

170Q + 4Q = 174Q = 0x7C

171Q + 4Q = 175Q = 0x7D

172Q + 4Q = 176Q = 0x7E

The bit definition for each register is described below:

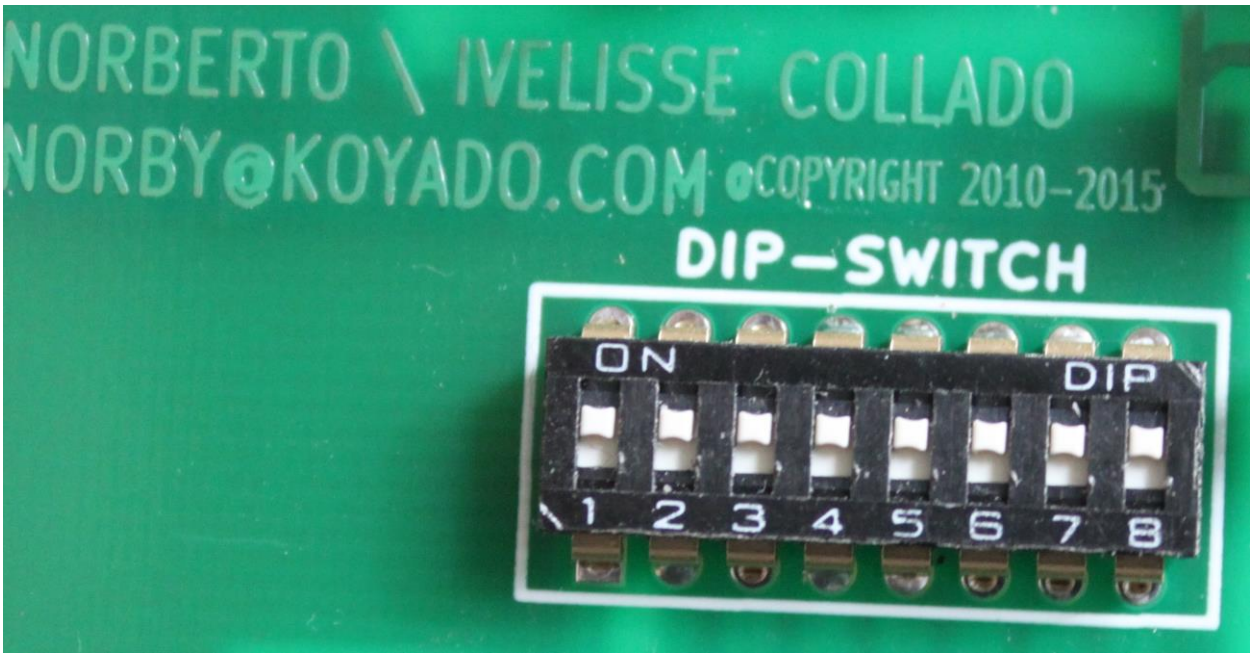
| HEX Address | Octal Address | Register | Operation |
|---|---|---|---|
| 0x78 | 170Q | Data In/Out | Read and Write |
| 0x79 | 171Q | Control Register | Write Only |
| 0x79 | 171Q | Status Register | Read Only |
| 0x7A | 172Q | DIP SWITCHES (DS1) | Read Only |

| Control Register | Output Address (0x79, 171Q) |
|---|---|
| bit 7 | Data Enable |
| bit 6 | SASI SEL - Assert Select and Data. Bit 0 is hard wire to access the controller. |
| bit 5 | Interrupt Enable - causes interrupt if SASI REQ is present. |
| bit 4 | SASI Reset |
| bit 3 | Not Used |
| bit 2 | Not Used |
| bit 1 | Not Used |
| bit 0 | Not Used |

| Bus Status | Input Address (0x79, 171Q) |
|---|---|
| bit 7 | SASI REQ - Indicates the Z67-IDE controller either request data or has data for the H89-Z67 Disk Controller. |
| bit 6 | SASI IN/OUT (referenced to controller) - Low indicates data to Interface board. High indicates data to controller. |
| bit 5 | SASI MSG – Indicates last byte in data or command string. |
| bit 4 | SASI COMMAND/DATA - Is high when a command is being sent to the controller, and it is low when data is being sent. |
| bit 3 | SASI BUSY - Indicates that the SASI Bus is busy, no other device can access the SASI Bus. |
| bit 2 | PARITY ERROR - Indicates BAD parity. |
| bit 1 | INTERRUPT IN PROGRESS - Verifies that interrupt has been activated. Reading status port resets interrupt. |
| bit 0 | SASI ACK - Acknowledges request for data. |

# H89-Z67 DS1 Switch Definition

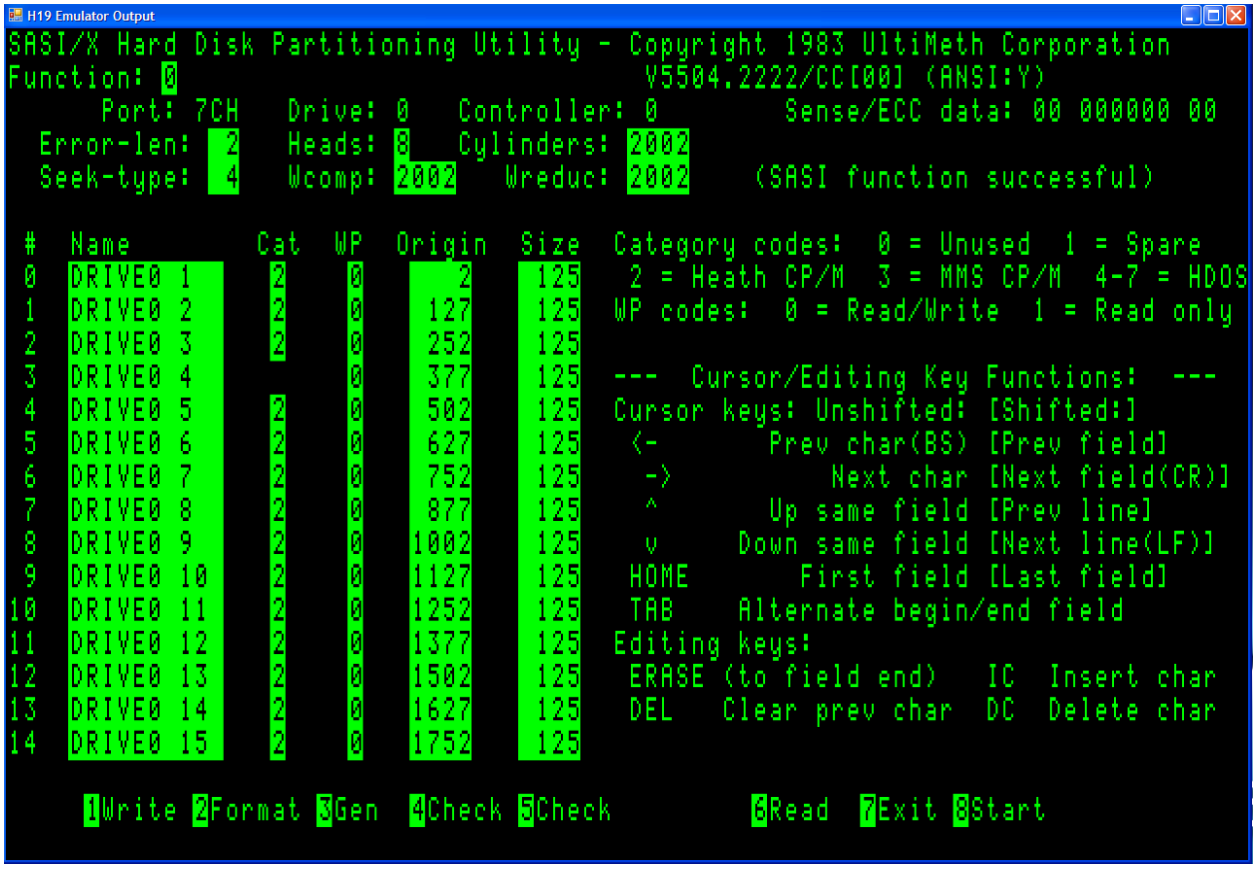
The DIP 8 Switch that is on the H89-Z67 controller is used to define the boot partition from Hard Disk 0 or Hard Disk 1. The QSBIOS supports 15 partitions per drive and all of them are bootable if the QSPUTSYS.COM file was used to enable them. Below are the 15 partitions for Drive 0 and 1, and its assignment per Switch DS1 definition. **Make sure all switches are set to the "ON" position as shown below.**



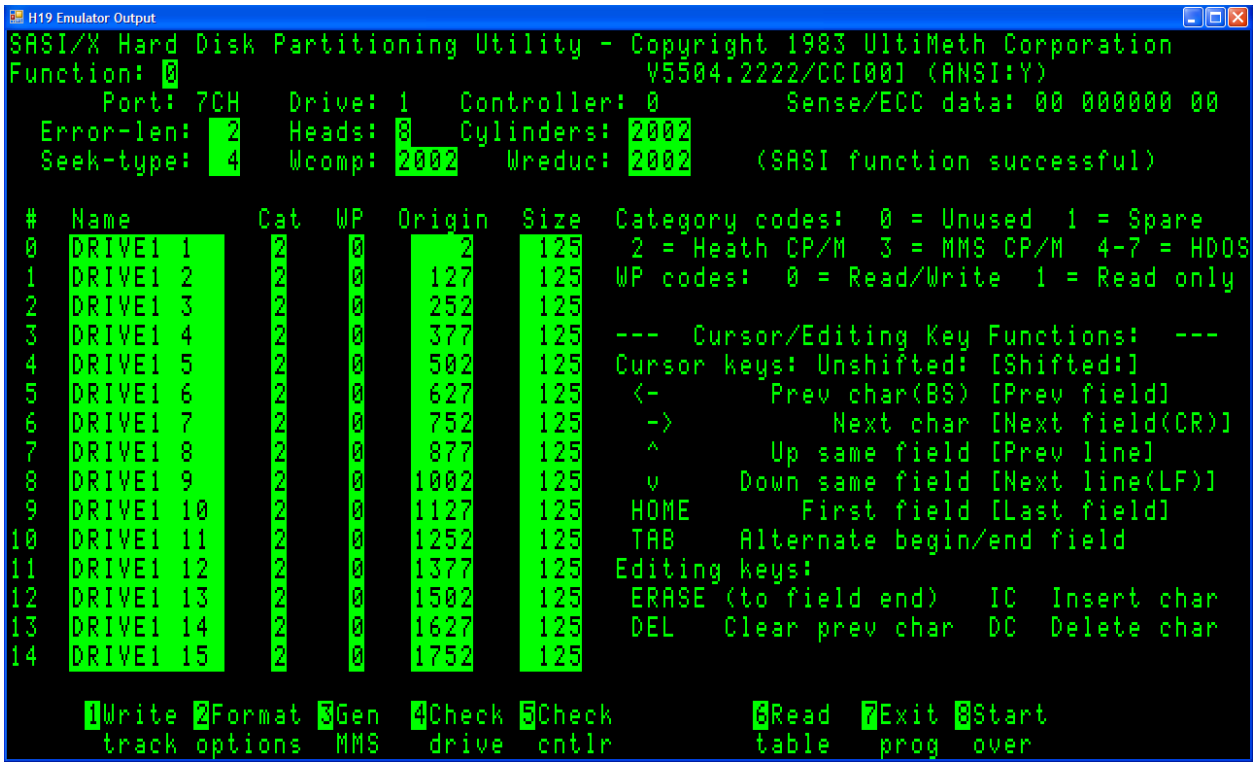
## DSI Boot Partitions Assignments

| DS1: | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| SW 8 | SW 7 | SW 6 | SW 5 | SW 4 | SW 3 | SW 2 | SW 1 | Boot Partition Drive 0 | Boot Partition Drive 1 |
| OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON | DRIVE0 2 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | OFF | ON | OFF | DRIVE0 3 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | OFF | ON | ON | DRIVE0 4 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | ON | OFF | OFF | DRIVE0 5 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | ON | OFF | ON | DRIVE0 6 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | ON | ON | OFF | DRIVE0 7 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | OFF | ON | ON | ON | DRIVE0 8 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | OFF | OFF | OFF | DRIVE0 9 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | OFF | OFF | ON | DRIVE0 10 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | OFF | ON | OFF | DRIVE0 11 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | OFF | ON | ON | DRIVE0 12 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | ON | OFF | OFF | DRIVE0 13 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | ON | OFF | ON | DRIVE0 14 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | ON | ON | OFF | DRIVE0 15 | DRIVE1 1 |
| OFF | OFF | OFF | OFF | ON | ON | ON | ON | MENU SELECTABLE | DRIVE1 1 |
| | | | | | | | | | |
| OFF | OFF | OFF | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 2 |
| OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 3 |
| OFF | OFF | ON | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 4 |
| OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 5 |
| OFF | ON | OFF | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 6 |
| OFF | ON | ON | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 7 |
| OFF | ON | ON | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 8 |
| ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 9 |
| ON | OFF | OFF | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 10 |
| ON | OFF | ON | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 11 |
| ON | OFF | ON | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 12 |
| ON | ON | OFF | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 13 |
| ON | ON | OFF | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 14 |
| ON | ON | ON | OFF | OFF | OFF | OFF | OFF | DRIVE0 1 | DRIVE1 15 |
| ON | ON | ON | ON | OFF | OFF | OFF | OFF | DRIVE0 1 | MENU SELECTABLE |
| | | | | | | | | | |

## Drive 0 Partitions



## Drive 1 Partitions



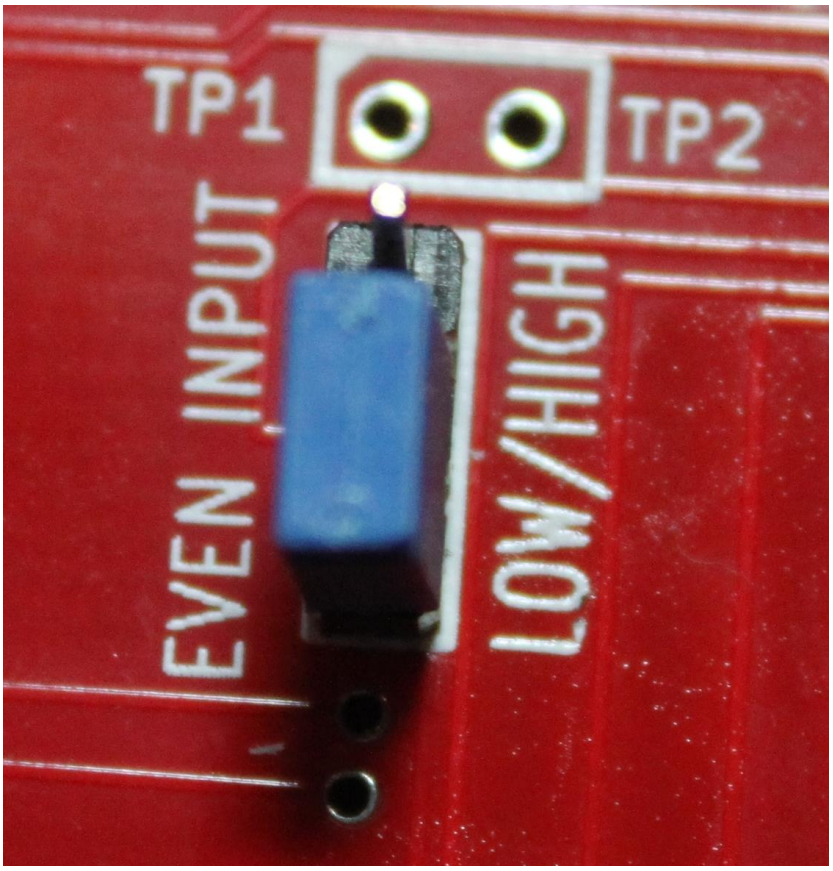
## Menu Selectable Boot Partitions


HEATH/ZENITH H/Z67
Software Boot Code (SBC) vers 1.1
Boot Option(s) Menu
Operating systems:
Maximum occurrence number:
HDOS 00
HDOS1 00
HDOS2 00
HDOS3 00
HDOS4 00
HDOS5 00
HDOS6 00
HDOS7 00
Boot String?.....> HDOS
ACTION? <BOOT> BOOT
Heathkit H89


CPU speed => 4MHZ....
IDE: Boot SS-1
64K LLL/HEATH/ZENITH QUIKSTOR (C) CP/M 2.2.04 05/15/85
FOR HI7 SASI DISKS WITH OPTION(S) IB
A>FBAD
FINDBAD - ver 5.4
Bad sector lockout program
Universal version
Type CTL-C to abort
Testing directory area...
Testing data area...
Heathkit H89

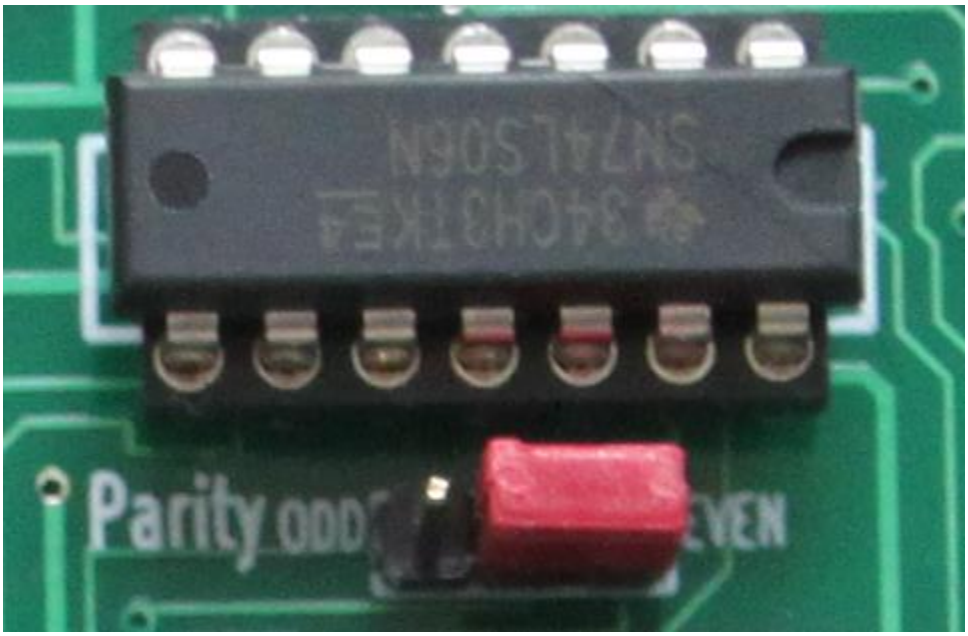
# H89-Z67 Configuring Parity for HDOS & CP/M Boot

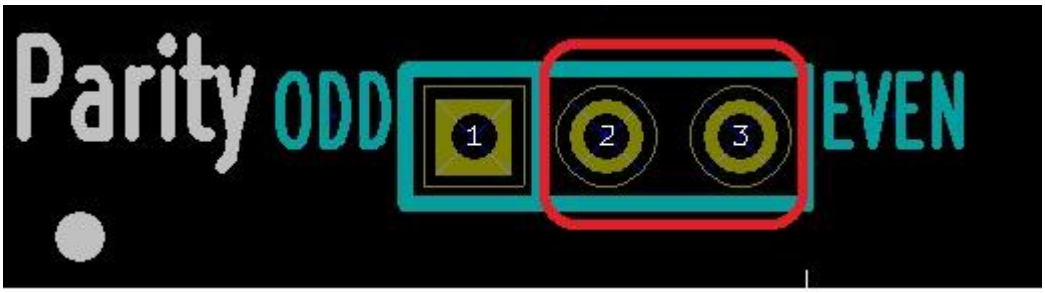
1. Install jumper across pin 1 and 2 on “EVEN INPUT” header (LOW)




2. Install jumper across pin 1 and 2 on “ODD INPUT” header (LOW).

3. Install jumper across pin 2 and 3 on “PARITY” header (EVEN).

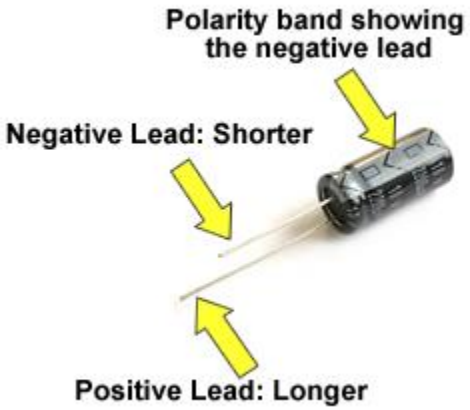


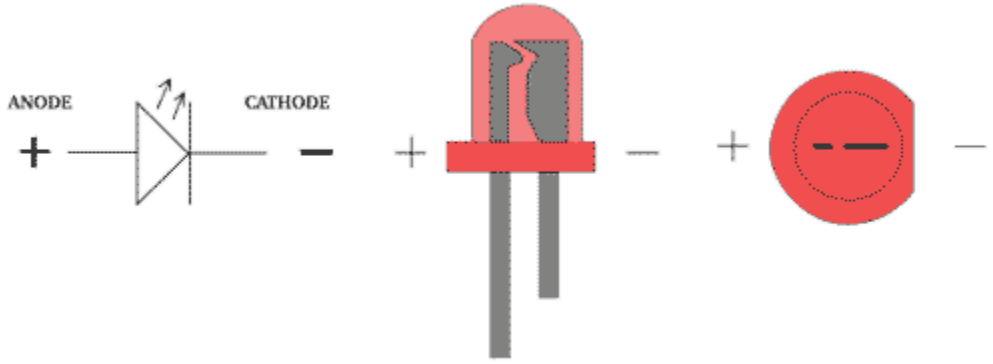

Note: Failure to configure properly will inhibit HDOS boot.

# H89-Z67 Board Assembly

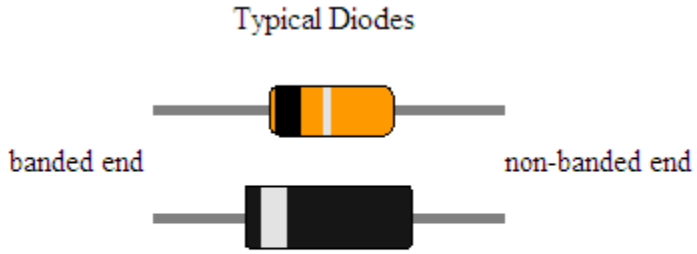
1. Install C3 – C16 - 0.01uF caps.
2. Install C1, C2, C17, C18, and C19 - 22uF caps (observed polarity).

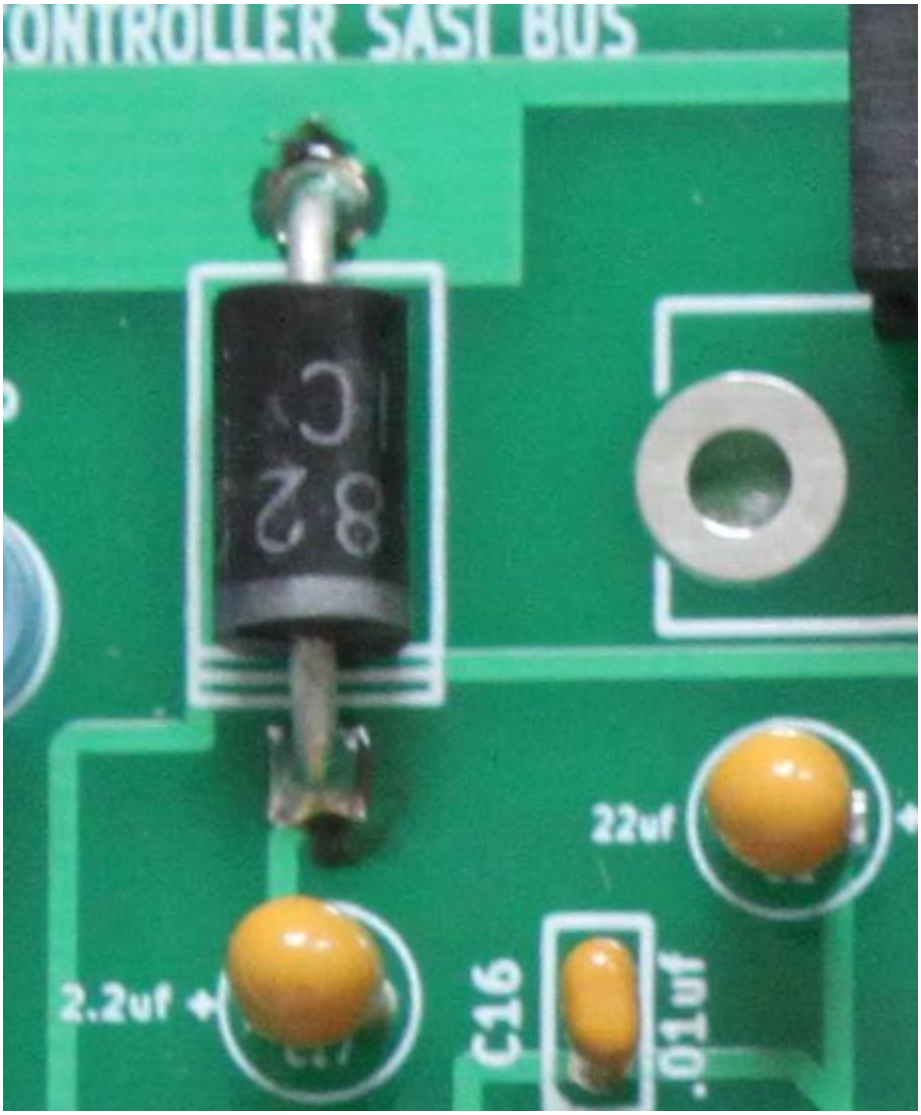



3. Install Green LED – D2 (observed polarity).
4. Install Red or Blue LED – D1 (observed polarity).



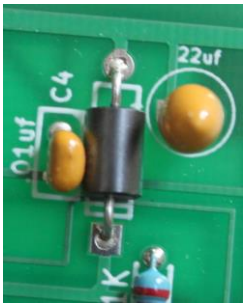
5. Install D1 – 1N5822 diode.



| Resistor Band Color Reference | | | | |
|---|---|---|---|---|
| *Color* | *Band 1* | *Band 2* | *Multiplier* | *Tolerance* |
| Black | 0 | 0 | x 1 | not used |
| Brown | 1 | 1 | x 10 | not used |
| Red | 2 | 2 | x 100 | not used |
| Orange | 3 | 3 | x 1000 = 1K | not used |
| Yellow | 4 | 4 | x 10000 = 10K | not used |
| Green | 5 | 5 | x 100000 = 100K | not used |
| Blue | 6 | 6 | x 1000000 = 1M | not use |
| Violet | 7 | 7 | not used | not used |
| Gray | 8 | 8 | not used | not used |
| White | 9 | 9 | not used | not used |
| Gold | not used | not used | divide by 10 | ±5% |
| Silver | not used | not used | divide by 100 | ±10% |
| None | not used | not used | not used | ±20% |

6. Install R6 – 220 OHMS resistor
7. Install R1, R2, and R7 – 330 OHMS resistors.
8. Install R3, R4, R5, R10, R11, R13 – 1K OHMS resistors.
9. Install RP1, RP2 AND RP3 10K BUSSED 10 pin resistor. Pin one is on the left side. If install incorrectly, data corruption might happen.
10. Install the two 220/330 - 10 pin Bus Termination resistors – RP4 and RP5.
11. Install all 14 pin IC sockets.
12. Install all 16 pin IC sockets.
13. Install all 20 pin sockets.
14. Install 40 pin right angle header connector.
15. Install five 3 pin headers.
16. Install DIP-SWITCH
17. Install 10 PIN MB Connector (P1)
18. Install 25 PIN MB Connectors (P2)
19. Install U10 – 74F280 or 74LS280 IC.
20. Install FB

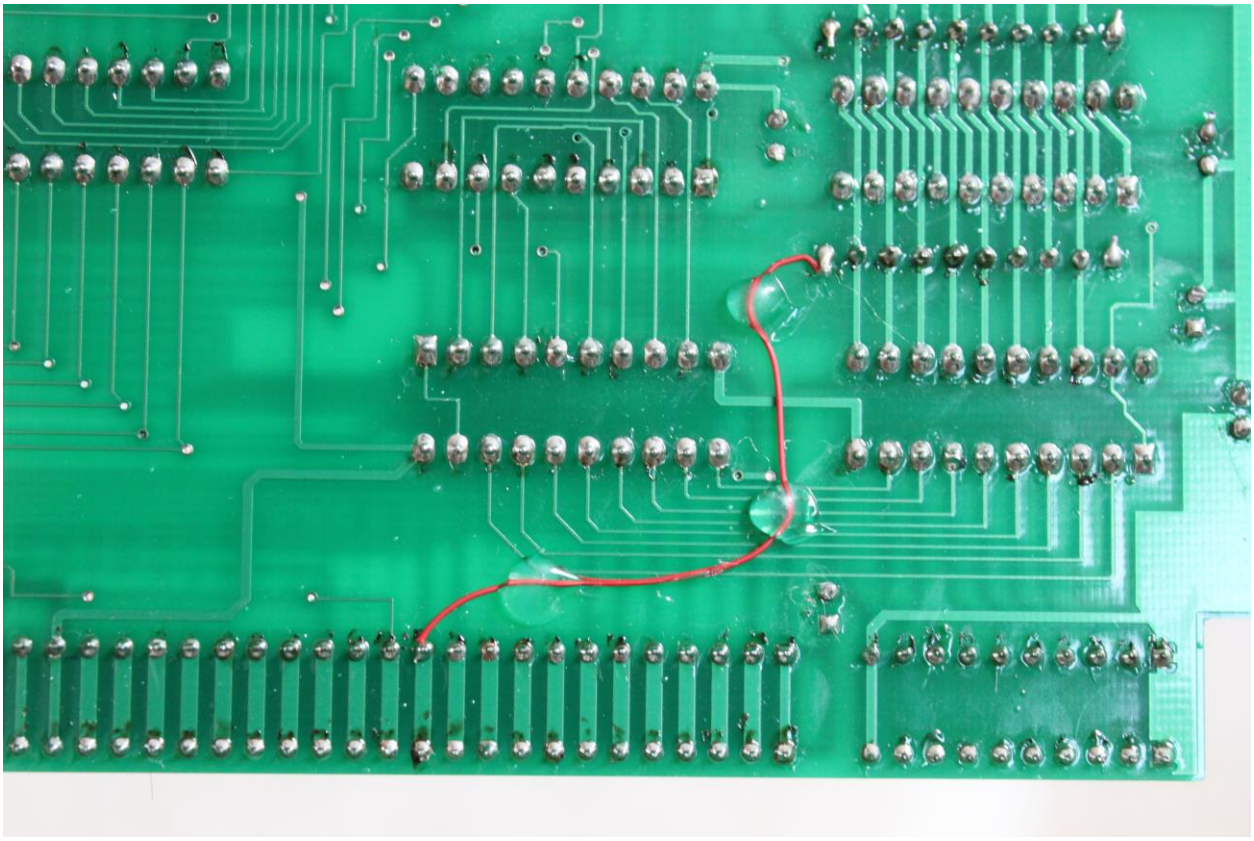



21. Install U2 – 74LS06 IC.
22. Install U1 – 74LS14 IC.
23. Install U7 - 74LS08 IC.
24. Install U8 – 74LS74 IC.

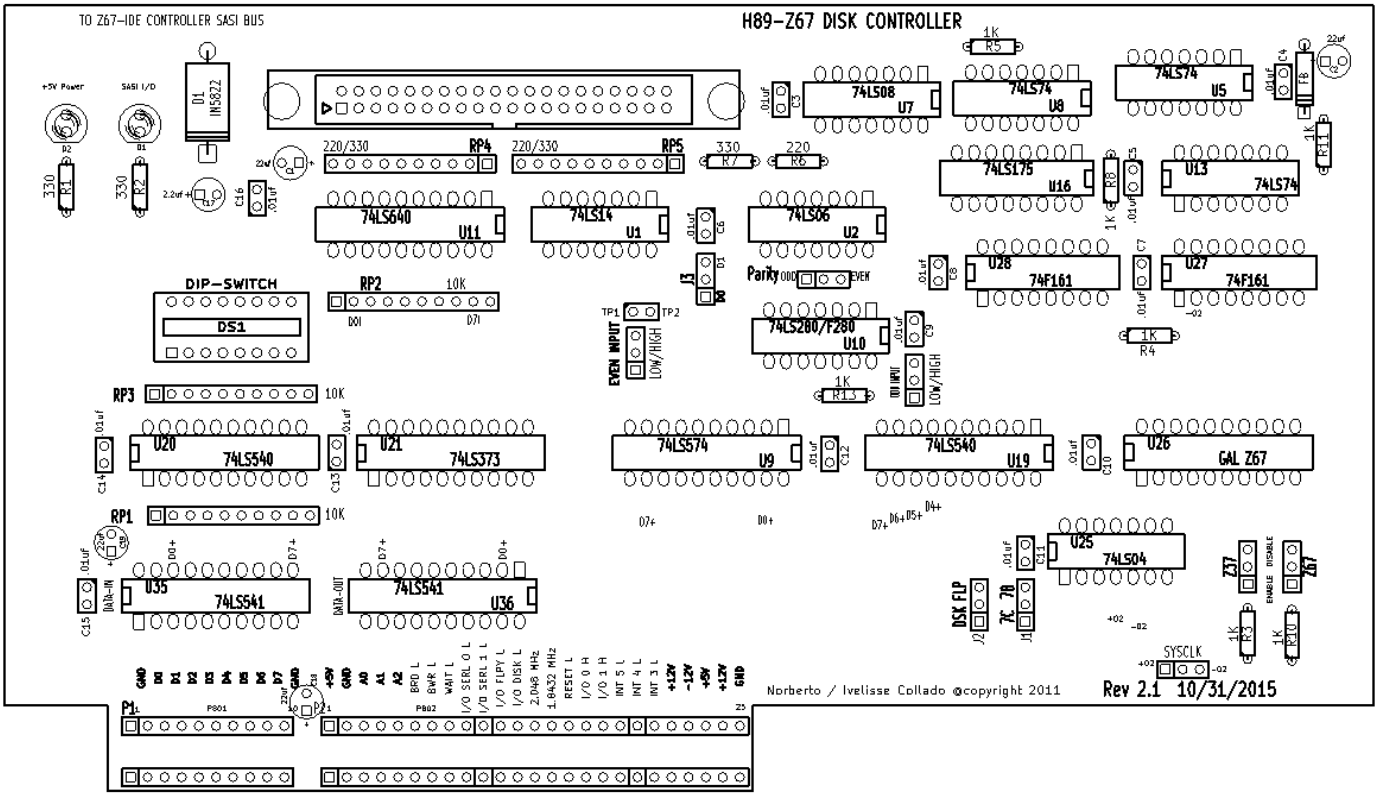
25. Install U5 – 74LS74 IC.
26. Install U13 – 74LS74 IC.
27. Install U25 – 74LS04 IC.
28. Install U16 – 74LS175 IC.
29. Install U28 – 74F161 IC.
30. Install U27 – 74F161 IC.
31. Install U26 – GAL-Z67 IC.
32. Install U11 – 74LS640 IC.
33. Install U19 – 74LS540 IC.
34. Install U9 – 74LS574 IC.
35. Install U21 – 74LS373 IC.
36. Install U20 – 74LS540 IC.
37. Install U35 – 74LS541 IC.
38. Install U26 – 74LS541 IC.

# H89-Z67 Board Rework

1. Solder a wire from RP1 10K PIN #10 to P2 PIN #12 as shown below.
2. This is required to support the H89-Z67 board on P506 and P512 connectors for the system to operate properly.



# H89-Z67 Board Components



# H89-Z67 Board Fully Assembled