CPU Board Troubleshooting

POWER SUPPLY CHECK OK

U565 (output pin)	-12 VDC	☐
U566 (output pin)	-5 VDC (A)	☐
U569 (output pin)	-5 VDC (B)	☐
P516-3	+5 VDC	☐
U567 (output pin)	+12 VDU (A)	☐
U568 (output pin)	+12 VDU (B)	☐

CLOCK CIRCUITS CHECK

2.048 MHz (0.488 uS) Clock

U504-6 (CPU) ☐
U556A-3 (Single Step) ☐
U512A- 3 (RAM Address MUX) ☐

500 Hz (2 mS) Clock

U506B-11 (2 mS Clock) ☐

1.8432 MHz (.543 uS) Clock

U567-17 (ACE) ☐

Also check the ACE internal clock to R CLK (U561-15). This should be a non-symmetrical square wave with a period of about 6.3 uS (see the waveform on the schematic). ☐

RESET CIRCUITS CHECK OK

The following test points should be logic one. Simultaneously pressing the RIGHT SHIFT and RESET keys will cause them to pulse low, then return to logic one.

U504-26 (CPU) ☐
U506B-10 (2 mS Clock) ☐

U552-1 (General Purpose Port) ☐
U515-12 (Inverter to ACE reset pin) ☐

The following test points are normally low and will pulse high, then back to zero, when RIGHT SHIFT/RESET keys are pressed and released.

U503-11 (500 Hz Clock) ☐
U561-35 (ACE.) ☐

OK AUTOMATIC MEMORY TEST

By setting SW501 to cause the CPU to jump to the memory test built into the system ROM, U518, and watching the results on the CRT, several circuits can be eliminated. This memory test resides totally in MTR-88 and uses the Z80 registers as a scratchpad. This allows it to check every byte in the user's dynamic memory.

Note: S501-5 will not cause an automatic memory test when running the MMS-84B ROM.

☐ Place section #5 of SW501 into its logic zero position. All switch sections should now be in the zero position.

Press the RIGHT SHIFT/RESET keys.

☐ If the memory test proceeds normally (see the discussion on memory testing in the Diagnostics section, page 164), then the CPU, the Memory Map decoder and dynamic RAM are probably okay; it is possible for the system ROM (U518) to proceed normally through the memory test but still have a faulty bit pattern in it. To check this, place SW501, section 5 into its logic one position and power-up the H89. If it will not go into the monitor mode, substitute the monitor ROM. If the problem still exists, then proceed to Checking the Bus Lines. Otherwise, go to Diagnostics.

☐ If the memory test prints the correct display, but fails immediately, then possibly the address bus is bad (see "Checking the Bus Lines"), or the memory is bad (see "Memory Testing"), or the Memory Map Decoder is faulty. Check pull-up resistors RP506 and RP507. Also try substituting U517. Check JJ501 through JJ504.

☐ If the memory test does not activate at all, then try substituting the system ROM (U518), the Memory Map Decoder (U516), and check JJ505 through JJ507. Verify correct operation of the address, data and control lines to the Memory Map Decoder and System ROM. The section, "Checking the Bus Lines", covers techniques on doing this.

☐ Set section 5 of SW501 back to its "one" position and press RIGHT SHIFT/RESET.

OK OTHER POSSIBLE CAUSES

The schematic shows the correct logic states for the WH89 immediately after a reset and idling in the monitor mode. If the pulses on the outputs of U509, U510, or U511 appear abnormal: check the CPU (U504) first.

☐ - Check if the address lines are pulsing. If not, then check the status of LA L (U515A-1) before going further.

If the Z80 (U504) checks okay, and the RAM and ROM circuits appear okay, then check the console Serial Port. Here's how:

☐ - Check that SW501, section 5, is in the logic one position and press RIGHT SHIFT/RESET.

☐ - Check U561-14 (ACE) for continuous pulsing. If not pulsing, check the 10 Map Decoder (U550) and support circuits.

☐ - Check U561-11 for idle at logic one and pulse each time the SHIFT/RESET is pressed and released. If not, check U561 the ACE) and its support lines. If it does pulse, then the serial output path is open somewhere between the ACE and the Terminal Logic board.

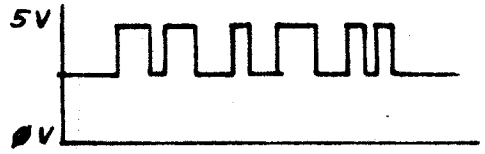
At this point, the major causes of the WH89 not properly powering-up into the monitor mode have been covered. It is possible that the faulty component has not been found yet. Such circuits as the General Purpose Port and the Interrupt circuits may also be the cause. You should:

☐ - Compare the levels in these areas to those shown on the schematic.

☐ - Check the CPU's "unused" lines. Are any of them asserted when they shouldn't be?

CHECKING THE BUS LINES

For quick checking, a logic probe can be used. Note, however, that occasionally a TTL logic circuit can internally short to the +5 volt supply (either its input or output) and exhibit the characteristic of outputting an "undefined" state of about 1.5 volts. If this is on a line shared by other ICs, their outputs will override this level to give a waveform similar to the one shown below:



Measuring this line with a logic probe may indicate normal operation. Although some probes will show pulses going from "open circuit" to logic one, this can be easily overlooked. In this case, an oscilloscope will give a quick and definite indication of a faulty line.

The short circuit can be more direct, causing zero ohms between a bus line and +5 volts, ground, or another bus line. If this were to occur, it would most likely be a shorted IC, rather than a solder bridge, as this board is factory assembled and tested. Since the ICs are installed in plug-in sockets, it is perhaps quickest to place an ohmmeter across the shorted lines and start pulling ICs until the reading jumps up from zero ohms.