AMERICAN MICROSYSTEMS, INC.

S2350

Universal Synchronous Receiver/Transmitter

Features

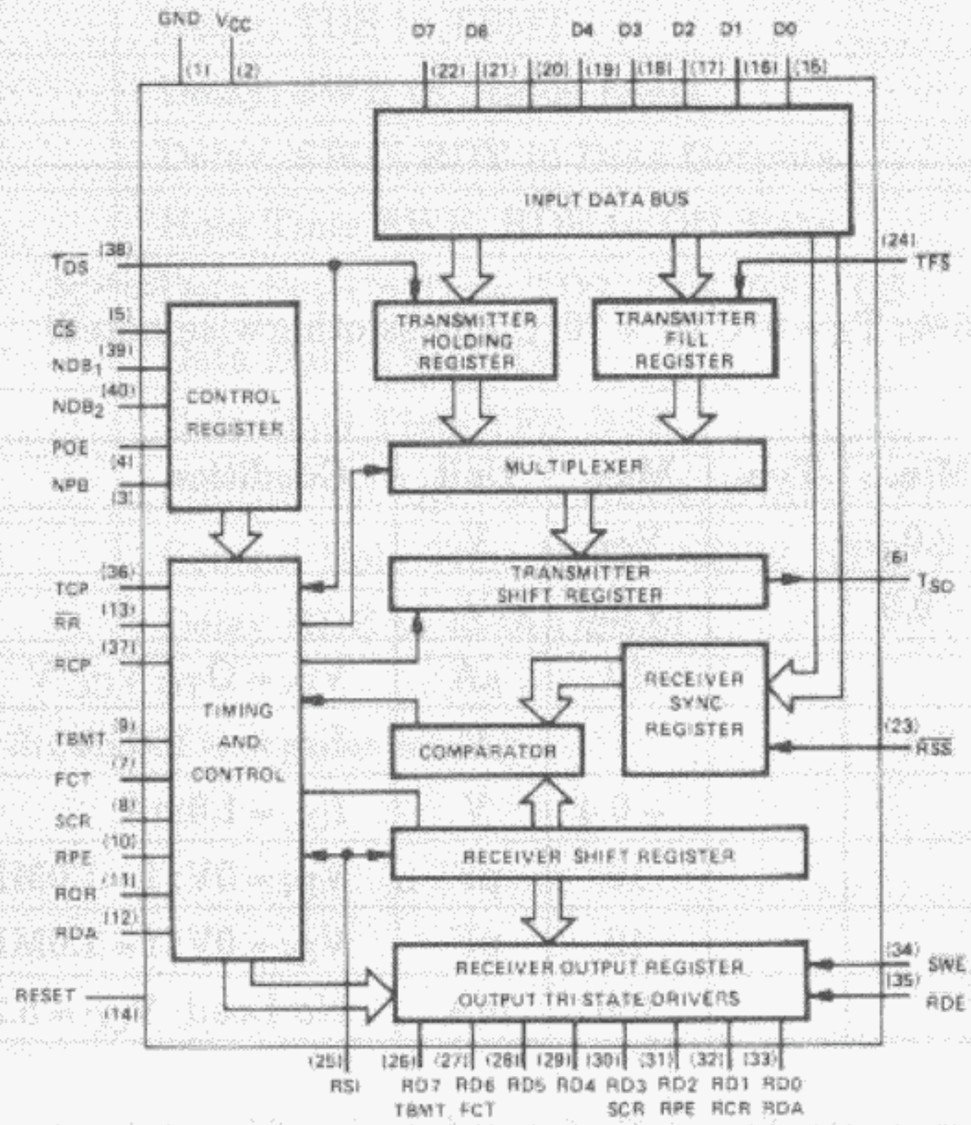
- 500kHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5-8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5V)
- Input/Output TTL-Compatible

General Description

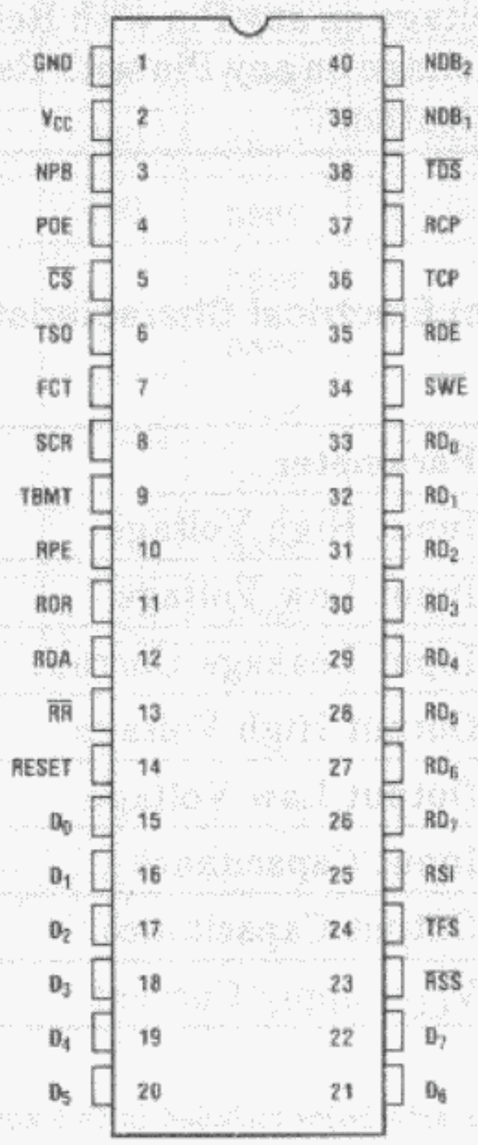
The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial-to-parallel and parallel-to-serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Block Diagram



Pin Configuration



Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8-bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

Typical Applications

- ☐ Computer Peripherals
- ☐ Communication Concentrators
- ☐ Integrated Modems
- ☐ High Speed Terminals
- ☐ Time Division Multiplexing
- ☐ Industrial Data Transmission

Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on any Pin with Respect to GROUND	+7V
Negative Voltage on any Pin with Respect to GROUND	−0.5V
Power Dissipation	0.75W

D.C. (Static) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
I_{IL}	Input Leakage Current			10	μA	V_{IN} = O_{TO} V_{CC} V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
V_{OL}	Output Low Voltage			+0.4	V	I_{OL} = 1.6mA
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0V; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0V; f = 1.0MHz
I_{CC}	V_{CC} Supply Current			100	mA	No Load; V_{CC} = 5.25V

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

A.C. (Dynamic) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC		500	kHz	
Input Pulse Widths						
P_{TCP}	Transmit Clock	900			nsec	CL = 20pF
P_{RCP}	Receive Clock	900			nsec	1TTL Load
P_{RST}	Reset	500			nsec	
P_{TDS}	Transmit Data Strobe	200			nsec	
P_{TFS}	Transmit Fill Strobe	200			nsec	
P_{RSS}	Receive Sync Strobe	200			nsec	
P_{CS}	Control Strobe	200			nsec	
P_{RDE}	Receive Data Enable	400			nsec	Note 1
P_{SWE}	Status Word Enable	400			nsec	Note 1
P_{RR}	Receiver Restart	500			nsec	
Switching Characteristics						
T_{TSO}	Delay, TCP Clock to Serial Data Out			700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output			1.4	μsec	
T_{TBMT}	Delay, TDS to TBMT			700	nsec	
T_{STS}	Delay, SWE to Status Reset			700	nsec	
T_{RDO}	Delay, SWE, RDE to Data Outputs			400	nsec	1TTL Load
T_{HRDO}	Hold Time SWE, RDE to Off State			400	nsec	C_L = 130pF
T_{DTS}	Data Set Up Time TDS, TFS, RSS, CS	0			nsec	
T_{DTH}	Data Hold Time TDS	700			nsec	
T_{DTI}	Data Hold Time TFS, RSS	200			nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0			nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200			nsec	
T_{RDA}	Delay RDE to RDA Output	700			nsec	

NOTE 1: Required to reset status and flags.

Figure 1. Timing Waveform

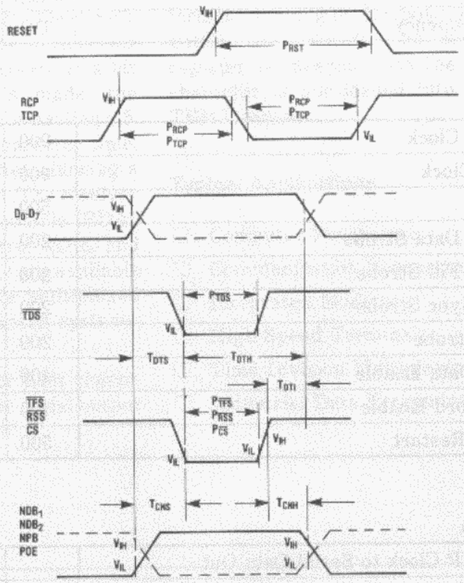


Figure 2. Timing Waveform

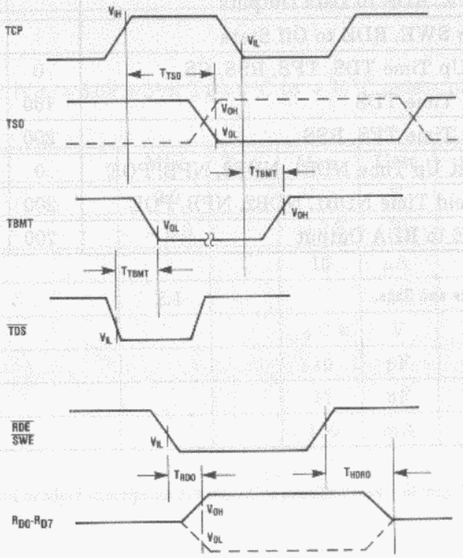
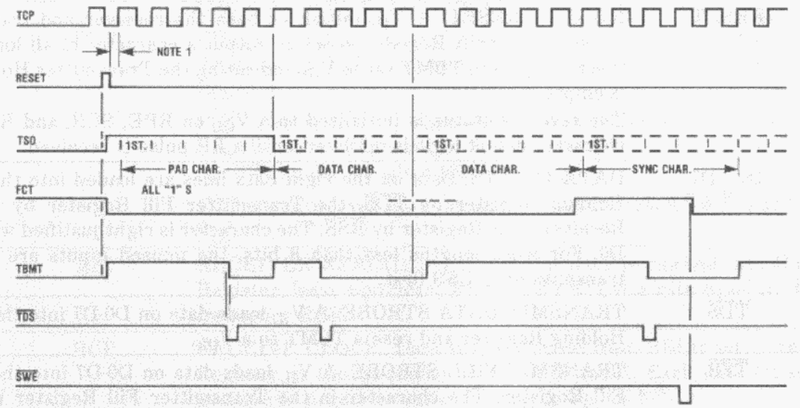
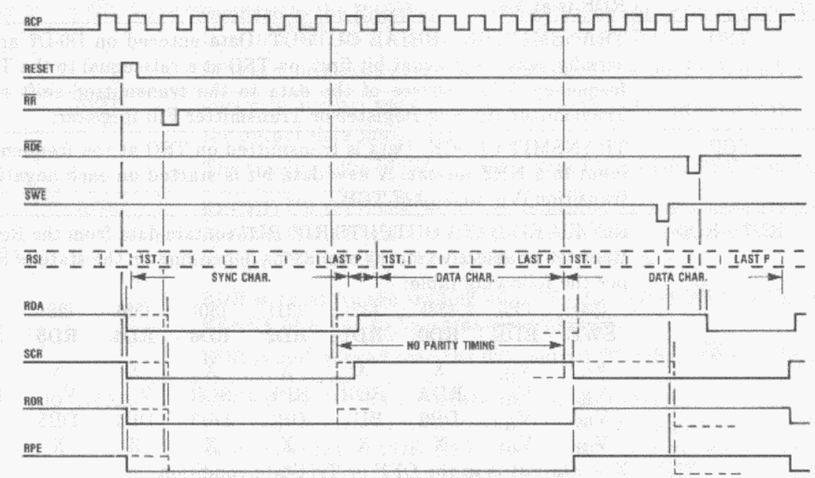


Figure 3. Transmitter Timing Diagram



NOTE 1: DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

Figure 4. Receiver Timing Diagram



Pin Definitions

Pin	Label	Function
(1)	GND	Ground
(2)	V_{CC}	+5 Volts ±5%
(14)	RESET	MASTER RESET. A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty. The receiver status is initialized to a V_{OL} on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.
(15–22)	D0–D7	DATA INPUTS. Data on the eight data lines are loaded into the Transmitter Holding Register by $\overline{TDS}$, the Transmitter Fill Register by $\overline{TFS}$, and the Receiver Sync Register by $\overline{RSS}$. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.
(24)	$\overline{TFS}$	TRANSMIT FILL STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE. A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	TRANSMIT BUFFER EMPTY. A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on $\overline{TDS}$. A V_{IH} on RESET sets TBMT to a V_{OH}. TBMT is also multiplexed onto the RD7 output (26) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(6)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK. Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.
(26–33)	RD7–RD0	RECEIVED DATA OUTPUTS RD0-RD7 contain data from the Receiver Output Register or selective status conditions depending on the state of $\overline{SWE}$ and $\overline{RDE}$ per the following table:

(34) $\overline{SWE}$	(35) $\overline{RDE}$	(33) RD0	(32) RD1	(31) RD2	(30) RD3	(39) RD4	(28) RD5	(27) RD6	(26) RD7
V_{IL}	V_{IL}	X	X	X	X	X	X	X	X
V_{IL}	V_{IH}	RDA	ROR	RPE	SCR	V_{OL}	V_{OL}	FCT	TBMT
V_{IH}	V_{IL}	DB0	BD1	DB2	DB3	DB4	DB5	DB6	DB7
V_{IH}	V_{IH}	X	X	X	X	X	X	X	X

X — Output is in the OFF or Tri-State condition
DB0 — LSB of Receiver Output Register
DB7 — MSB of Receiver Output Register
The two unused outputs are held at V_{OL} in the output status condition.

Pin Definitions (continued)

Pin	Label	Function
(35)	$\overline{RDE}$	RECEIVE DATA ENABLE. A V_{IL} enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$ resets RDA to the V_{OL} condition.
(7)	FCT	FILL CHARACTER TRANSMITTED. A V_{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V_{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V_{IL} to V_{IH}) of the $\overline{SWE}$ pulse, or when RESET is V_{IH}. FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(25)	RSI	RECEIVER SERIAL INPUT. Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.
(37)	RCP	RECEIVE CLOCK. Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V_{IH} to V_{IL}) of RCP.
(12)	RDA	RECEIVED DATA AVAILABLE. A V_{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V_{OL} on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(8)	SCR	SYNC CHARACTER RECEIVED. A V_{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V_{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{SWE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V_{IL} and $\overline{RDE}$ is V_{IH}.
(34)	$\overline{SWE}$	STATUS WORD ENABLE. A V_{IL} enables the internal status conditions onto the output data lines RD0–RD7. The trailing edge of $\overline{SWE}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.
(11)	ROR	RECEIVER OVERRUN. A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost. ROR is reset by the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$, a V_{IH} on RESET or a V_{OL} to V_{OH} transition of RDA. ROR is multiplexed onto the RD1 output (32) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(10)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE. RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RPE is multiplexed onto the RD2 output (31) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.

Pin Definitions (continued)

Pin	Label	Function
(13)	$\overline{RR}$	RECEIVER RESTART. A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{RR}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time. **NOTE:** Parity is not checked on the first sync character but is enabled for every succeeding character.
(39)	NDB1	NUMBER DATA BITS. The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit. NDB2 / NDB1 / CHARACTER LENGTH V_{IL} / V_{IL} / 5 Bits V_{IL} / V_{IH} / 6 Bits V_{IH} / V_{IL} / 7 Bits V_{IH} / V_{IH} / 8 Bits For character length less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.
(3)	NPB	NO PARITY BIT. A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.
(4)	POE	PARITY ODD/EVEN. A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces parity operation. NPB must be V_{IL} for parity to be enabled.
(5)	$\overline{CS}$	CONTROL STROBE. A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{CS}$ can be tied directly to ground.