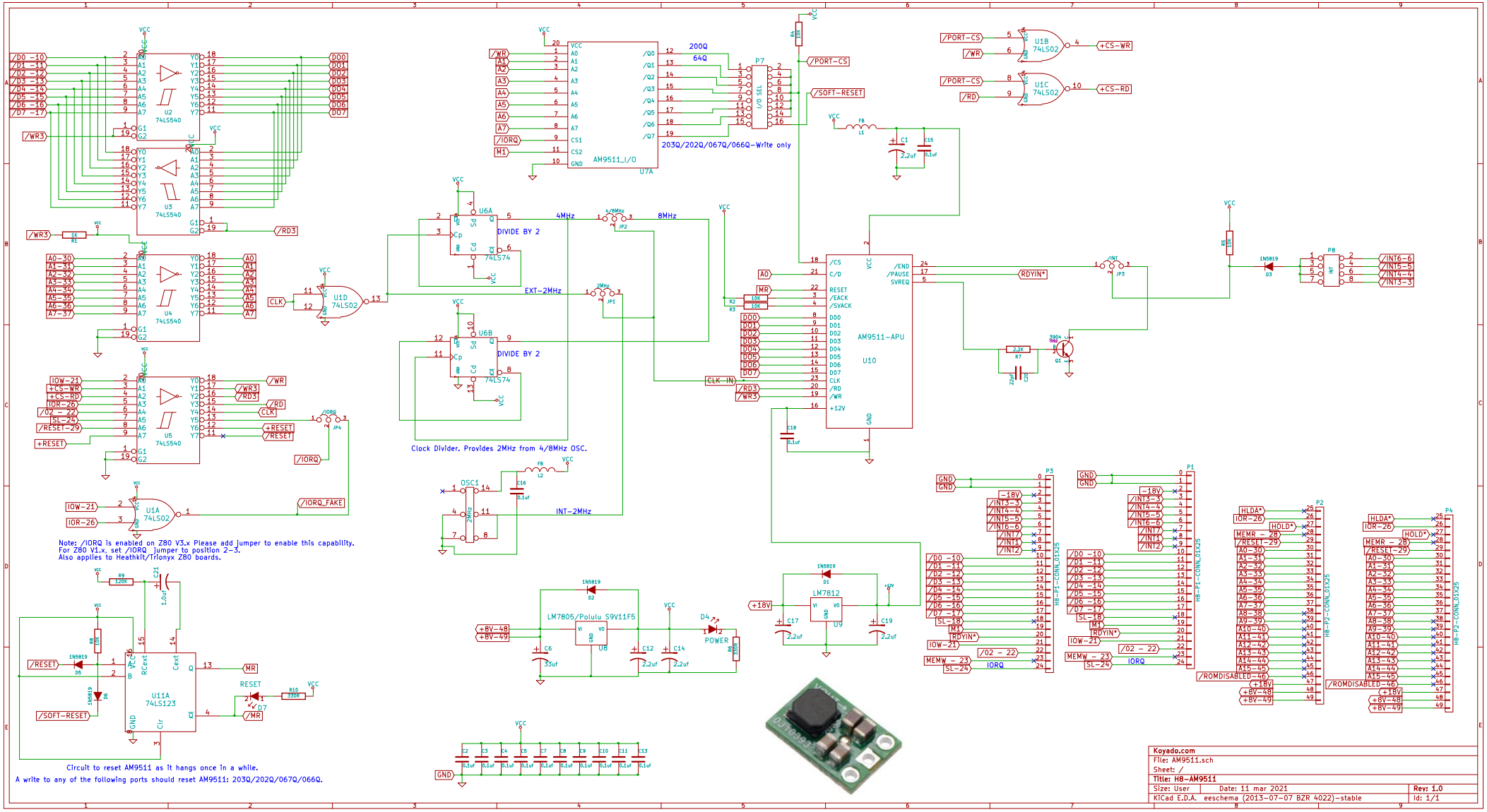
U2 74LS540
U3 74LS540
U4 74LS540
U5 74LS540
U1D 74LS02
U1A 74LS02
U1B 74LS02
U1C 74LS02
U11A 74LS123
U7A AM9511_I/O
200Q
64Q
203Q/202Q/067Q/066Q-Write only
U6A DIVIDE BY 2
U6B DIVIDE BY 2
74LS74
4MHz
8MHz
EXT-2MHz
INT-2MHz
Clock Divider. Provides 2MHz from 4/8MHz OSC.
U10 AM9511-APU
LM7805/Polulu S9V11F5
LM7812
POWER
Note: /IORQ is enabled on Z80 V3.x Please add jumper to enable this capability.
For Z80 V1.x. set /IORQ jumper to position 2-3.
Also applies to Heathkit/Tlonyx Z80 boards.
Circuit to reset AM9511 as it hangs once in a while.
A write to any of the following ports should reset AM9511: 203Q/202Q/067Q/066Q.
Koyado.com
File: AM9511.sch
Sheet: /
Title: H8-AM9511
Size: User
Date: 11 mar 2021
Rev: 1.0
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 1/1