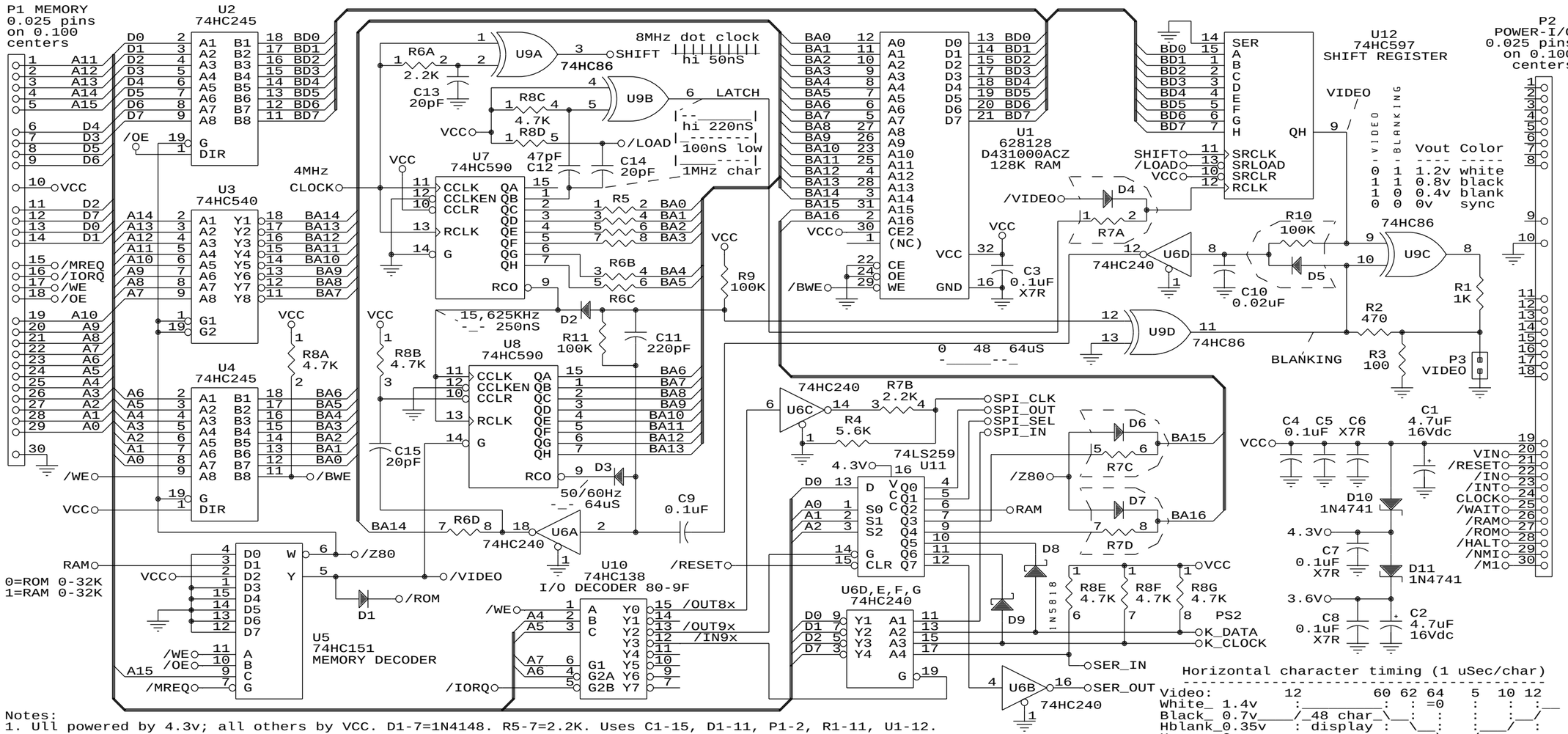

Notes:
1. Ull powered by 4.3v; all others by VCC. D1-7=1N4148. R5-7=2.2K. Uses C1-15, D1-11, P1-2, R1-11, U1-12.

2. MUX RAM between video/Z80. Video needs a character every 1000nS. Z80 needs 375 or 500nS. That leaves enough time to access both in each 1000nS cycle.

3. Must load video into shift register exactly every 1000nS. But Z80 might be using RAM at that time. 74HC597 has input reg AND shift reg. Load input reg when data available:
- If /VIDEO=0 (no Z80 access), at end of video read cycle.
- If /VIDEO=1 (Z80 using RAM), latch when /VIDEO goes high.
The input reg is then copied into the shift reg at the end of the video read cycle (when LATCH goes high).

4. Hardware HBLANK and VBLANK signals combined to make BLANK. RAM data is video when BLANK=1, HSYNC and VSYNC when BLANK=0. HBLANK=12uS, set by R11*C11. HSYNC=5uS, set by 5 FFh in RAM. VBLANK starts at line 254, ends at line 260 or 312 by VSYNC. VSYNC=3 lines, set by R10*C10 and 3 lines of FFh in RAM.

```
VBLANK 0  256 260
 60Hz _------_-
 50Hz _------___-
 lines 0  256   312
```

Timing Diagram

```
CLOCK   __--__--__--__--__--__ 4MHz  from Z80 CPU board
U7-QA   --____----____----____ 2MHz
U7-QB   --________--------____ 1MHz  character clock
/LOAD   --_________________--- 100nS low=load shift register
SHIFT   -_-_-_-_-_-_-_-_-_-_-_ 8MHz  dot clock
U12-QH  0 7 6 5 4 3 2 1 0 7 6  video shift reg. output bit
```

U12 input register RCLK (loads on rising edge)

```
LATCH   __---_________________---_ 220nS high=RAM data changing
 RCLK   __---_________________---_ /VIDEO=0 (no Z80 access)

1./VIDEO _--------_______________   example Z80 accesses:
 RCLK   _--------_________---_ 1. latch at end (usual time)
                        ^
2./VIDEO _____--------_________
 RCLK   __----------_____---_ 2. latch at end. less RAM
                        ^       access time, still enough
3./VIDEO _________--------_____
 RCLK   __---____--------_---_ 3. latch early. may be glitch
                  ^     ^       pulse at end, bad data?
4./VIDEO _______________-------__ 4. latch early
 RCLK   __---_________--------_
                        ^
```

Horizontal character timing (1 uSec/char)

```
Video:          12          60 62 64    5  10 12
White_ 1.4v     :__________:  : =0  :  :  :  :__
Black_ 0.7v____/_48 char_\__:  :   :  :  :__/
Hblank_0.35v  : display  :  \__:   :  :__/
Hsync_ 0v     :          :  :  \___/  :  :
15.625KHz          48      2  2  5    5   2
```

Vertical display timing (in scan lines)
Hsync pulses maintained throughout Vsync

```
PAL:  312=0     225 255 258 261 264 282 312=0
NTSC: 260=0     225 233 236 239 242 252 260=0
White_  :_______:   :   :   :   :   :     :_
Black___:/__225__\:___:   :   :   :   :____:/_
Vblank_ : display :   \___:___:___/   :     :
Vsync_  :         :       :   :       :     :
NTSC 60.096Hz 225   8   3   3   10    8
PAL  50.08Hz  225  30   3   3   3   18   30
   equalizing pulses_||||||||||||
```

TMSI c/o Lee Hart		
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